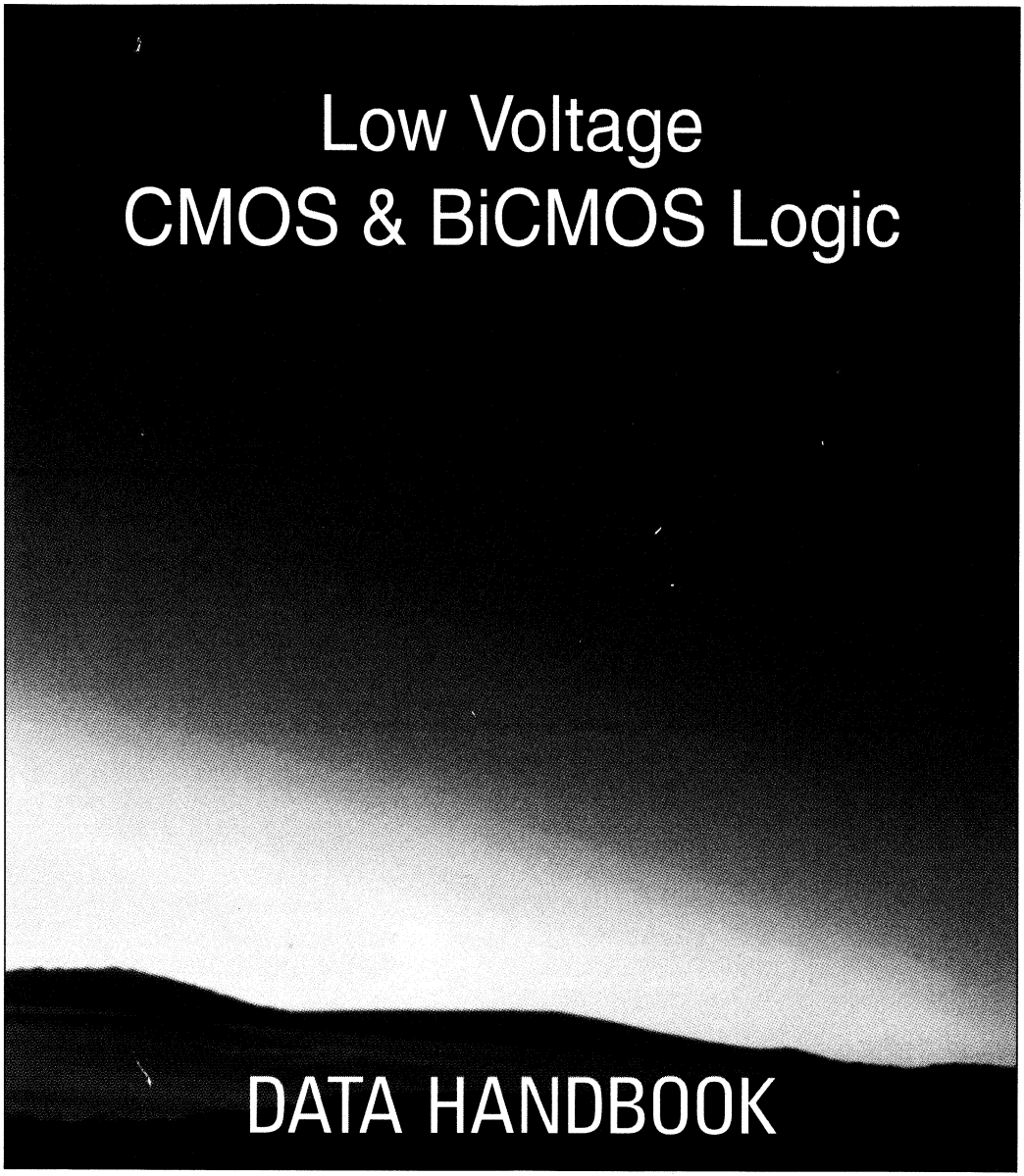
Low Voltage CMOS & BiCMOS Logic



DATA HANDBOOK

BOOK IC24 1995

Philips Semiconductors

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LOW VOLTAGE CMOS AND BiCMOS LOGIC FAMILIES

LV, LVC, HLL, ALVC and LVT 3.3V PLDs

Printed in USA

Preface

This data book provides the broad selection of Philips Standard and Programmable Logic functions developed for 3.3 Volt supply. The families have been defined to meet your emerging requirement for systems featuring low power, high performance, or portability.

These parts are manufactured on the most advanced CMOS and BiCMOS technologies. The Standard Logic packaging includes the traditional Philips SO concepts, and the new Philips SSOP (Shrink Small Outline Package) and TSSOP (Thin Shrink Small Outline Package) in single as well as multiple byte levels. For Standard Logic, Texas Instruments and Hitachi are the second sources, ensuring global industry standardization for these families.

Philips' commitment to the Standard and Programmable Logic markets is evident in this program. From our worldwide design centres, we integrate our performance to you with common product definition, design and qualification tools, total quality processes, and a cycle time focus that will ensure you have the products you need, when you need them.

We want to be **Your First Choice for the Products we Provide**. Please let us know what we can do to meet your needs. Thank you.

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Contents

Section 1 - General Information

Section 2 - Low Voltage HCMOS (LV)

*) considered for future introduction

Contents

Section 2 - Low Voltage HCMOS (LV) (continued)

Section 3 - Low Voltage CMOS (LVC)

*) considered for future introduction

Contents

Section 3 - Low Voltage CMOS (LVC) (continued)

Section 4 - HLL

Section 5 - Advanced Low Voltage CMOS (ALVC)

Contents

Section 6 - Low Voltage Technology (LVT)

Section 7 - Low Voltage Technology MULTIBYTE (LVT16)

Section 8 - 3.3V PLDs

Section 9 - Package Information

Contents

Section 9 - Package Information (continued)

Fast, low-power LV, LVC, HLL and LVT logic families

This databook gives device data about Philips Semiconductors low-voltage CMOS and BiCMOS logic families. The following families were introduced for the low voltage market: LV, LVC, HLL, ALVC, LVT and LVT16. All families are complete new designs, optimised for 3.3 V operation.

EDP MARKET TRENDS

The heavy load imposed on EDP equipment by the ever-increasing complexity of modern software has led to the recent entry into the market of 'power PCs' using PC60x and workstations with RISC R4000/ R6000 and ALPHA processors. Also, the speed of the processors used in desktop computers and other mains-fed EDP equipment is increasing as typified by the migration from '386 to '486 and Pentium® processors. This, in turn, has caused a demand for equally high-performance portable EDP equipment. Such equipment demands a low voltage supply and sufficiently low power consumption to allow extended periods of operation from 1, 2 or 3 battery cells without recharging. This type of equipment includes memory cards for laptop computers, point-of sales equipment, personal digital assistants, mobile radios, hand-held video games, telecom equipment and instrumentation.

To satisfy the component needs of equipment manufacturers' for this smaller, faster and lower-power equipment with extended battery life, it has been necessary for logic IC manufacturers to increase the speed of their products by using very small dimensions on their chips. This leads to a reduction of maximum supply voltage from 5 V to 3.3 V. Many new 3.3 V ICs such as 'x86 and 680X0 microprocessors, memory, ASICs, disk controllers, flat-panel LCD controllers, data converters and regulators are available on the market. This has added considerable momentum to the demand for fast, low voltage 'glue logic' ICs to complete the chip-sets for fast, low voltage EDP applications. Philips has responded to this demand with six new low voltage CMOS and BiCMOS logic families to complement their existing range of logic ICs.

We have four new single byte and basic function families:

- LV (Low-voltage, high speed CMOS) logic which is a 3.3 V version of our HCMOS family.
- LVC (Low-voltage CMOS) logic which is a 3.3 V family compatible with FAST logic
- HLL (High-speed Low-power Low-voltage) is the fastest 3.3 V CMOS logic available
- LVT (Low-Voltage Technology) advanced BiCMOS logic which is a 3.3 V version of ABT logic.

In addition we introduced two low voltage Multibyte families:

- ALVC (Advanced Low Voltage CMOS) which is basically the Multibyte™ version of HLL
- LVT16 (Low-Voltage Technology Multibyte) advanced BiCMOS logic which is the 3.3 V version of ABT16. LVT16 is the fastest low voltage family on the market.

The CMOS families have a wide operating supply voltage range 1.2 V (LV even from 1.0 V) to 3.6 V, and the BiCMOS LVT and LVT16 families operate from 2.7 V to 3.6 V. All the families have very low power consumption to make them an ideal choice for battery or mains-powered EDP applications where high speed and low power consumption are prime considerations.

Package Considerations

Market trends with respect to logic IC packages are to aim for smaller PCB area, thinner packages and fewer packages for each application. This puts emphasis on SSOP (Shrink Small Outline Package) type II packages, TSSOP (Thin Small Outline Package) type I packages and multibyte packages SSOP type III and TSSOP type II for 48-56 pins. Furthermore, except for LV, there will be no DIL packages due to the noise generated. The new logic families are available in the following packages:

- Standard JEDEC SO (Small Outline)
- US/Japanese standard SSOP EIAJ type II (14-28 pins)
- Japanese standard TSSOP EIAJ type I (14-28 pins)
- Jedec standard SSOP type III (48-56 pins)
- Japanese standard TSSOP EIAJ type II (48-56 pins)

The multibyte parts (LVT16 and ALVC) and HLL have multiple supply and ground pinning to obtain the fastest possible switching. All other 3 V families have corner supply and ground pinning.

Second-source Agreements.

Philips have come to a second-source agreement with Texas Instruments for LV, LVC, ALVC, and LVT.

In addition, Hitachi is a second-source for these families. The new logic families are therefore set to become industry standards.

SUPPLY VOLTAGE CONSIDERATIONS

There are three main reasons for reducing the supply voltage of logic ICs:

- To allow them to be used in portable battery-powered equipment
- To reduce power consumption (dissipation) so that the size and weight of portable equipment can be reduced and can function for longer periods without recharging the battery
- Very fast new processors must be fabricated with finer process geometry limiting the supply voltage to 3.6 V.

Other benefits of a low supply voltage include lower noise levels, reduced EMI, and improved reliability due to reduced stresses on the ICs. A supply voltage level of 3.3 V ±0.3 V is common for

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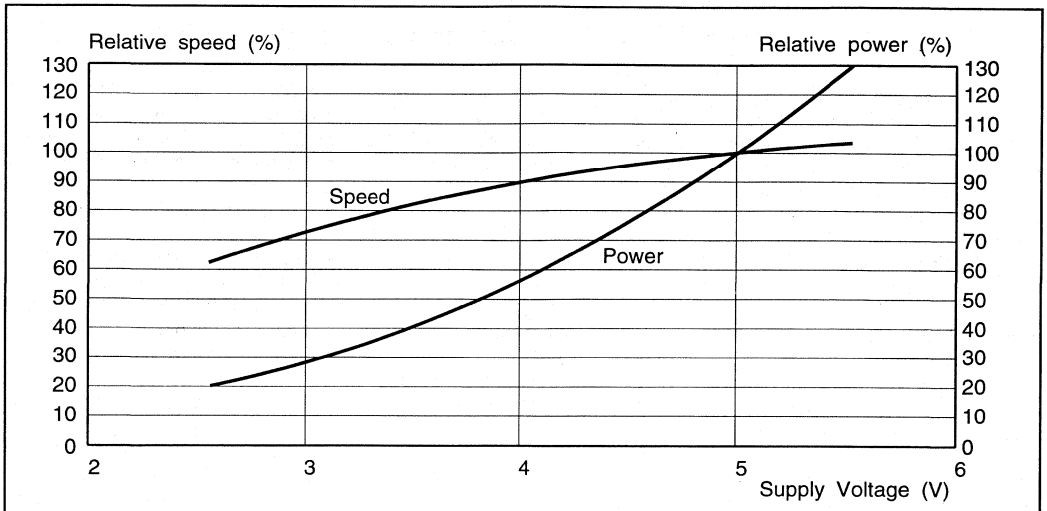


Fig.1 Normalised speed and power dissipation of logic ICs

equipment with a regulated supply and is also supported by JEDEC. For battery operation, the requirements are more stringent because the supply voltage variation is greater. For example, at the end of their operating life, a pair of Alkaline or Carbon Zinc batteries can only supply about 1.8 V, and a single NiCd cell provides only 1.2 V just before it needs recharging. The wide supply voltage range and output drive levels of LV, LVC, HLL and ALVC ICs allow them to be powered from any of these sources.

Reducing the Supply Voltage Without Losing Speed

As shown in Fig.1, the dynamic power dissipation of logic ICs diminishes approximately with the square of the supply voltage reduction. An obvious method of minimizing the power consumption of these circuits is therefore to reduce the supply voltage of 5 V to 3.3 V. Fig.1 shows that this reduction of supply voltage reduces the power consumption by about 65%, and leads to a speed reduction of only 20%. The immediate advantages gained simply by moving from 5 V to 3.3 V are therefore that the speed/power ratio is more than doubled, and it becomes possible to power CMOS logic from a 1-cell or 2-cell battery in portable equipment.

The reduction of maximum speed resulting from the supply voltage reduction can be restored, and even increased, by using finer geometry and sub-micron technology which is tailored for low-power and low-voltage applications. We have used both supply voltage reduction and speed enhancement techniques for our logic families.

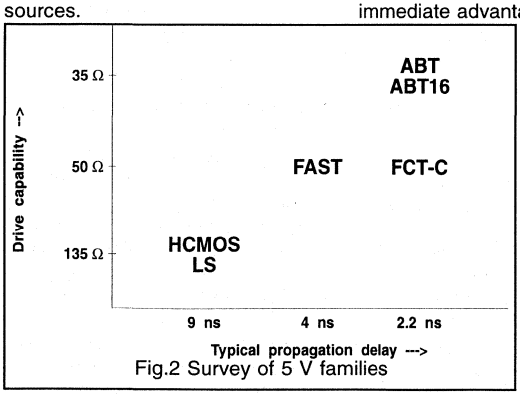


Fig.2 Survey of 5 V families

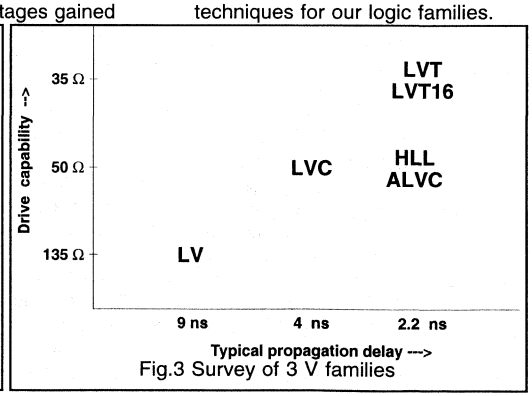


Fig.3 Survey of 3 V families

Table 1 THE COMPLEMENTARITY OF OUR LOW VOLTAGE LOGIC FAMILIES

Feature	LV	LVC	HLL	ALVC	LVT	LVT16
Process	CMOS	CMOS	CMOS	CMOS	BiCMOS	BiCMOS
Speed	medium	high	very high	very high	very high	very high
Product range	switches gates/FF decoders MUX/DEMUX octals	gates/FF decoders MUX/MUX octals	octals	multibyte	octals	multibyte
Output drive	low	high	high	high	very high	very high
5 V input[1)]	no	yes	yes	yes	yes	yes
Overvoltage protection	no	no	no	no	yes	yes
Live insertion support	no	no	no	no	yes	yes
5 V equivalent	LS, HC, N74	F, ACL	FCT-C	FCT16-C	ABT, BCT, FCT-A	ABT16, FCT16-C
Primary applications	glue logic portable eq.	glue logic portable eq. local bus	portable eq. local bus super µP	portable eq. local bus super µP	local bus super µP backplanes	local bus super µP backplanes

[1)] See Table 2 for details

WHY SIX LOW-VOLTAGE LOGIC FAMILIES FROM PHILIPS?

As shown by the 5 V logic family drive capability as a function of speed positioning in Fig.2, there are two main clusters of 5 V logic families:

- LSTTL, HCMOS (HC/HCT)
- FAST, ALS, ACL, QFACT.

The most important trends in 5 V logic are:

- higher speed (FCT-C)
- increased output drive capability combined with higher speed and added features such as live-insertion support (ABT)
- further multibyte integration (ABT16)

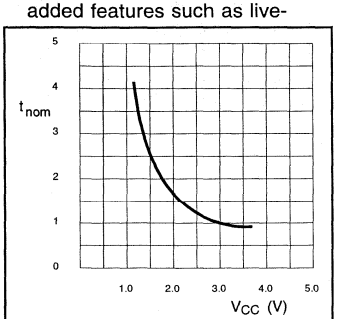


Fig.4 Normalised derating curve for typical propagation delay (t_p)

As shown in Fig.3, Philips have used essentially the same approach for the new low-voltage logic families which together achieve complete coverage of market requirements for 3.3 V logic. Each of the new families has a unique product differentiator:

- LV is a 3.3 V medium speed CMOS family which is compatible with LS and HCMOS
- LVC is an advanced 3.3 V CMOS logic family which is compatible with FAST, ALS and their CMOS equivalents
- HLL is the world's fastest 3.3 V CMOS family with centre supply pinning and featuring low skew, low EMI and a speed as FCT-C
- ALVC is the Multibyte version of HLL
- LVT is a 3.3 V BiCMOS family which is optimized for driving backplanes and features live insertion/auto 3-state, bus hold and outputs that can handle overvoltage. It is compatible with ABT, BCT and FCT-A.
- LVT16 is the Multibyte version of ABT16 having the same features as LVT and a speed that is even faster than LVT.

Not only for their specific properties, but also for product portfolio the families are complementary as detailed in Table 1.

FEATURES OF THE NEW LOW-VOLTAGE LOGIC FAMILIES

Features common to all our new 3 V logic families are:

- Specifically designed for 3.3 V operation, NOT a re-characterized 5 V family
- Supply voltage 2.7 to 3.6 V for maximum speed applications
- CMOS minimum supply voltage of 1.2 V (1.0 V for LV) for battery-powered equipment
- Since they also function, at reduced speed (see Fig.4), with supply voltages down to as little as 1.2 V (2.7 V for LVT), they can also be used in equipment powered by a one or two cell battery
- Designed in accordance with the JEDEC LV standard (8.1) of 3.3 V ±0.3 V for ICs powered from a regulated supply

- With a 3.3 V ±0.3 V supply, inputs and outputs interface directly with TTL levels
- Latch-up free operation
- Excellent ESD protection
- Low ground-bounce
- Improved system reliability due to lower power dissipation and minimized gate oxide thermal breakdown voltage
- Lowered power consumption allows:
  - smaller, lighter batteries and longer battery life
  - higher PCB packing density
  - reduced power supply costs.

Features of the LV family

This low-voltage CMOS logic family is based on Philips' well-known HCMOS (HC) range and uses the same well-proven fabrication process with only slight modifications. It operates from a typical supply voltage of 3.3 V but can be used within the supply voltage range 1.0 V to 3.6 V. With a 3.3 V supply, the speed and performance are the same as HCMOS with a 5 V supply. The main usage areas are glue logic and battery-powered applications. To obtain the speed and output drive of HCMOS at the lower supply voltage, the channel length for LV is reduced to 2 μm, the gate oxide is thinner and the threshold voltages are lowered. Specific features of the LV family are:

- Process tuned for low-power applications with supply voltages between 1.0 V and 3.6 V
- Low power dissipation increases system reliability
- Fabricated in CMOS for intrinsic low power consumption - only a few nanoamps of supply current flow in the static state
- 2 μm technology allows typical propagation delay of 9 ns with a 3.3 V supply. Propagation delay is <18 ns with a 3.3 V supply
- Output drive at V_{CC} = 2 V is 6 mA (8 mA for driver outputs)
- With a 3.3 V supply, outputs can drive 130 Ω loads
- Speed at 3.3 V is virtually the same as that of HCMOS at 5 V
- Pin- and function-compatible with HCMOS ICs
- Faster than HCMOS at lower supply voltages
- Requires minimal qualification by the user because it is produced with a process almost identical to our established standard HCMOS process
- Identical high quality standards as for all Philips' HCMOS ICs.
- DIL packages and SO, SSOP and TSSOP packages for surface mounting.

Features of the LVC family

This advanced low-voltage logic family is compatible to FAST and its CMOS equivalent families with respect to pinning, speed and output drive capability. It is fabricated in full 0.6 μm CMOS technology and therefore dissipates much less power than FAST logic. It operates from a typical supply voltage of 3.3 V ±0.3 V but can be used within the supply voltage range 1.2 V to 3.6 V. Since LVC ICs also function, at reduced speed (see Fig.2), with supply voltages down to as little as 1.2 V, they can also be used in equipment powered by a single battery cell. A wide selection of types is available ranging from simple gates to multibyte functions for glue logic, battery-powered equipment and local bus applications. LVC is the backbone of Philips' low-voltage logic. Specific features of the family are:

- Output drive I_{OH}/I_{OL} = 24/24 mA
- Extensive output edge control with a patented circuit to reduce noise (low EMI)
- Outputs can drive 50 Ω loads
- Fabricated in CMOS for intrinsic low power consumption - only a few nanoamps of supply current flow in the static state
- Sub-micron (0.6 μm) technology allows short propagation delays
- The input voltage can exceed the supply voltage (up to 5.5 V), so LVC can be used for 5 V to 3 V, and 3 V to 5 V level shifting in mixed 3 V/5 V systems
- SO, SSOP and TSSOP packages for surface mounting.

Features of the HLL family

HLL comprises the world's fastest 3.3 V low-power CMOS logic ICs. They are fabricated in a sub-micron (0.6 μm) CMOS process with two-level metal and epitaxial substrates. HLL ICs with a 3.3 V ±0.3 V supply operate at twice the speed of FAST bipolar logic and, because they are CMOS ICs, they consume only a small fraction of the power. The family functions are mainly tailored for very high speed operation in the data-intensive bus interface area of mains-powered EDP equipment. Specific features of the HLL family are:

- Fabricated in CMOS for intrinsic low power consumption - only a few nanoamps of supply current flow in the static state
- High dynamic output drive allows transition times to be much shorter than the propagation delay
- Outputs can drive 50 Ω loads
- Sub-micron (0.6 μm) technology allows propagation delay of <4 ns with a 3.3 V supply - twice the speed of FAST with a 5 V supply
- Low-inductance, multiple centre power and ground pins for minimum noise and ground-bounce
- Low skew
- The input voltage can exceed the supply voltage (up to 5.5 V), so HLL can be used for 5 V to 3 V, and 3 V to 5 V level shifting in mixed 3 V/5 V systems
- Output edge-rate control circuitry for low noise generation (low EMI)
- SO, SSOP and TSSOP packages for surface mounting.

Table 2 KEY PARAMETERS AND FEATURES COMPARISON OF PHILIPS 3 V LOGIC FAMILIES

	LV	LVC	HLL	ALVC	LVT	LVT16
KEY PARAMETERS						
Nomenclature[1]	74LVxxxX	74LVCxxxX	74HL33xxxX	74ALVC16xxxX	74LVTxxxX	74LVT16xxxX
Minimum V_{CC} V	1.0	1.2	1.2	1.2	2.7	2.7
Maximum V_{CC} V	3.6	3.6	3.6	3.6	3.6	3.6
Output current mA	6/6	24/24	24/24	24/24	32/64	32/64
Quiescent current µA	80	20	80	40	80	80
'244 delay times						
T_{PD} typ. ns	9	4.0	2.1	2.1	2.4	2.4
T_{PD} max. ns	14	5.8	4.0	4.0	3.6	3.6
Max. ground bounce V	0.4	0.8	1.0	0.7	0.8	0.5
FEATURES						
Full CMOS	✓	✓	✓	✓		
Advanced BiCMOS					✓	✓
Drive capability:						
135 Ω	✓					
50 Ω		✓	✓	✓		
35 Ω					✓	✓
Feature size:						
2.0 µm	✓					
0.8 µm					✓	✓
0.6 µm		✓	✓	✓		
Corner supply pins	✓	✓			✓	
Centre supply pins			✓			
Multiple V_{CC}/GND pins				✓		✓
TTL level input	✓	✓	✓	✓	✓	✓
TTL level output	✓	✓	✓	✓	✓	✓
5 V input capability		✓[2]	✓[2]	✓[3]	✓	✓
Overvoltage protection					✓	✓
Live insertion					✓	✓
Input bus hold					✓	✓
Packages:						
DIL	✓					
SO	✓	✓	✓		✓	✓
SSOP	✓	✓	✓	✓	✓	✓
TSSOP	✓	✓	✓	✓	✓	✓
Application:						
glue logic	✓	✓				
battery-powered	✓	✓	✓	✓		
equipment		✓	✓	✓	✓	✓
local bus			✓	✓	✓	✓
super µP					✓	✓
backplane						
Compatible 5 V families	LS-TTL HC/HCT N74xx	FAST, ALS ACL (Q)FACT	FCT-C	FCT-C	ABT BC/BCT FCT-A	ABT BC/BCT FCT-C

[1] xxx = function indication, 245 etc
X = package code: D = SO, DB = SSOP II, PW = TSSOP I, DL=SSOP 48-56, DGG=TSSOP 48-56

[2] For transceiver I/O pins: $V_{IN\,max} = V_{CC} + 0.5$ V.

[3] For control pins only; other input and output pins: $V_{IN\,max} = V_{CC} + 0.5$ V.

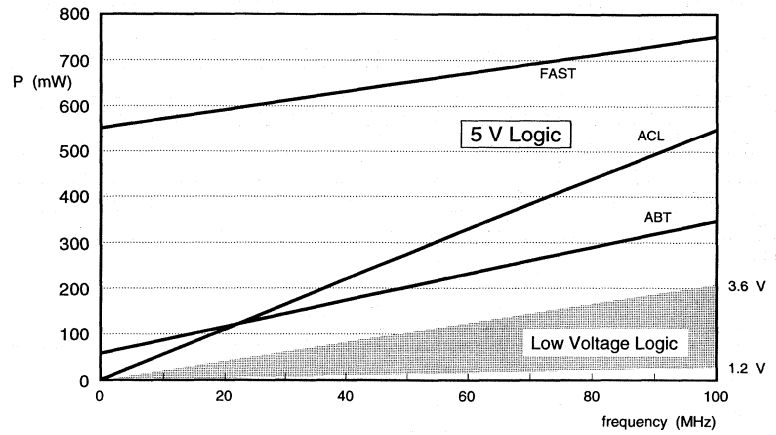


Fig.5 Comparison of power consumption versus speed for 3 V and 5 V logic octal transceivers

Features of the ALVC family

Produced according to the same design rules as HLL, this family is in essence the Multibyte version of HLL. Due to the multiple ground and V_{CC} pins groundbounce can be kept to a minimum and speed can be optimised.

These devices are available in the SSOP type III and TSSOP type II packages (48-56 pins).

The advantages of using multibyte functions are the board space savings and increased functionality leading to a lower chip count.

Features of the LVT family

This advanced 3.3 V BiCMOS logic family is fabricated in the 0.8 µm QUBiC process to give the best of CMOS combined with the best of bipolar. This assures extremely high output current combined with very high speed switching without compromise of power dissipation or noise levels. LVT operates from a typical supply voltage of 3.3 V ±0.3 V but can be used within the supply voltage range 2.7 V to 3.6 V. The main application areas for LVT ICs in EDP around 3.3 V processors, mainframes, workstations, telecom switchers and advanced backplanes where high output current and very high speed are vital. Specific features of the LVT family are:

- Output drive I_{OH}/I_{OL} = 32/64 mA
- Outputs can drive 35 Ω loads
- Advanced sub-micron (0.8 µm) QUBiC technology allows propagation delay of <4 ns with a 3.3 V supply
- Output overvoltage protection allows outputs to be forced to 5.5 V without any further interfacing needed. LVT is therefore fully compatible with 5 V TTL logic on both inputs and outputs without additional hardware
- Supports live insertion
- Bus hold capability to eliminate the need for pull-up/pull-down resistors on data and bus pins
- Split ground design and controlled output edge rates for reduced noise
- Optimized for backplane drive
- SO, SSOP type II and TSSOP type III packages for surface mounting.

Features of the LVT16 family

LVT16 is the Multibyte implementation of the LVT family having the same features except for the following:

- SSOP typ III and TSSOP type II packages for surface mount
- Multiple ground and V_{CC} pins for reduced groundbounce and fastest possible switching.
- The fastest 3 V family available

Comparison of the features of the new 3 v logic families

The features and key parameters of the six new families are compared in Table 2.

POSITIONING OF THE LOW-VOLTAGE FAMILIES WITH RESPECT TO OTHER LOGIC FAMILIES

Fig.5 is included here for clarification purposes only. Fig.5 shows power consumption as a function of speed for an octal transceiver from Philips' 3 V range compared with the same device from various 5 V logic families. Each output of the IC is loaded with 50 pF and the eight transceivers in the device are driven by a binary code.

With a 3 V supply, a low-voltage octal transceiver consumes up to 80% less power than similar 5 V logic devices. At lower supply voltages, the power savings are even greater.

QUALITY AND RELIABILITY OF PHILIPS' PRODUCTS

All Philips' products are of a high quality, constantly enhanced by a system of continuous quality improvement. We start to achieve our high level of quality during development of new devices by including staff from our Quality Department in the development teams. Testing includes life testing (including HAST) and thermal shock. We use sound methods of managing product reliability improvement to ensure that our products continue to perform to their specifications. Up-to-date quality reports are available to customers. Over the years, Philips has proved itself to be a quality supplier and our commitment to quality has been underlined by many awards including ISO9001/9002 awards for all Philips Semiconductor plants and TQE awards. Pairing innovation and high quality, Philips Semiconductors show they are 'Ready for Tomorrow'.

The LV family

These family specifications cover the common electrical ratings and characteristics of the entire LV 74LV/74LVU family, unless otherwise specified in the individual device datasheet.

This low-voltage CMOS logic family is based on Philips' well-known HCMOS (HC) range and uses the same well-proven fabrication process with only slight modifications. It operates from a typical supply voltage of 3.3 V but can be used within the supply voltage range 1.0 V to 3.6 V. With a 3.3 V supply , the speed and performance is the same as HCMOS with a 5 V supply.

RECOMMENDED OPERATING CONDITIONS FOR THE LV FAMILY

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	1.0	3.3	3.6	V	see note 1
V_I	input voltage	0	–	V_{CC}	V	
V_O	output voltage	0	–	V_{CC}	V	
T_{amb}	operating ambient temperature range in free air	–40 –40	– –	+85 +125	°C	see DC and AC characteristics per device
t_r, t_f	input rise and fall times except for Schmitt-trigger inputs	– – –	– – –	500 200 100	ns/V	V_{CC} = 1.0 V to 2.0 V V_{CC} = 2.0 V to 2.7 V V_{CC} = 2.7 V to 3.6 V

Notes: 1. The LV is guaranteed to function down to V_{CC} = 1.0 V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2 V to V_{CC} = 3.6 V.

ABSOLUTE MAXIMUM RATINGS FOR THE LV FAMILY

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	–0.5	+4.6	V	
$\pm I_{IK}$	DC input diode current	–	20	mA	$V_I < -0.5$ or $V_I > V_{CC}$ +0.5 V
$\pm I_{OK}$	DC output diode current	–	50	mA	$V_O < -0.5$ or $V_O > V_{CC}$ +0.5 V
$\pm I_O$	DC output source or sink current - standard outputs - bus driver outputs	– –	25 35	mA	–0.5 V < V_O < V_{CC} + 0.5 V
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with - standard outputs - bus driver outputs	– –	50 70	mA	
T_{stg}	storage temperature range	–65	+150	°C	
P_{tot}	power dissipation per package - plastic DIL - plastic mini-pack (SO) - plastic medium-shrink SO (SSOP)	 – – –	 750 500 500	 mW	for temperature range: –40 to +125 °C above + 70 °C derate linearly with 12 mW/K above + 70 °C derate linearly with 8 mW/K above + 70 °C derate linearly with 8 mW/K

Notes to the limiting values

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those under 'recommended operating conditions' is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS FOR THE LV FAMILY

Over recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS		
		−40 to +85			−40 to +125			V_{CC} (V)	V_I	OTHER
		MIN.	TYP.	MAX.	MIN.	MAX.				
V_{IH}	HIGH level input voltage	0.9 1.4 2.0	– – –	– – –	0.9 1.4 2.0	– – –	V	1.2 2.0 2.7 .. 3.6		
V_{IL}	LOW level input voltage	– – –	– – –	0.3 0.6 0.8	– – –	0.3 0.6 0.8	V	1.2 2.0 2.7 .. 3.6		
V_{OH}	HIGH level output voltage; all outputs	– 1.8 2.5 2.8	1.2 2.0 2.7 3.0	– – – –	– 1.8 2.5 2.8	– – – –	V	1.2 2.0 2.7 3.0	V_{IH} or V_{IL}	$-I_O$ = 100 µA
V_{OH}	HIGH level output voltage; STANDARD outputs	2.40	2.82	–	2.20	–	V	3.0	V_{IH} or V_{IL}	$-I_O$ = 6 mA
V_{OH}	HIGH level output voltage; BUS driver outputs	2.40	2.82	–	2.20	–	V	3.0	V_{IH} or V_{IL}	$-I_O$ = 8 mA
V_{OL}	LOW level output voltage; all outputs	– – – –	0 0 0 0	– 0.2 0.2 0.2	– – – –	– 0.2 0.2 0.2	V	1.2 2.0 2.7 3.0	V_{IH} or V_{IL}	I_O = 100 µA
V_{OL}	LOW level output voltage; STANDARD outputs	–	0.25	0.4	–	0.5	V	3.0	V_{IH} or V_{IL}	I_O = 6 mA
V_{OL}	LOW level output voltage; BUS driver outputs	–	0.20	0.4	–	0.5	V	3.0	V_{IH} or V_{IL}	I_O = 8 mA
I_I	input leakage current	–	–	1.0	–	1.0	µA	3.6	V_{CC} or GND	
I_{OZ}	3-state output OFF-state current	–	–	5.0	–	10.0	µA	3.6	V_{IH} or V_{IL}	V_O = V_{CC} or GND
I_{CC}	quiescent supply current; SSI flip-flops MSI LSI	 – – – –	 – – – –	 20.0 20.0 20.0 500	 – – – –	 40.0 80.0 160.0 1000	µA	3.6	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current per input	–	–	500	–	850	µA	2.7 .. 3.6	V_I = V_{CC} − 0.6 V	

Note: All typical values are measured at T_{amb} = 25 °C.

FAMILY DESCRIPTION

The LVC family comprises very fast low-power logic ICs fabricated in a sub-micron CMOS process.
LVC ICs with 3.3 V ±0.3 V supply operate at the same speed as FAST bipolar logic and consumes only a fraction of the power. The LVC family functions with supply voltages down to 2.7 V. The reduction from the conventional 5.0 V to 3.3 V reduces the output swing leading to a much lower dynamic power dissipation. Pin and function compatibility with FAST ensures an easy transfer of existing systems into new 3.3 V systems.

RECOMMENDED OPERATING CONDITIONS FOR THE LVC FAMILY

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage (for max. speed performance)	2.7	3.6	V	
V_{CC}	DC supply voltage (for low-voltage applications)	1.2	3.6	V	
V_I	DC input voltage range	0	5.5	V	
$V_{I/O}$	DC input voltage range for I/Os	0	V_{CC}	V	
V_O	DC output voltage range	0	V_{CC}	V	
T_{amb}	operating ambient temperature range in free air	−40	+85	°C	see DC and AC characteristics per device
t_r, t_f	input rise and fall times	0 0	20 10	ns/V	V_{CC} = 1.2 to 2.7 V V_{CC} = 2.7 to 3.6 V

LIMITING VALUES FOR THE LVC FAMILY (Note 1)

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+4.6	V	
I_{IK}	DC input diode current	–	−50	mA	$V_I < 0$
V_I	DC input voltage	−0.5	+5.5	V	note 2
$V_{I/O}$	DC input voltage range for I/Os	−0.5	V_{CC} + 0.5	V	
I_{OK}	DC output diode current	–	±50	mA	$V_O > V_{CC}$ or $V_O < 0$
V_O	DC output voltage	−0.5	V_{CC} + 0.5	V	note 2
I_O	DC output source or sink current	–	±50	mA	V_O = 0 to V_{CC}
I_{GND}, I_{CC}	DC V_{CC} or GND current	–	±100	mA	
T_{stg}	storage temperature range	−60	+150	°C	
P_{tot}	power dissipation per package				See page 1 – 20

Notes to the limiting values

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those under 'recommended operating conditions' is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS FOR THE LVC FAMILY

Over recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C) −40 to +85			UNIT	TEST CONDITIONS		
		MIN.	TYP.	MAX.		V_{CC} (V)	V_I	OTHER
V_{IH}	HIGH level input voltage	V_{CC} 2.0	– –	– –	V	1.2 2.7 to 3.6		
V_{IL}	LOW level input voltage	– –	– –	GND 0.8	V	1.2 2.7 to 3.6		
V_{OH}	HIGH level output voltage	V_{CC} − 0.5 V_{CC} − 0.2 V_{CC} − 0.6 V_{CC} − 1.0	– V_{CC} – –	– – – –	V	2.7 3.0 3.0 3.0	V_{IH} or V_{IL}	I_O = −12 mA I_O = −100 µA I_O = −12 mA I_O = −24 mA
V_{OL}	LOW level output voltage	– – –	– – –	0.40 0.20 0.55	V	2.7 3.0 3.0	V_{IH} or V_{IL}	I_O = 12 mA I_O = 100 µA I_O = 24 mA
I_I	input leakage current	–	±0.1	±5	µA	3.6	5.5 V or GND	not for I/O pins
I_{IHZ}/I_{ILZ}	input current for common I/O pins	–	±0.1	±15	µA	3.6	V_{CC} or GND	
I_{OZ}	3-state output OFF-state current	–	0.1	±10	µA	3.6	V_{IH} or V_{IL}	V_O = V_{CC} or GND
I_{CC}	quiescent supply current	–	0.1	20	µA	3.6	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current given per input pin	–	5	500	µA	2.7 to 3.6	V_{CC} − 0.6 V	I_O = 0

Note: All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

FAMILY DESCRIPTION

The HLL family comprises extremely fast low-power logic ICs fabricated in a sub-micron CMOS process with two-level metal and epitaxial substrates. HLL ICs with 3.3 V ±0.3 V supply operates at twice the speed of FAST bipolar logic and consumes only a fraction of the power. The HLL functions with supply voltages down to 1.2 V. The reduction from the conventional 5.0 V to 3.3 V reduces the output swing dramatically and this with the low-inductance multiple centre power and ground pins significantly reduces noise and ground bounce that would otherwise occur for signals with this very high speed.

RECOMMENDED OPERATING CONDITIONS FOR THE HLL FAMILY

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage (for max. speed performance)	3.0	3.6	V	
V_{CC}	DC supply voltage (for low-voltage applications)	1.2	3.6	V	
V_I	DC input voltage range	0	5.5	V	
$V_{I/O}$	DC input voltage range for I/Os	0	V_{CC}	V	
V_O	DC output voltage range	0	V_{CC}	V	
T_{amb}	operating ambient temperature range in free air	−40	+85	°C	see DC and AC characteristics per device
t_r, t_f	input rise and fall times	– –	20 50	ns ns	V_{CC} = 3.6 V V_{CC} = 1.2 V

LIMITING VALUES FOR THE HLL FAMILY

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+4.6	V	
I_{IK}	DC input diode current	–	−50	mA	$V_I < 0$
V_I	DC input voltage	−0.5	+5.5	V	note 2
$V_{I/O}$	DC input voltage range for I/Os	−0.5	V_{CC} + 0.5	V	
I_{OK}	DC output diode current	–	±75	mA	$V_O > V_{CC}$ or $V_O < 0$
V_O	DC output voltage	−0.5	V_{CC} + 0.5	V	note 2
I_O	DC output source or sink current	–	±70	mA	V_O = 0 to V_{CC}
I_{GND}, I_{CC}	DC V_{CC} or GND current	–	+100	mA	
T_{stg}	storage temperature range	−60	+150	°C	
P_{tot}	power dissipation per package	–			See page 1 – 20

Notes to the limiting values

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those under 'recommended operating conditions' is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS FOR THE HLL FAMILY

Over recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS		
		+25			−40 to +85			V_{CC} (V)	V_I	OTHER
		MIN.	TYP.	MAX.	MIN.	MAX.				
V_{IH}	HIGH level input voltage	–	–	–	2.0	–	V	3.6		
V_{IL}	LOW level input voltage	–	–	–	–	0.8	V	3.0		
V_H	hysteresis (all inputs)	–	0.25	–	–	–	V	3.0 to 3.6		
V_{OH}	HIGH level output voltage	V_{CC} − 0.2 V_{CC} − 0.4	V_{CC} –	– –	V_{CC} − 0.2 V_{CC} − 0.4	– –	V	3.0	V_{IH} or V_{IL}	I_O = −100 µA I_O = −24 mA
V_{OL}	LOW level output voltage	– –	– –	0.2 0.4	– –	0.2 0.4	V	3.0	V_{IH} or V_{IL}	I_O = 100 µA I_O = 24 mA
I_I	input leakage current	–	–	–	–	±5	µA	3.6	V_{CC} or GND	
I_{OZ}	3-state output OFF-state current	–	–	–	–	10	µA	3.6	V_{IH} or V_{IL}	V_O = V_{CC} or GND
I_{CC}	quiescent supply current	–	–	8.0	–	80	µA	3.6	V_{CC} or GND	I_O = 0

FAMILY DESCRIPTION

The ALVC family comprises very fast low-power logic ICs fabricated in a sub-micron CMOS process. The ALVC family functions with supply voltages down to 1.2 V.

Active bushold circuitry is provided on all data inputs to hold floating inputs at a valid logical level. This feature eliminates the need for external pull-up/pull-down resistors.

ALVC combines very high speeds and high output drive with very low power consumption.

RECOMMENDED OPERATING CONDITIONS FOR THE ALVC FAMILY

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage (for max. speed performance)	2.7	3.6	V	
V_{CC}	DC supply voltage (for low-voltage applications)	1.2	3.6	V	
V_I	DC input voltage range	0	V_{CC}	V	data inputs only
V_I	DC input voltage range	0	5.5	V	control pins only
V_O	DC output voltage range	0	V_{CC}	V	
T_{amb}	operating ambient temperature range in free air	−40	+85	°C	
t_r, t_f	input rise and fall times	0 0	20 10	ns/V	V_{CC} = 2.7 to 3.0 V V_{CC} = 3.0 to 3.6 V

LIMITING VALUES FOR THE ALVC FAMILY

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+4.6	V	
I_{IK}	DC input diode current	–	−50	mA	$V_I < 0$
V_I	DC input voltage	−0.5	5.5	V	for control pins only; note 2
V_I	DC input voltage	−0.5	V_{CC} + 0.5	V	for data inputs only; note 2
I_{OK}	DC output diode current	–	±50	mA	$V_O > V_{CC}$ or $V_O < 0$
V_O	DC output voltage	−0.5	V_{CC} + 0.5	V	note 2
I_O	DC output source or sink current	–	±50	mA	V_O = 0 to V_{CC}
I_{GND}, I_{CC}	DC V_{CC} or GND current	–	±100	mA	
T_{stg}	storage temperature range	−60	+150	°C	
P_{tot}	power dissipation per package				Se page 1 – 20

Notes to the limiting values

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operating of the device at these or any other conditions beyond those under 'recommended operating conditions' is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS FOR THE ALVC FAMILY

Over recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C) −40 to +85			UNIT	TEST CONDITIONS		
		MIN.	TYP.[1]	MAX.		V_{CC} (V)	V_I	OTHER
V_{IH}	HIGH level input voltage	V_{CC} 2.0	– –	– –	V	1.2 2.7 to 3.6		
V_{IL}	LOW level input voltage	– –	– –	GND 0.8	V	1.2 2.7 to 3.6		
V_{OH}	HIGH level output voltage	V_{CC} − 0.5 V_{CC} − 0.2 V_{CC} − 1.0	– V_{CC} –	– – –	V	2.7 3.0 3.0	V_{IH} or V_{IL}	I_O = −12 mA I_O = −100 µA I_O = −24 mA
V_{OL}	LOW level output voltage	– – –	– – –	0.40 0.20 0.55	V	2.7 3.0 3.0	V_{IH} or V_{IL}	I_O = 12 mA I_O = 100 µA I_O = 24 mA
I_I	input leakage current	–	±0.1	±5	µA	3.6	5.5V or GND	for control pins only
I_I	input leakage current	–	±0.1	±5	µA	3.6	V_{CC} or GND	for data inputs only
I_{IHZ}/I_{ILZ}	input current for common I/O pins	–	±0.1	±15	µA	3.6	V_{CC} or GND	
I_{OZ}	3-state output OFF-state current	–	0.1	±10	µA	3.6	V_{IH} or V_{IL}	V_O = V_{CC} or GND
I_{CC}	quiescent supply current	–	0.2	40	µA	3.6	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current given per control pin	–	5	500	µA	2.7 to 3.6	V_{CC} − 0.6 V	I_O = 0
ΔI_{CC}	additional quiescent supply current given per data i/o pin	–	150	750	µA	2.7 to 3.6	V_{CC} − 0.6 V	I_O = 0
IBHL	bushold LOW sustaining current	75	–	–	µA	3.0	0.8 V	For data inputs only[2]
IBHH	bushold HIGH sustaining current	−75	–	–	µA	3.0	2.0 V	
IBHLO	bushold LOW overdrive current	450	–	–	µA	3.6		
IBHHO	bushold HIGH overdrive current	−450	–	–	µA	3.6		

Notes:

1) All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

2) Control inputs do not have a bushold circuit.

FAMILY DESCRIPTION

The LVT family comprises very fast low-power logic ICs fabricated in an advanced sub-micron BiCMOS process.
LVT ICs at a supply voltage of 3.3 V operate at the same speed as ABT BiCMOS logic at V_{CC} = 5V and they consume considerably less power.
The LVT family functions down to V_{CC} = 2.7 V for application in unregulated systems and provides a number of extra features not found in other logic families.

The reduction from the standard 5.0 V to 3.3 V reduces the output swing, leading to a much lower dynamic power dissipation. Pin and function compatibility with ABT ensure an easy transfer of existing systems into new 3.3 V systems.

RECOMMENDED OPERATING CONDITIONS FOR THE LVT FAMILY

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	DC input voltage	0	5.5	V
V_{IH}	High level input voltage	2.0		V
V_{IL}	Low level input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%, f ≥ 1 kHz		64	
$\Delta t/\Delta V$	Input transition rise or fall rate, outputs enabled		10	ns/V
T_{amb}	operating ambient temperature range in free air	–40	+85	°C

LIMITING VALUES FOR THE LVT FAMILY (Notes 1 and 2)

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC supply voltage		–0.5	+4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–	–50	mA
V_I	DC input voltage	note 3	–0.5	7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–	–50	mA
V_O	DC output voltage	Output in High or Off state; note 3	–0.5	7.0	V
I_O	DC output source or sink current	Output in Low state Output in High state		128 –64	mA
T_{stg}	storage temperature range		–65	+150	°C

Notes to the limiting values

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under 'recommended operating conditions' is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. The temperature capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

DC CHARACTERISTICS FOR THE LVT FAMILY

Over recommended operating conditions

Voltages are referenced to GND (ground=0 V)

SYMBOL	PARAMETER		TEST CONDITIONS	T_{amb} (°C) −40 to +85			UNIT
				MIN.	TYP.[1]	MAX.	
V_{IK}	Input clamping voltage		V_{CC}=2.7V; I_{IK}=−18 mA	–	–	−1.2	V
V_{OH}	HIGH level output voltage		V_{CC}=2.7 to 3.6V; I_{OH}=−100 µA V_{CC}=2.7V; I_{OH}=−8 mA V_{CC}=3.0V; I_{OH}=−32 mA	V_{CC}−0.2 2.4 2.0	– – –	– – –	V
V_{OL}	LOW level output voltage		V_{CC}=2.7V; I_{OL}=100 µA V_{CC}=2.7V; I_{OL}=24 mA V_{CC}=3.0V; I_{OL}=16mA V_{CC}=3.0V; I_{OL}=32mA V_{CC}=3.0V; I_{OL}=64mA	– – – – –	– – – – –	0.2 0.5 0.4 0.5 0.55	V
I_{RST}	Power-up output low voltage[5]		V_{CC}=3.6V; I_O=1mA; V_I GND or V_{CC}	–	–	0.55	V
I_I	Input leakage current	All pins	V_{CC}=0 or 3.6V; V_I=5.5V	–	–	10	µA
		Control pins	V_{CC}=3.6V; V_I=V_{CC} or GND	–	–	±1	
		I/O pins[4]	V_{CC}=3.6V; V_I=V_{CC}	–	–	10	
		I/O pins[4]	V_{CC}=3.6V; V_I=5.5V	–	–	20	
		Data pins[4]	V_{CC}=3.6V; V_I=V_{CC}	–	–	1	
		Data pins[4]	V_{CC}=3.6V; V_I=0	–	–	−5	
I_{OFF}	Output off current		V_{CC}=0V; V_I or V_O=0 to 4.5V	–	–	±100	µA
I_{HOLD}	Bus hold current A or B outputs		V_{CC}=3.0V; V_I=0.8V	75	–	–	µA
			V_{CC}=3.0V; V_I=2.0V	-75	–	–	µA
I_{EX}	Current into an output in the High state when V_O>V_{CC}		V_{CC}=3.0V; V_O=5.5 V	–	–	125	µA
I_{CCH}	quiescent supply current		V_{CC}=3.6V, Outputs High, V_I=V_{CC} or GND; I_O=0	–	0.13	0.19	mA
I_{CCL}			V_{CC}=3.6V, Outputs Low, V_I=V_{CC} or GND; I_O=0	–	3	12	
I_{CCZ}			V_{CC}=3.6V, Outputs disabled, V_I=V_{CC} or GND; I_O=0	–	0.13	0.19	
ΔI_{CC}	additional supply current per input pin[2]		V_{CC}=3.0 to 3.6V; one input at V_{CC}-0.6; other inputs at V_{CC} or GND	–		200	µA
$I_{PU/PD}$	Power-up/down 3-state output current[3]		V_{CC}≤1.2 V; V_O=0.5V to V_{CC}; V_I=GND or V_{CC}; OE/$\overline{OE}$=Don't care	–	–	±100	µA
C_I	Input capacitance		V_I=0 or 3V	–	4	–	
C_O	Output capacitance		V_I=0 or 3V	–	10	–	

Notes:

1. All typical values are at V_{CC} = 3.3 V and Tamb = 25 °C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2 V with a transition time of up to 10ms. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µs is permitted. This parameter is valid at T_{amb} = 25 °C.
4. Unused pins at V_{CC} or GND
5. This applies to parts with storage cells. For valid results, data must not be loaded in the flip-flops (or latches) after applying the power.

FAMILY DESCRIPTION

The LVT16 family comprises very fast low-power logic ICs fabricated in an advanced sub-micron BiCMOS process.
LVT16 ICs at a supply voltage of 3.3 V operate at the same speed as ABT BiCMOS logic at V_{CC} = 5V and they consume considerably less power.
The LVT16 family functions down to V_{CC} = 2.7 V for application in unregulated systems and provides a number of extra features not found in other logic families.
The reduction from the standard 5.0 V to 3.3 V reduces the output swing, leading to a much lower dynamic power dissipation. Pin and function compatibility with ABT16 ensure an easy transfer of existing systems into new 3.3 V systems.

RECOMMENDED OPERATING CONDITIONS FOR THE LVT16 FAMILY

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	DC input voltage	0	5.5	V
V_{IH}	High level input voltage	2.0		V
V_{IL}	Low level input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%, f ≥ 1 kHz		64	
$\Delta t/\Delta V$	Input transition rise or fall rate, outputs enabled		10	ns/V
T_{amb}	operating ambient temperature range in free air	–40	+85	°C

LIMITING VALUES FOR THE LVT16 FAMILY (Notes 1 and 2)

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC supply voltage		–0.5	+4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–	–50	mA
V_I	DC input voltage	note 3	–0.5	7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–	–50	mA
V_O	DC output voltage	Output in High or Off state; note 3	–0.5	7.0	V
I_O	DC output source or sink current	Output in Low state Output in High state		128 –64	mA
T_{stg}	storage temperature range		–65	+150	°C

Notes to the limiting values

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under 'recommended operating conditions' is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. The temperature capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

DC CHARACTERISTICS FOR THE LVT16 FAMILY

Over recommended operating conditions

Voltages are referenced to GND (ground=0 V)

SYMBOL	PARAMETER		TEST CONDITIONS	T_{amb} (°C) –40 to +85			UNIT
				MIN.	TYP.[1]	MAX.	
V_{IK}	Input clamping voltage		V_{CC}=2.7V; I_{IK}=–18 mA	–	–	–1.2	V
V_{OH}	HIGH level output voltage		V_{CC}=2.7 to 3.6V; I_{OH}=–100 µA V_{CC}=2.7V; I_{OH}=–8 mA V_{CC}=3.0V; I_{OH}=–32 mA	V_{CC}–0.2 2.4 2.0	– – –	– – –	V
V_{OL}	LOW level output voltage		V_{CC}=2.7V; I_{OL}=100 µA V_{CC}=2.7V; I_{OL}=24 mA V_{CC}=3.0V; I_{OL}=16mA V_{CC}=3.0V; I_{OL}=32mA V_{CC}=3.0V; I_{OL}=64mA	– – – – –	– – – – –	0.2 0.5 0.4 0.5 0.55	V
I_{RST}	Power-up output low voltage[5]		V_{CC}=3.6V; I_O=1mA; V_I GND or V_{CC}	–	–	0.55	V
I_I	Input leakage current	All pins	V_{CC}=0 or 3.6V; V_I=5.5V	–	–	10	µA
		Control pins	V_{CC}=3.6V; V_I=V_{CC} or GND	–	–	±1	
		I/O pins[4]	V_{CC}=3.6V; V_I=V_{CC}	–	–	10	
		I/O pins[4]	V_{CC}=3.6V; V_I=5.5V	–	–	20	
		Data pins[4]	V_{CC}=3.6V; V_I=V_{CC}	–	–	1	
		Data pins[4]	V_{CC}=3.6V; V_I=0	–	–	–5	
I_{OFF}	Output off current		V_{CC}=0V; V_I or V_O=0 to 4.5V	–	–	±100	µA
I_{HOLD}	Bus hold current A or B outputs		V_{CC}=3.0V; V_I=0.8V	75	–	–	µA
			V_{CC}=3.0V; V_I=2.0V	-75	–	–	µA
I_{EX}	Current into an output in the High state when V_O>V_{CC}		V_{CC}=3.0V; V_O=5.5 V	–	–	125	µA
I_{CCH}	quiescent supply current		V_{CC}=3.6V, Outputs High, V_I=V_{CC} or GND; I_O=0	–	–	0.12	mA
I_{CCL}			V_{CC}=3.6V, Outputs Low, V_I=V_{CC} or GND; I_O=0	–	–	6	
I_{CCZ}			V_{CC}=3.6V, Outputs disabled, V_I=V_{CC} or GND; I_O=0	–	–	0.12	
ΔI_{CC}	additional supply current per input pin[2]		V_{CC}=3.0 to 3.6V; one input at V_{CC}-0.6; other inputs at V_{CC} or GND	–		200	µA
$I_{PU/PD}$	Power-up/down 3-state output current[3]		V_{CC}≤1.2 V; V_O=0.5V to V_{CC}; V_I=GND or V_{CC}; OE/OE=Don't care	–	–	±100	µA
C_I	Input capacitance		V_I=0 or 3V	–	4	–	
C_O	Output capacitance		V_I=0 or 3V	–	10	–	

Notes:

1. All typical values are at V_{CC} = 3.3 V and Tamb = 25 °C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2 V with a transition time of up to 10ms. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µs is permitted. This parameter is valid at T_{amb} = 25 °C.
4. Unused pins at V_{CC} or GND
5. This applies to parts with storage cells. For valid results, data must not be loaded in the flip-flops (or latches) after applying the power.

Package thermal data

THERMAL DATA OF DIL, SO, SSOP AND TSSOP PACKAGES

The table below specifies both P_{TOT}, the maximum power dissipation at an ambient temperature of T = 55 °C. Above this temperature the dissipation should be limited according to the derating factor Df.

Pincount		14	16	20	24	28	48	56	Unit
DIL	Ptot	825	900	1200	1300	1400			mW
	Df	11	12	16	17.5	19			mW/K
SO	Ptot	400	450	0	0	0			mW
	Df	5.25	6.50	0.00	0.00	0.00			mW/K
SOL	Ptot	0	750	900	950	950			mW/K
	Df	0	10	12	12.67	12.67			mW
SSOP	Ptot	400	400	500	500	500	850	1000	mW
	Df	5.33	5.33	6.67	6.67	6.67	11.33	13.33	mW/K
TSSOP	Ptot	400	400	500	500	500	600	700	mW
	Df	5.33	5.33	6.67	6.67	6.67	8	9.33	mW/K

P_{tot} = maximum power dissipation per package
Df = derating factor above T = 55 °C

Currents

Positive current is defined as conventional current flow into a device.
Negative current is defined as conventional current flow out of a device.

IBHL	Bushold LOW sustaining current holding the input below the specified V_I level
IBHH	Bushold HIGH sustaining current holding the input below the specified V_I level
IBHLO	Bushold LOW overdrive current forcing the data input to the opposite logic input state
IBHHO	Bushold HIGH overdrive current forcing the data input to the opposite logic input state
I_{CC}	Quiescent power supply current; the current flowing into the V_{CC} supply terminal.
ΔI_{CC}	Additional quiescent supply current per input pin at a specified input voltage and V_{CC}.
I_{EX}	Current into an output in the high state when the voltage on the output is forced to exceed the supply voltage.
I_{GND}	Quiescent power supply current; the current flowing into the GND terminal.
I_{HOLD}	A holding current provided to latch the last known input state to a valid logic level.
I_I	Input leakage current; the current flowing into a device at a specified input voltage and V_{CC}.
I_{IK}	Input diode current; the current flowing into a device at a specified input voltage.
I_O	Output source or sink current; the current flowing into a device at a specified output voltage.
I_{OFF}	Off-state output current: the leakage current flowing into the output of a 3-state device in the off-state, when the output is connected to V_{CC} or GND.
I_{OK}	Output diode current; the current flowing into a device at a specified output voltage.
I_{OZ}	OFF-state output current: the leakage current flowing into the output of a 3-state device in the OFF-state, when the output is connected to V_{CC} or GND.
$I_{PU/PD}$	Current flowing into/out of an output while device is powered up/down (live insertion/extraction).
I_S	Analog switch leakage current; the current flowing into an analog switch at a specified voltage across the switch and V_{CC}.

Voltages

All voltages are referenced to GND (ground), which is typically 0 V.

GND	Supply voltage; for a device with a single negative power supply, the most negative power supply, used as the reference level for other voltages; typically ground.
V_{CC}	Supply voltage; the most positive potential on the device.
V_{EE}	Supply voltage; the one of two (GND and V_{EE}) negative power supplies.
V_H	Hysteresis voltage; difference between the trigger levels, when applying a positive and negative-going input signal.
V_I	DC input voltage
$V_{I/O}$	DC input voltage for I/Os
V_{IH}	HIGH level input voltage; the range of input voltages that represents a logic HIGH level in the system.
V_{IL}	LOW level input voltage; the range of input voltages that represents a logic LOW level in the system.
V_{OH}	HIGH level output voltage; the range of voltages at an output terminal with a specified output loading and supply voltage. Device inputs are conditioned to establish a HIGH level at the output.
V_{OL}	LOW level output voltage; the range of voltages at an output terminal with a specified output loading and supply voltage. Device inputs are conditioned to establish a LOW level at the output.
V_{RST}	Power-up output voltage; storage cells are reset to the low-state upon power-up
V_{T+}	Trigger threshold voltage; positive-going signal.
V_{T-}	Trigger threshold voltage; negative going signal.

Analog terms

R_{ON}	ON-resistance; the effective ON-state resistance of an analog switch, at a specified voltage across the switch and output load.
ΔR_{ON}	ΔON-resistance; the difference in ON-resistance between any two switches of an analog device at a specified voltage across the switch and output load.

Capacitances

C_I	Input capacitance; the capacitance measured at a terminal connected to an input of a device.
$C_{I/O}$	Input/Output capacitance; the capacitance measured at a terminal connected to an I/O-pin (e.g. a transceiver).
C_O	Output capacitance; the capacitance measured at a terminal connected to a 3-state output.
C_L	Output load capacitance; the capacitance connected to an output terminal including jig and probe capacitance.
C_{PD}	Power dissipation capacitance; the capacitance used to determine the dynamic power dissipation per logic function, when no extra load is provided to the device.
C_S	Switch capacitance; the capacitance of a terminal to a switch of an analog device.

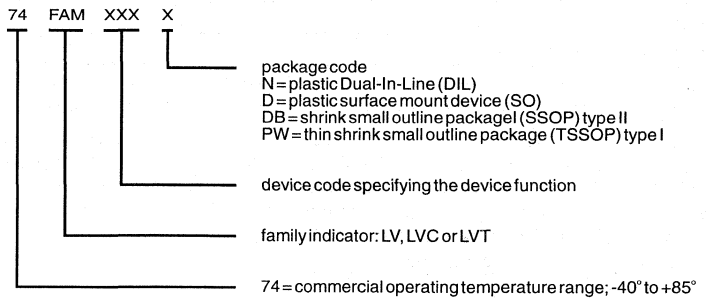
AC switching parameters

f_i	Input frequency; for combinatorial logic devices the maximum number of inputs and outputs switching in accordance with the device function table. For sequential logic devices the clock frequency using alternate HIGH and LOW for data input or using the toggle mode, whichever is applicable.
f_o	Output frequency; each output.
f_{max}	Maximum clock frequency; clock input waveforms should have a 50% duty factor and be such as to cause the outputs to be switching from 10%V_{CC} to 90%V_{CC} in accordance with the device function table.
t_h	Hold time; the interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure their continued recognition. A negative hold time indicates that the correct logic level may be released prior to the timing pulse and still be recognized.
t_r, t_f	Clock input rise and fall times; 10% and 90% values.
t_{PHL}	Propagation delay; the time between the specified reference points, normally the 50% points for logic devices on the input and output waveforms, with the output changing from the defined HIGH level to the defined LOW level.
t_{PLH}	Propagation delay; the time between the specified reference points, normally the 50% points for logic devices on the input and output waveforms, with the output changing from the defined LOW level to the defined HIGH level.
t_{PHZ}	3-state output disable time; the time between the specified reference points, normally the 50% points for the logic devices on the output enable input voltage waveform and a point representing 10% of the output swing on the output voltage waveform of a 3-state device, with the output changing from a HIGH level (V_{OH}) to a high impedance OFF-state (Z).
t_{PLZ}	3-state output disable time; the time between the specified reference points, normally the 50% points for the logic devices on the output enable input voltage waveform and a point representing 10% of the output swing on the output voltage waveform of a 3-state device, with the output changing from a LOW level (V_{OL}) to a high impedance OFF-state (Z).
t_{PZH}	3-state output enable time; the time between the specified reference points, normally the 50% points for the logic devices on the output enable input voltage waveform and the 50% point on the output voltage waveform of a 3-state device, with the output changing from a high impedance OFF-state (Z) to a HIGH level (V_{OH}).
t_{PZL}	3-state output enable time; the time between the specified reference points, normally the 50% points for the logic devices on the output enable input voltage waveform and the 50% point on the output voltage waveform of a 3-state device, with the output changing from a high impedance OFF-state (Z) to a LOW level (V_{OL}).
t_{rem}	Removal time; the time between the end of an overriding asynchronous input, typically a clear or reset input, and the earliest permissible beginning of a synchronous control input, typically a clock input, normally measured at the 50% points for logic devices on both input voltage waveforms.
t_s/t_{su}	Set-up time; the interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure their recognition. A negative set-up time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.
t_{THL}	Output transition time; the time between two specified reference points on a waveform, normally 90% and 10% points, that is changing from HIGH-to-LOW.
t_{TLH}	Output transition time; the time between two specified reference points on a waveform, normally 10% and 90% points, that is changing from LOW-to-HIGH.
t_W	Pulse width; the time between the 50% amplitude points on the leading and trailing edges of a pulse for the logic family devices

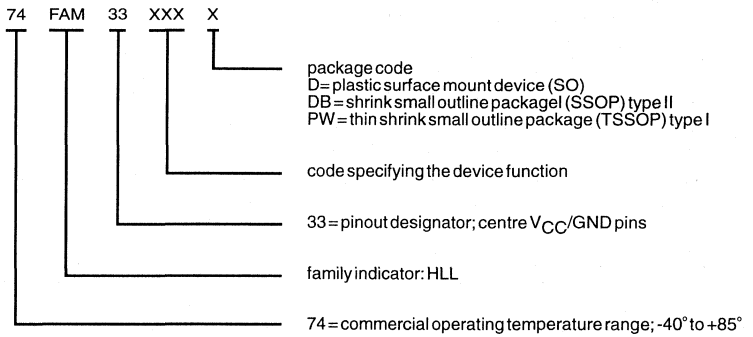
Ordering Information

TYPE NUMBER DESIGNATIONS

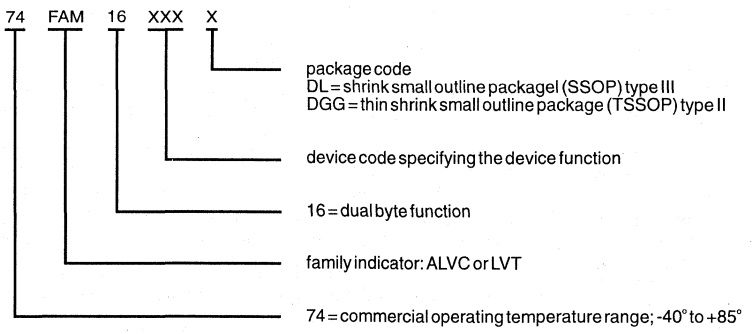
LV, LVC and LVT FAMILIES



HLL FAMILY



ALVC and LVT16 MULTIBYTE FAMILIES



Definition of data sheet status

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operating of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

The following persons were
indispensable for their suport,
committment and dedication:
Julie Abbot
Carin Habraken
Celia Tippit
and Tom Tieben.

Thanks a lot!

Tinus van de Wouw/Albert Beijer

August 1994

DEVICE DATA

LV

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Output capability: standard**
- **I_{CC} category: SSI**

DESCRIPTION

The 74LV00 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT00.

The 74LV00 provides the 2-input NAND function.

FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF V_{CC} = 3.3 V	7	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	22	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV00N	14	DIL	plastic	DIL14/SOT27
74LV00D	14	SO	plastic	SO14/SOT108A
74LV00DB	14	SSOP	plastic	SSOP14/SOT337
74LV00PW	14	TSSOP	plastic	TSSOP14/SOT402

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

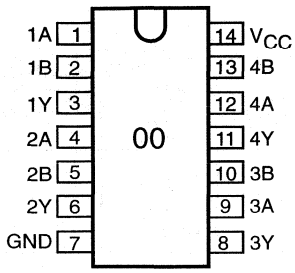


Fig.1 Pin configuration.

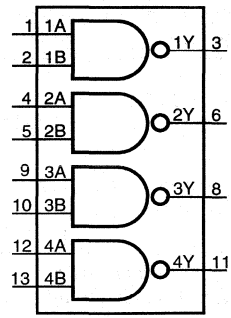


Fig.2 Logic symbol.

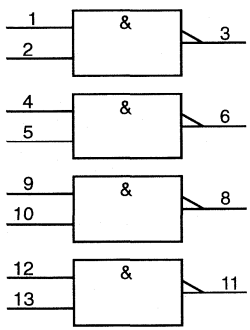


Fig.3 IEC Logic symbol.

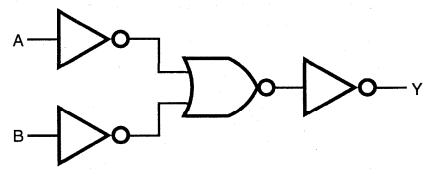


Fig.4 Logic diagram (one gate).

DC CHARACTERISTICS FOR 74LV00

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74LV00

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	–	45	–	–	–	ns	1.2	Fig.5
		–	15	31	–	36		2.0	
		–	11	23	–	26		2.7	
		–	9*	18	–	21		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

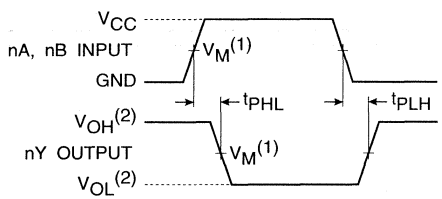


Fig. 5 Waveforms showing the input (nA, nB) to output (nY) propagation delays.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Output capability: standard**
- **I_{CC} category: SSI**

DESCRIPTION

The 74LV02 a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT02.

The 74LV02 provides the 2-input NOR function.

FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	H
L	H	L
H	L	L
H	H	L

H = HIGH voltage level
L = LOW voltage level

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF V_{CC} = 3.3 V	7	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	22	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV02N	14	DIL	plastic	DIL14/SOT27
74LV02D	14	SO	plastic	SO14/SOT108A
74LV02DB	14	SSOP	plastic	SSOP14/SOT337
74LV02PW	14	TSSOP	plastic	TSSOP14/SOT402

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	1Y to 4Y	data outputs
2, 5, 8, 11	1A to 4A	data inputs
3, 6, 9, 12	1B to 4B	data inputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

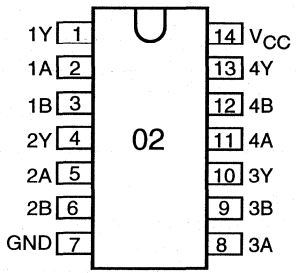


Fig.1 Pin configuration.

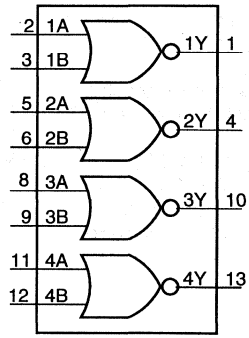


Fig.2 Logic symbol.

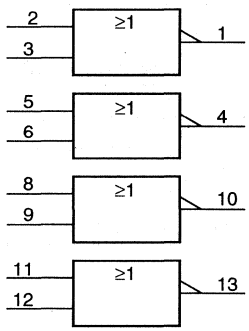


Fig.3 IEC Logic symbol.

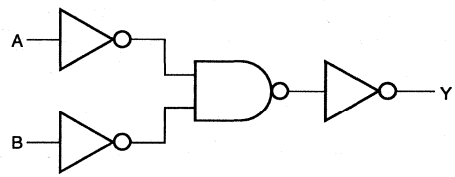


Fig.4 Logic diagram (one gate).

DC CHARACTERISTICS FOR 74LV02

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74LV02

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	–	45	–	–	–	ns	1.2	Fig. 5
		–	15	31	–	36		2.0	
		–	11	23	–	26		2.7	
		–	9*	18	–	21		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

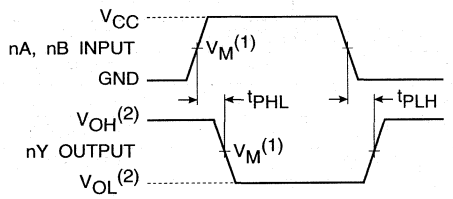


Fig. 5 Waveforms showing the input (nA, nB) to output (nY) propagation delays.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Level shifter capability**
- **Output capability: standard (open drain)**
- **I_{CC} category: SSI**

DESCRIPTION

The 74LV03 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT03.

The 74LV03 provides the 2-input NAND function.

The 74LV03 has open-drain N-transistor outputs, which are not clamped by a diode connected to V_{CC}. In the OFF-state, i.e. when one input is LOW, the output may be pulled to any voltage between GND and V_{Omax}. This allows the device to be used as a LOW-to-HIGH or HIGH-to-LOW level shifter. For digital operation and OR-tied output applications, these devices must have a pull-up resistor to establish a logic HIGH level.

FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	Z
L	H	Z
H	L	Z
H	H	L

H = HIGH voltage level
L = LOW voltage level
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PZL}/t_{PLZ}	propagation delay nA, nB to nY	C_L = 15 pF; V_{CC} = 3.3 V	8	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1, 2 and 3	4	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}
3. The given value of C_{PD} is obtained with: C_L = 0 pF and $R_L = \infty$

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV03N	14	DIL	plastic	DIL14/SOT27
74LV03D	14	SO	plastic	SO14/SOT108A
74LV03DB	14	SSOP	plastic	SSOP14/SOT337
74LV03PW	14	TSSOP	plastic	TSSOP14/SOT402

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

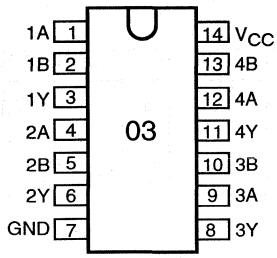


Fig.1 Pin configuration.

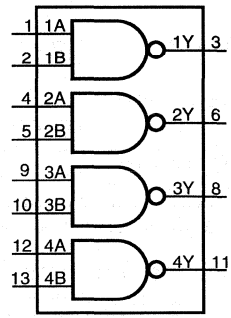


Fig.2 Logic symbol.

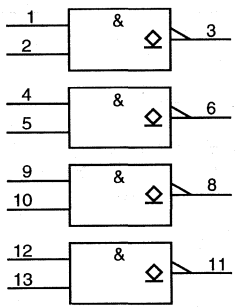


Fig.3 IEC Logic symbol.

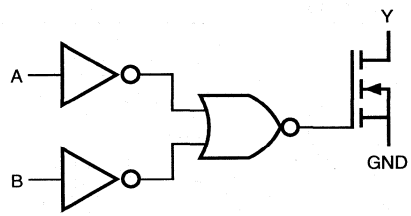


Fig.4 Logic diagram (one gate).

DC CHARACTERISTICS FOR 74LV03

For the DC characteristics see chapter "LV family characteristics", section "DC characteristics", except that the V_{OH} values are not valid for open drain. They are replaced by I_{OZ} as given below.
Output capability: standard (open drain), excepting V_{OH}.
I_{CC} category: SSI

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS		
		−40 to +85			−40 to +125			V_{CC} (V)	V_I	OTHER
		MIN.	TYP.	MAX.	MIN.	MAX.				
I_{OZ}	HIGH level output leakage current	–	–	5.0	–	10	μA	2.0 to 3.6	V_{IL}	$V_O = V_{O(max)}$* or GND

Notes: * The maximum operating output voltage ($V_{O(max)}$) is 3.6 V.

AC CHARACTERISTICS FOR 74LV03

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PZL}/t_{PLZ}	propagation delay nA, nB to nY	– – – –	50 17 13 10*	– 32 24 19	– – – –	– 39 29 23	ns	1.2 2.0 2.7 3.0 to 3.6	Fig.5

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

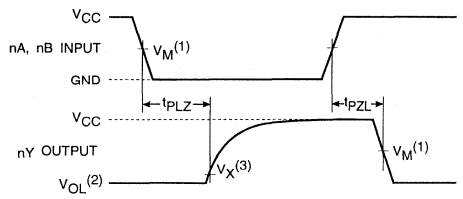
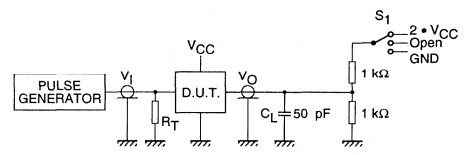


Fig. 5 Waveforms showing the input (nA, nB) to output (nY) propagation delays.



Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig. 6 Load circuitry for switching times.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Output capability: standard**
- **I_{CC} category: SSI**

DESCRIPTION

The 74LV04 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT04.

The 74LV04 provides six inverting buffers.

FUNCTION TABLE

INPUT	OUTPUT
nA	nY
L	H
H	L

H = HIGH voltage level
L = LOW voltage level

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 15 pF V_{CC} = 3.3 V	6	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	21	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV04N	14	DIL	plastic	DIL14/SOT27
74LV04D	14	SO	plastic	SO14/SOT108A
74LV04DB	14	SSOP	plastic	SSOP14/SOT337
74LV04PW	14	TSSOP	plastic	TSSOP14/SOT402

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A to 6A	data inputs
2, 4, 6, 8, 10, 12	1Y to 6Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

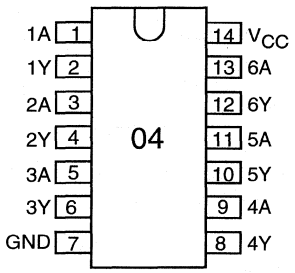


Fig.1 Pin configuration.

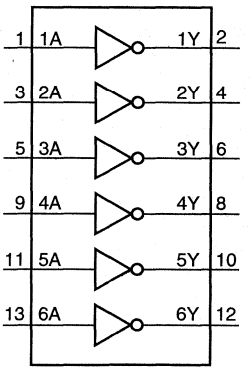


Fig.2 Logic symbol.

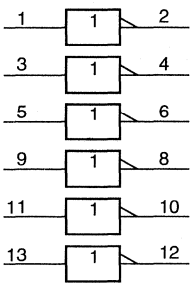


Fig.3 IEC Logic symbol.

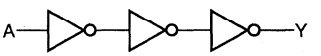


Fig.4 Logic diagram (one inverter).

DC CHARACTERISTICS FOR 74LV04

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74LV04

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay nA to nY	–	40	–	–	–	ns	1.2	Fig.5
		–	14	26	–	31		2.0	
		–	10	19	–	23		2.7	
		–	8*	15	–	18		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

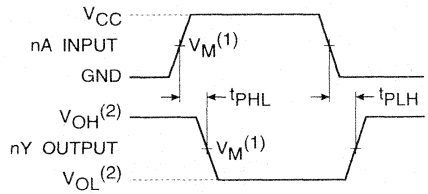


Fig. 5 Waveforms showing the input (nA) to output (nY) propagation delays.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Output capability: standard**
- **I_{CC} category: SSI**

DESCRIPTION

The 74LVU04 is a low-voltage Si-gate CMOS device and is pin compatible with the 74HCU04.

The 74LVU04 is a general purpose hex inverter. Each of the six inverters is a single stage.

FUNCTION TABLE

INPUT	OUTPUT
nA	nY
L	H
H	L

H = HIGH voltage level
L = LOW voltage level

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 15 pF V_{CC} = 3.3 V	6	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	18	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV04N	14	DIL	plastic	DIL14/SOT27
74LV04D	14	SO	plastic	SO14/SOT108A
74LV04DB	14	SSOP	plastic	SSOP14/SOT337
74LV04PW	14	TSSOP	plastic	TSSOP14/SOT402

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A to 6A	data inputs
2, 4, 6, 8, 10, 12	1Y to 6Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

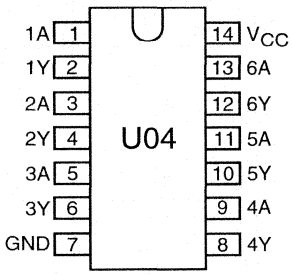


Fig.1 Pin configuration.

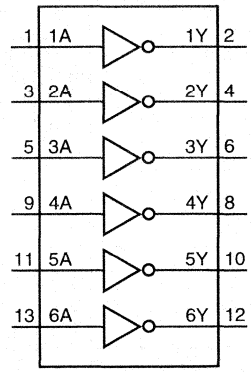


Fig.2 Logic symbol.

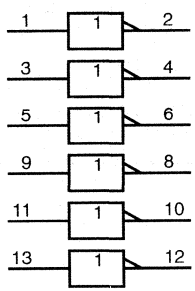


Fig.3 IEC Logic symbol.

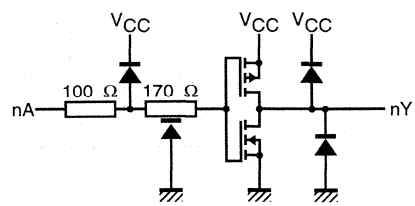


Fig.4 Schematic diagram (one inverter).

DC CHARACTERISTICS FOR THE LVU04

Over recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS		
		−40 to +85			−40 to +125			V_{CC} (V)	V_I	OTHER
		MIN.	TYP.	MAX.	MIN.	MAX.				
V_{IH}	HIGH level input voltage	1.0 1.6 2.4	– – –	– – –	1.0 1.6 2.4	– – –	V	1.2 2.0 2.7 to 3.6		
V_{IL}	LOW level input voltage	– – –	– – –	0.2 0.4 0.5	– – –	0.2 0.4 0.5	V	1.2 2.0 2.7 to 3.6		
V_{OH}	HIGH level output voltage	– 1.5 2.2 2.5	1.2 2.0 2.7 3.0	– – – –	– 1.5 2.2 2.5	– – – –	V	1.2 2.0 2.7 3.0	V_{IH} or V_{IL}	$-I_O$ = 100 μA
V_{OH}	HIGH level output voltage	2.4	2.82	–	2.20	–	V	3.0	V_{CC} or GND	$-I_O$ = 6 mA
V_{OL}	LOW level output voltage	– – – –	0 0 0 0	– 0.5 0.5 0.5	– – – –	– 0.5 0.5 0.5	V	1.2 2.0 2.7 3.0	V_{IH} or V_{IL}	I_O = 100 μA
V_{OL}	LOW level output voltage	–	0.25	0.4	–	0.5	V	3.0	V_{CC} or GND	I_O = 6 mA
$\pm I_I$	input leakage current	–	–	1.0	–	1.0	μA	3.6	V_{CC} or GND	
I_{CC}	quiescent supply current	–	–	20.0	–	40.0	μA	3.6	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current per input	–	–	500	–	850	μA	2.7 to 3.6	$V_I = V_{CC} - 0.6$ V	

AC CHARACTERISTICS FOR 74LVU04

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay nA to nY	–	35	–	–	–	ns	1.2	Fig. 5
		–	12	26	–	31		2.0	
		–	9	19	–	23		2.7	
		–	7*	15	–	18		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

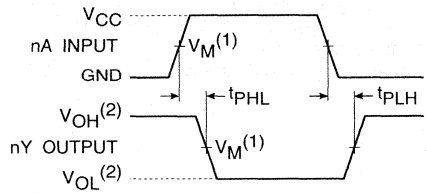


Fig. 5 Waveforms showing the data input (nA) to data output (nY) propagation delays.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

TYPICAL TRANSFER CHARACTERISTICS

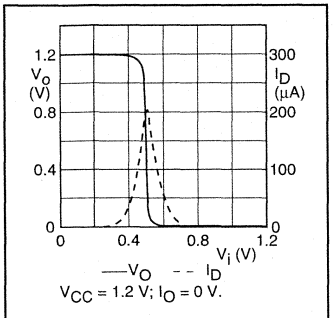


Fig.6

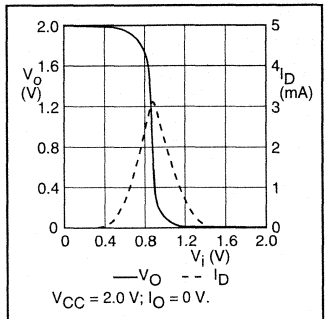


Fig.7

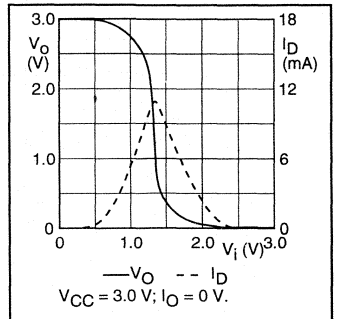


Fig.8

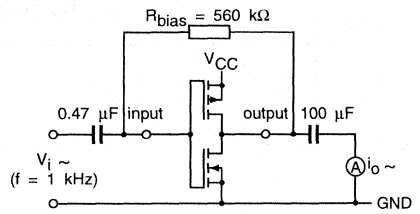


Fig.9 Test set-up for measuring forward transconductance $g_{fs} = di_o/dv_i$ at v_o is constant (see also graph Fig.10).

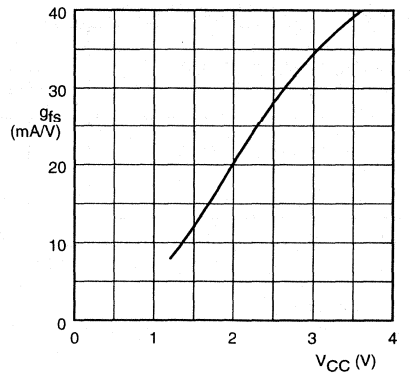


Fig.10 Typical forward transconductance g_{fs} as a function of the supply voltage V_{CC} at T_{amb} = 25 °C.

APPLICATION INFORMATION

Some applications for the 'LVU04' are:

- Linear amplifier (see Fig.11)
- In crystal oscillator designs (see Fig.12)
- Astable multivibrator (see Fig.13)

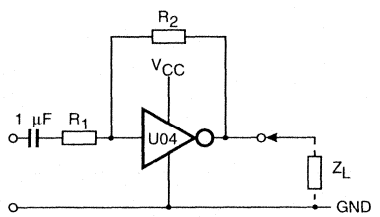


Fig.11 LVU04 used as a linear amplifier.

Note to Fig.11

Z_L > 10 kΩ; A_{OL} = 20 (typical)

$$A_u = -\frac{A_{OL}}{1 + \frac{R_2}{R_1}(1 + A_{OL})}$$; $V_{O\,max\,(P-P)} \approx V_{CC} - 1.5$ V centered at $^1/_2 V_{CC}$

3 kΩ ≤ R1, R2 ≤ 1 MΩ
Typical unity gain bandwidth product is 5 MHz.
C_l, see Fig.14
A_{OL} = open loop amplification
A_u = voltage amplification

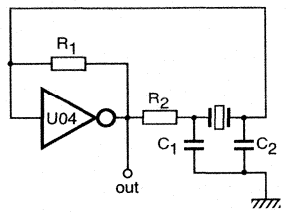


Fig.12 Crystal oscillator configuration.

Note to Fig.12
C_1 = 47 pF (typ.)
C_2 = 22 pF (typ.)
R_1 = 1 to 10 MΩ (typ.)
R_2 optimum value depends on the frequency and required stability against changes in V_{CC} or average minimum I_{CC} (I_{CC} is typically 2 mA at V_{CC} = 3 V and f = 1 MHz).

EXTERNAL COMPONENTS FOR RESONATOR (f < 1 MHz)

FREQUENCY (kHz)	R_1(MΩ)	R_2 (KΩ)	C_1 (pF)	C_2 (pF)
10 .. 15.9	2.2	220	56	20
16 .. 24.9	2.2	220	56	10
25 .. 54.9	2.2	100	56	10
55 .. 129.9	2.2	100	47	5
130 .. 199.9	2.2	47	47	5
200 .. 349.9	2.2	47	47	5
350 .. 600	2.2	47	47	5

Where:
All values given are typical and must be used as an initial set-up.

OPTIMUM VALUE FOR R_2

FREQUENCY (MHz)	R_2 (kΩ)	OPTIMUM FOR
3	2.0 8.0	minimum required I_{CC} minimum influence due to change in V_{CC}
6	1.0 4.7	minimum I_{CC} minimum influence by V_{CC}
10	0.5 2.0	minimum I_{CC} minimum influence by V_{CC}
14	0.5 1.0	minimum I_{CC} minimum influence by V_{CC}
> 14	replace R_2 by C_3 with a typical value of 35 pF	

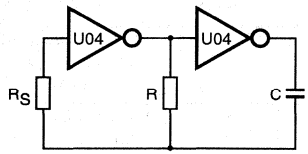


Fig.13 LVU04 used as an astable multivibrator.

Note to Fig.13

$$f = \frac{1}{T} \approx \frac{1}{2.2\ RC}$$

$R_S \approx 2 \times R$

The average I_{CC} (mA) is approximately 3.5 + 0.05 x f (MHz) x C (pF) at V_{CC} = 3.0 V.

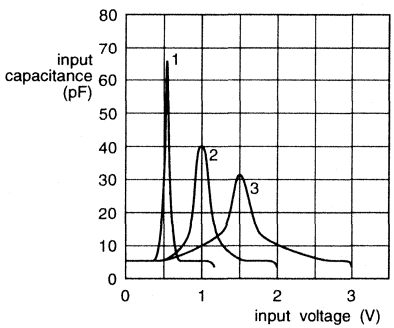


Fig.14 Typical input capacitance as a function of the input voltage.

Note to Fig.14

1. V_{CC} = 1.2 V.
2. V_{CC} = 2.0 V.
3. V_{CC} = 3.0 V.

Note to Application information

All values given are typical unless otherwise specified.

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Output capability: standard**
- **I_{CC} category: SSI**

DESCRIPTION

The 74LV08 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT08.

The 74LV08 provides the 2-input AND function.

FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	L
L	H	L
H	L	L
H	H	H

H = HIGH voltage level
L = LOW voltage level

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF V_{CC} = 3.3 V	7	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	10	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV08N	14	DIL	plastic	DIL14/SOT27
74LV08D	14	SO	plastic	SO14/SOT108A
74LV08DB	14	SSOP	plastic	SSOP14/SOT337
74LV08PW	14	TSSOP	plastic	TSSOP14/SOT402

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

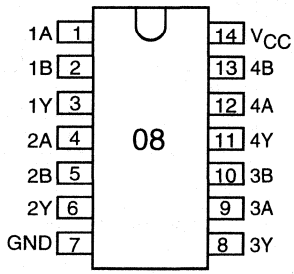


Fig.1 Pin configuration.

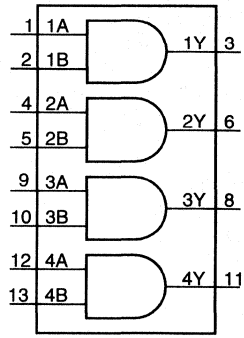


Fig.2 Logic symbol.

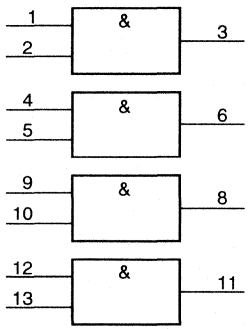


Fig.3 IEC Logic symbol.

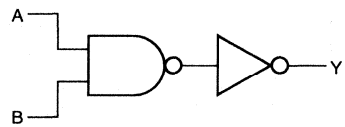


Fig.4 Logic diagram (one gate).

DC CHARACTERISTICS FOR 74LV08

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74LV08

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	–	45	–	–	–	ns	1.2	Fig.5
		–	15	31	–	36		2.0	
		–	11	23	–	26		2.7	
		–	9*	18	–	21		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

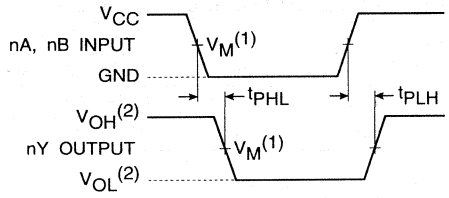


Fig.5 Waveforms showing the input (nA, nB) to output (nY) propagation delays.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

Triple 3-input NAND gate | 74LV10

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Output capability: standard**
- **I_{CC} category: SSI**

DESCRIPTION

The 74LV10 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT10.

The 74LV10 provides the 3-input NAND function.

FUNCTION TABLE

INPUTS			OUTPUTS
nA	nB	nC	nY
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

H = HIGH voltage level
L = LOW voltage level

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA, nB, nC to nY	C_L = 15 pF V_{CC} = 3.3 V	9	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	12	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV10N	14	DIL	plastic	DIL14/SOT27
74LV10D	14	SO	plastic	SO14/SOT108A
74LV10DB	14	SSOP	plastic	SSOP14/SOT337
74LV10PW	14	TSSOP	plastic	TSSOP14/SOT402

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 9	1A to 3A	data inputs
2, 4, 10	1B to 3B	data inputs
7	GND	ground (0 V)
12, 6, 8	1Y to 3Y	data outputs
13, 5, 11	1C to 3C	data inputs
14	V_{CC}	positive supply voltage

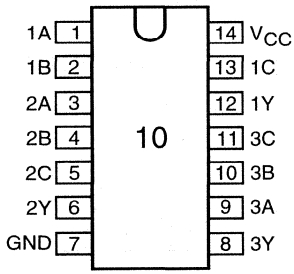


Fig.1 Pin configuration.

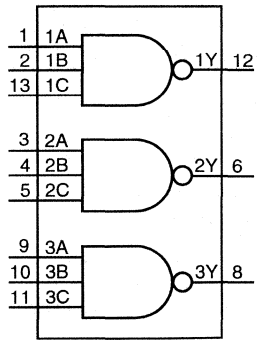


Fig.2 Logic symbol.

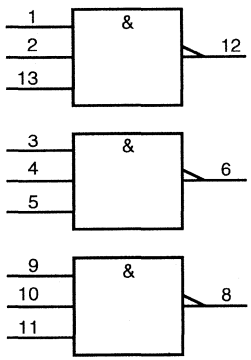


Fig.3 IEC Logic symbol.

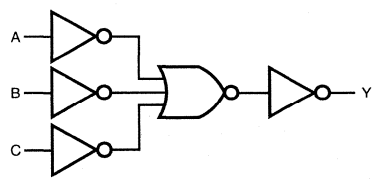


Fig.4 Logic diagram (one gate).

DC CHARACTERISTICS FOR 74LV10

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74LV10

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay nA, nB, nC to nY	–	55	–	–	–	ns	1.2	Fig. 5
		–	19	36	–	44		2.0	
		–	14	26	–	33		2.7	
		–	10*	21	–	26		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

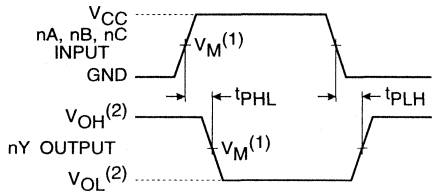


Fig. 5 Waveforms showing the input (nA, nB, nC) to output (nY) propagation delays.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

Triple 3-input AND gate | 74LV11

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Output capability: standard**
- **I_{CC} category: SSI**

DESCRIPTION

The 74LV11 a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT11.

The 74LV11 provides the 3-input AND function.

FUNCTION TABLE

INPUTS			OUTPUTS
nA	nB	nC	nY
L	L	L	L
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	H

H = HIGH voltage level
L = LOW voltage level

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA, nB, nC to nY	C_L = 15 pF V_{CC} = 3.3 V	10	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	18	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV11N	14	DIL	plastic	DIL14/SOT27
74LV11D	14	SO	plastic	SO14/SOT108A
74LV11DB	14	SSOP	plastic	SSOP14/SOT337
74LV11PW	14	TSSOP	plastic	TSSOP14/SOT402

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 9	1A to 3A	data inputs
2, 4, 10	1B to 3B	data inputs
7	GND	ground (0 V)
12, 6, 8	1Y to 3Y	data outputs
13, 5, 11	1C to 3C	data inputs
14	V_{CC}	positive supply voltage

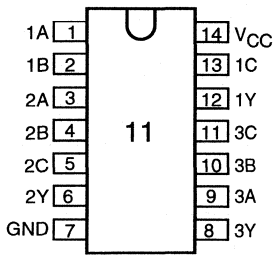


Fig.1 Pin configuration.

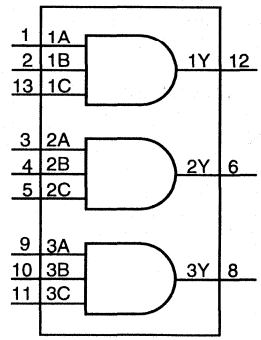


Fig.2 Logic symbol.

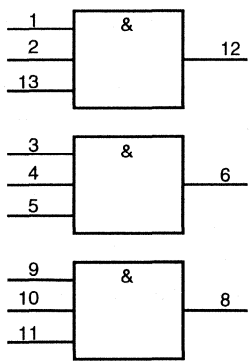


Fig.3 IEC Logic symbol.

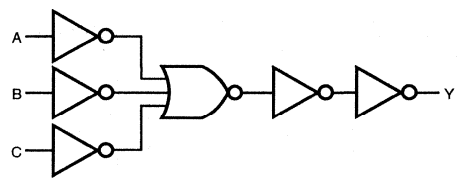


Fig.4 Logic diagram (one gate).

DC CHARACTERISTICS FOR 74LV11

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74LV11

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay nA, nB, nC to nY	–	60	–	–	–	ns	1.2	Fig. 5
		–	20	39	–	46		2.0	
		–	15	29	–	34		2.7	
		–	11*	23	–	27		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

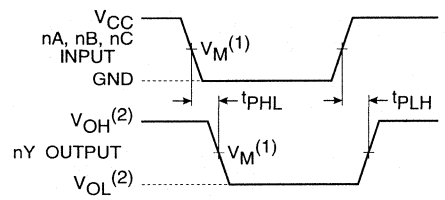


Fig. 5 Waveforms showing the input (nA, nB, nC) to output (nY) propagation delays.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Output capability: standard**
- **I_{CC} category: SSI**

APPLICATIONS

- **Wave and pulse shapers for highly noisy environments**

DESCRIPTION

The 74LV14 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT14.

The 74LV14 provides six inverting buffers with Schmitt-trigger action. It is capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

FUNCTION TABLE

INPUT	OUTPUT
nA	nY
L	H
H	L

H = HIGH voltage level
L = LOW voltage level

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 15 pF V_{CC} = 3.3 V	13	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	15	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV14N	14	DIL	plastic	DIL14/SOT27
74LV14D	14	SO	plastic	SO14/SOT108A
74LV14DB	14	SSOP	plastic	SSOP14/SOT337
74LV14PW	14	TSSOP	plastic	TSSOP14/SOT402

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A to 6A	data inputs
2, 4, 6, 8, 10, 12	1Y to 6Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

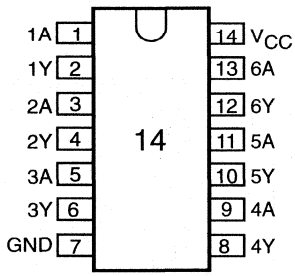


Fig.1 Pin configuration.

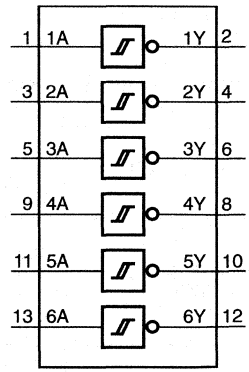


Fig.2 Logic symbol.

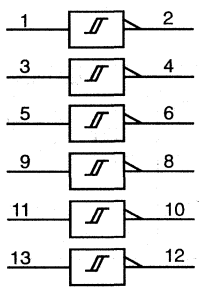


Fig.3 IEC Logic symbol.

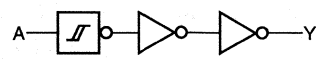


Fig.4 Logic diagram (one Schmitt-trigger).

DC CHARACTERISTICS FOR 74LV14

For the DC characteristics see chapter "LV family characteristics", section "Family specifications". Transfer characteristics are given below.
Output capability: standard
I_{CC} category: SSI

TRANSFER CHARACTERISTICS FOR 74LV14

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
V_{T+}	positive-going threshold	–	0.70	–	–	–	V	1.2	Figs 5 and 6
		0.8	1.10	1.4	0.8	1.4		2.0	
		1.0	1.45	2.0	1.0	2.0		2.7	
		1.2	1.60	2.2	1.2	2.2		3.0	
		1.5	1.95	2.4	1.5	2.4		3.6	
V_{T-}	negative-going threshold	–	0.34	–	–	–	V	1.2	Figs 5 and 6
		0.3	0.65	0.9	0.3	0.9		2.0	
		0.4	0.90	1.4	0.4	1.4		2.7	
		0.6	1.05	1.5	0.6	1.5		3.0	
		0.8	1.30	1.8	0.8	1.8		3.6	
V_H	hysteresis ($V_{T+} - V_{T-}$)	–	0.30	–	–	–	V	1.2	Figs 5 and 6
		0.2	0.55	0.8	0.2	0.8		2.0	
		0.3	0.60	1.1	0.3	1.1		2.7	
		0.4	0.65	1.2	0.4	1.2		3.0	
		0.4	0.70	1.2	0.4	1.2		3.6	

Note: All typical values are measured at T_{amb} = 25 °C.
The V_{IH} and V_{IL} from the DC family characteristics are superseeded by the V_{T+} and V_{T-}.

AC CHARACTERISTICS FOR 74LV14

GND = 0 V; $t_r = t_f \leq 2.5$ ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay nA to nY	–	75	–	–	–	ns	1.2	Fig.10
		–	26	49	–	60		2.0	
		–	19	36	–	44		2.7	
		–	14*	29	–	35		3.0 to 3.6	

Notes: All typical values are measured at T_{amb} = 25 °C.
* Typical values are measured at V_{CC} = 3.3 V.

TRANSFER CHARACTERISTIC WAVEFORMS

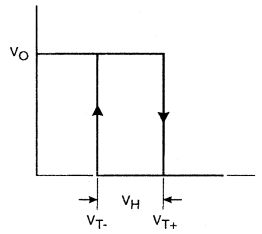


Fig.5 Transfer characteristic.

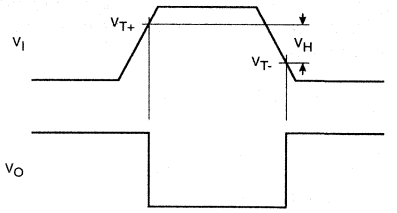


Fig. 6 Waveforms showing the definition of V_{T+}, V_{T-} and V_H; where V_{T+} and V_{T-} are between limits of 20% and 70%.

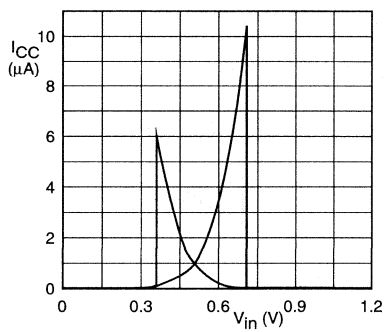


Fig.7 Typical LV14 transfer characteristics; V_{CC} = 1.2 V.

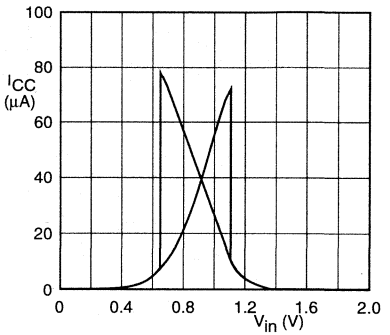


Fig.8 Typical LV14 transfer characteristics; V_{CC} = 2.0 V.

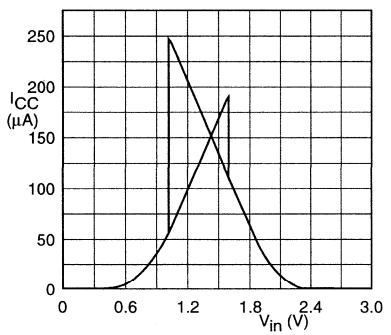


Fig.9 Typical LV14 transfer characteristics; V_{CC} = 3.0 V.

AC WAVEFORMS

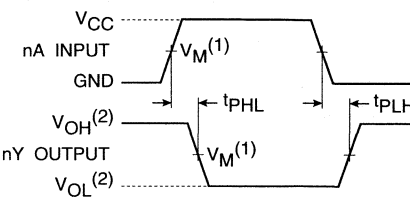


Fig.10 Waveforms showing the input (nA) to output (nY) propagation delays.

Notes to the AC waveforms

(1) V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
$V_M = 0.5 \cdot V_{CC}$ at V_{CC} < 2.7 V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

APPLICATION INFORMATION

The slow input rise and fall times cause additional power dissipation, this can be calculated using the following formula:

$P_{ad} = f_i \times (t_r \times I_{CCa} + t_f \times I_{CCa}) \times V_{CC}$.

Where:

P_{ad} = additional power dissipation (μW)
f_i = input frequency (MHz)
t_r = input rise time (ns); 10% – 90%
t_f = input fall time (ns); 10% – 90%
I_{CCa} = average additional supply current (μA)

Average I_{CCa} differs with positive or negative input transitions, as shown in fig.11.

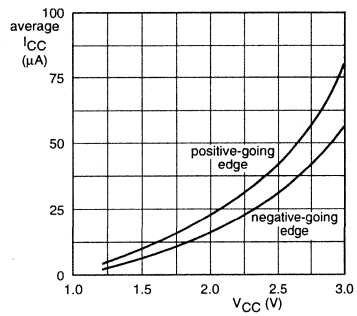


Fig.11 Average I_{CC} for LV Schmitt-trigger devices; linear change of V_i between 0.1 V_{CC} to 0.9 V_{CC}.

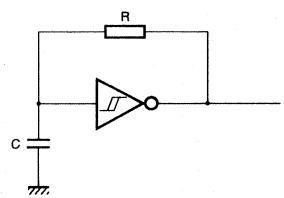


Fig.12 Relaxation oscillator using the LV14.

Note to the application information
All values given are typical unless otherwise specified.

Note to fig.12

$$f = \frac{1}{T} \approx \frac{1}{0.8 \times RC}$$

Dual 4-input NAND gate | 74LV20

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Output capability: standard**
- **I_{CC} category: SSI**

DESCRIPTION

The 74LV20 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT20.

The 74LV20 provides the 4-input NAND function.

FUNCTION TABLE

INPUTS				OUTPUTS
nA	nB	nC	nD	nY
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA, nB, nC, nD to nY	C_L = 15 pF; V_{CC} = 3.3 V	7	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	22	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV20N	14	DIL	plastic	DIL14/SOT27
74LV20D	14	SO	plastic	SO14/SOT108A
74LV20DB	14	SSOP	plastic	SSOP14/SOT337
74LV20PW	14	TSSOP	plastic	TSSOP14/SOT402

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 9	1A to 2A	data inputs
2, 10	1B to 2B	data inputs
3, 11	n.c.	not connected
4, 12	1C to 2C	data inputs
5, 13	1D to 2D	data inputs
6, 8	1Y to 2Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

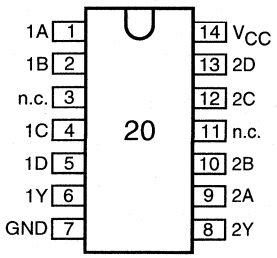


Fig.1 Pin configuration.

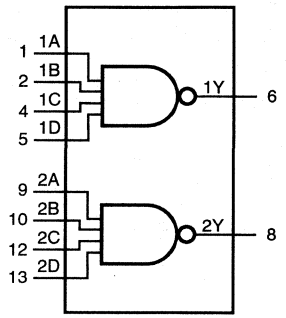


Fig.2 Logic symbol.

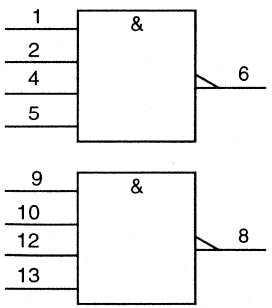


Fig.3 IEC Logic symbol.

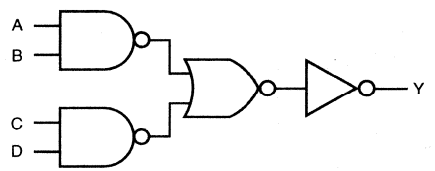


Fig.4 Logic diagram (one gate).

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Output capability: standard**
- **I_{CC} category: SSI**

DESCRIPTION

The 74LV27 a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT27.

The 74LV27 provides the 3-input NOR function.

FUNCTION TABLE

INPUTS			OUTPUTS
nA	nB	nC	nY
L	L	L	H
X	X	H	L
X	H	X	L
H	X	X	L

H = HIGH voltage level
L = LOW voltage level
X = don't care

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA, nB, nC to nY	C_L = 15 pF V_{CC} = 3.3 V	8	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	24	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV27N	14	DIL	plastic	DIL14/SOT27
74LV27D	14	SO	plastic	SO14/SOT108A
74LV27DB	14	SSOP	plastic	SSOP14/SOT337
74LV27PW	14	TSSOP	plastic	TSSOP14/SOT402

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 9	1A to 3A	data inputs
2, 4, 10	1B to 3B	data inputs
13, 5, 11	1C to 3C	data inputs
7	GND	ground (0 V)
12, 6, 8	1Y to 3Y	data outputs
14	V_{CC}	positive supply voltage

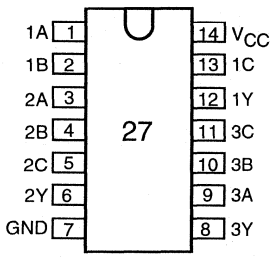


Fig.1 Pin configuration.

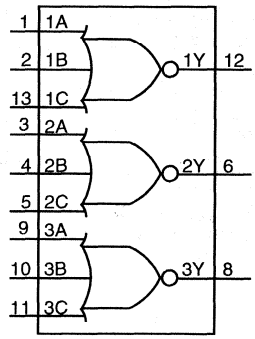


Fig.2 Logic symbol.

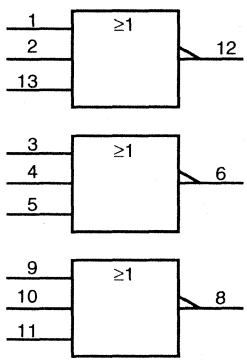


Fig.3 IEC Logic symbol.

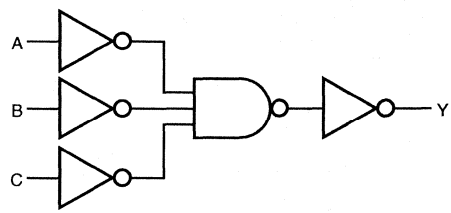


Fig.4 Logic diagram (one gate).

DC CHARACTERISTICS FOR 74LV27

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74LV27

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay nA, nB, nC to nY	–	50	–	–	–	ns	1.2	Fig. 5
		–	17	32	–	39		2.0	
		–	13	24	–	29		2.7	
		–	10*	19	–	23		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

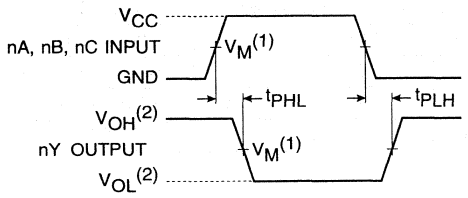


Fig. 5 Waveforms showing the input (nA, nB, nC) to output (nY) propagation delays.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

Quad 2-input OR gate | 74LV32

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Output capability: standard**
- **I_{CC} category: SSI**

DESCRIPTION

The 74LV32 a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT32.

The 74LV32 provides the 2-input OR function.

FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	H

H = HIGH voltage level
L = LOW voltage level

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF V_{CC} = 3.3 V	6	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	16	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV32N	14	DIL	plastic	DIL14/SOT27
74LV32D	14	SO	plastic	SO14/SOT108A
74LV32DB	14	SSOP	plastic	SSOP14/SOT337
74LV32PW	14	TSSOP	plastic	TSSOP14/SOT402

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

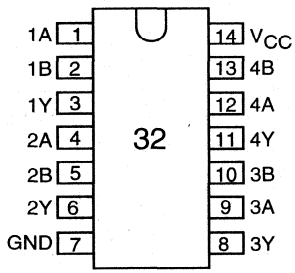


Fig.1 Pin configuration.

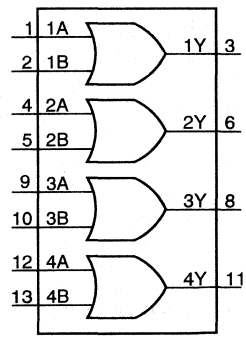


Fig.2 Logic symbol.

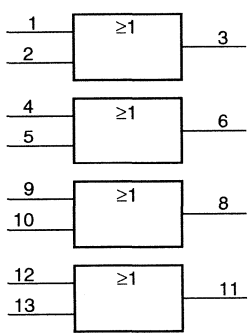


Fig.3 IEC Logic symbol.

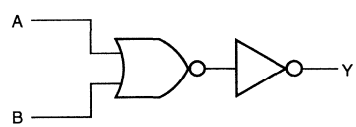


Fig.4 Logic diagram (one gate).

DC CHARACTERISTICS FOR 74LV32

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74LV32

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	–	40	–	–	–	ns	1.2	Fig.5
		–	14	29	–	34		2.0	
		–	10	22	–	25		2.7	
		–	8*	17	–	20		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

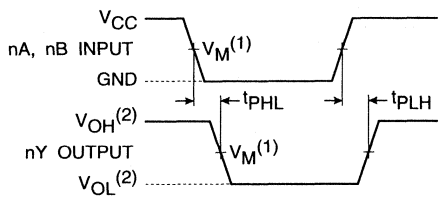


Fig. 5 Waveforms showing the input (nA, nB) to output (nY) propagation delays.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

Dual D-type flip-flop with set and reset; positive-edge trigger

74LV74

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Output capability: standard**
- **I_{CC} category: flip-flops**

GENERAL DESCRIPTION

The 74LV74 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT74.

The 74LV74 is a dual positive edge triggered, D-type flip-flop with individual data (D) inputs, clock (CP) inputs, set ($\overline{S}_D$) and ($\overline{R}_D$) inputs; also complementary Q and $\overline{Q}$ outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition, for predictable operation.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nCP to nQ, n$\overline{Q}$ n$\overline{S}_D$ to nQ, n$\overline{Q}$ n$\overline{R}_D$ to nQ, n$\overline{Q}$	C_L = 15 pF V_{CC} = 3.3 V	 11 14 14	ns
f_{max}	maximum clock frequency		76	MHz
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	24	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV74N	14	DIL	plastic	DIL14/SOT27
74LV74D	14	SO	plastic	SO14/SOT108A
74LV74DB	14	SSOP	plastic	SSOP14/SOT337
74LV74PW	14	TSSOP	plastic	TSSOP14/SOT402

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 13	1$\overline{R}_D$, 2$\overline{R}_D$	asynchronous reset-direct input (active LOW)
2, 12	1D, 2D	data inputs
3, 11	1CP, 2CP	clock input (LOW-to-HIGH, edge-triggered)
4, 10	1$\overline{S}_D$, 2$\overline{S}_D$	asynchronous set-direct input (active LOW)
5, 9	1Q, 2Q	true flip-flop outputs
6, 8	1$\overline{Q}$, 2$\overline{Q}$	complement flip-flop outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

Dual D-type flip-flop with set and reset; positive-edge trigger

74LV74

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{S}_D$	$\overline{R}_D$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH CP transition
Q_{n+1} = state after the next LOW-to-HIGH CP transition

INPUTS				OUTPUTS	
$\overline{S}_D$	$\overline{R}_D$	CP	D	Q_{n+1}	$\overline{Q}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

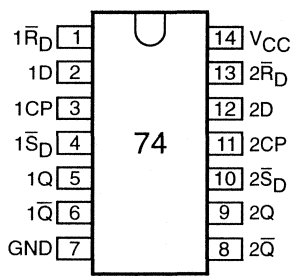


Fig.1 Pin configuration.

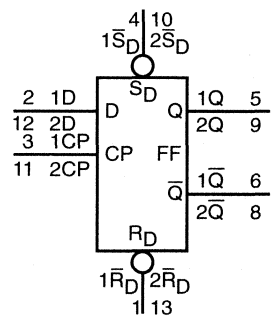


Fig.2 Logic symbol.

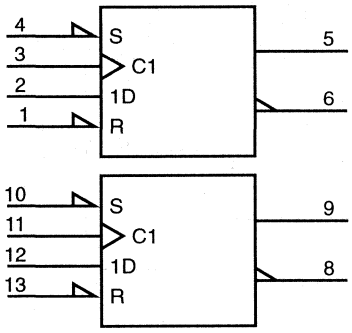


Fig.3 IEC Logic symbol.

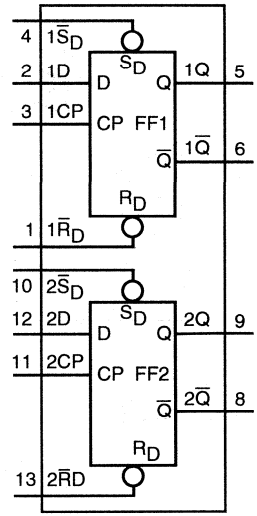


Fig.4 Functional diagram.

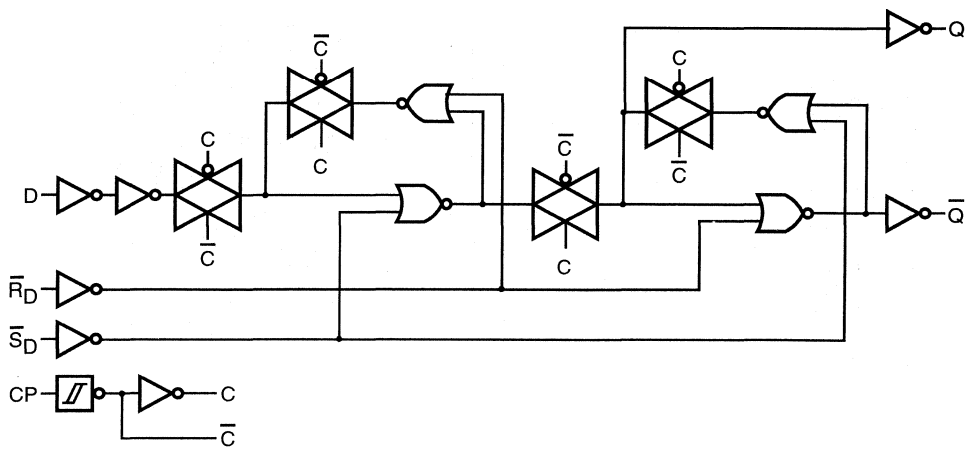


Fig.5 Logic diagram (one flip-flop).

DC CHARACTERISTICS FOR 74LV74

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: standard
I_{CC} category: flip-flops

AC CHARACTERISTICS FOR 74LV74

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay nCP to nQ, n$\overline{Q}$	– – – –	70 24 18 13*	– 48 35 28	– – – –	– 54 40 32	ns	1.2 2.0 2.7 3.0 to 3.6	Fig. 6
t_{PHL}/t_{PLH}	propagation delay n$\overline{S}_D$ to nQ, n$\overline{Q}$	– – – –	90 31 23 17*	– 58 43 34	– – – –	– 70 51 41	ns	1.2 2.0 2.7 3.0 to 3.6	Fig. 7
t_{PHL}/t_{PLH}	propagation delay n$\overline{R}_D$ to nQ, n$\overline{Q}$	– – – –	90 31 23 17*	– 58 43 34	– – – –	– 70 51 41	ns	1.2 2.0 2.7 3.0 to 3.6	Fig. 7
t_W	clock pulse width HIGH or LOW	34 25 20	10 8 7*	– – –	41 30 24	– – –	ns	2.0 2.7 3.0 to 3.6	Fig. 6
t_W	set or reset pulse width LOW	34 25 20	10 8 7*	– – –	41 30 24	– – –	ns	2.0 2.7 3.0 to 3.6	Fig. 7
t_{rem}	removal time set or reset	– 14 10 8	5 2 1 1*	– – – –	– 15 11 9	– – – –	ns	1.2 2.0 2.7 3.0 to 3.6	Fig. 7
t_{su}	set-up time nD to nCP	– 22 16 13	10 4 3 2*	– – – –	– 26 19 15	– – – –	ns	1.2 2.0 2.7 3.0 to 3.6	Fig. 6
t_h	hold time nD to nCP	– 3 3 3	−10 −2 −2 −2*	– – – –	– 3 3 3	– – – –	ns	1.2 2.0 2.7 3.0 to 3.6	Fig. 6
f_{max}	maximum clock pulse frequency	14 19 24	40 58 70*	– – –	12 16 20	– – –	MHz	2.0 2.7 3.0 to 3.6	Fig. 6

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

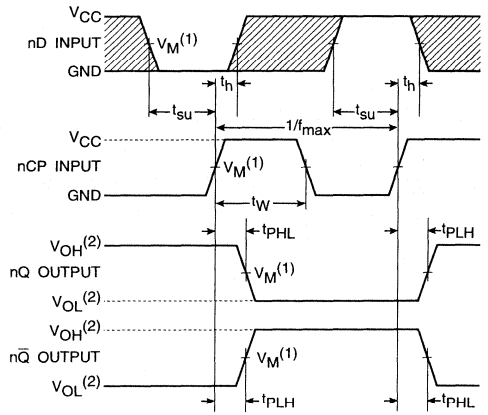


Fig. 6 Waveforms showing the clock (nCP) to output (nQ, nQ̄) propagation delays, the clock pulse width, the nD to nCP set-up times, the nCP to nD hold times and the maximum clock pulse frequency.

Note to Fig.6

The shaded areas indicate when the input is permitted to change for predictable output performance.

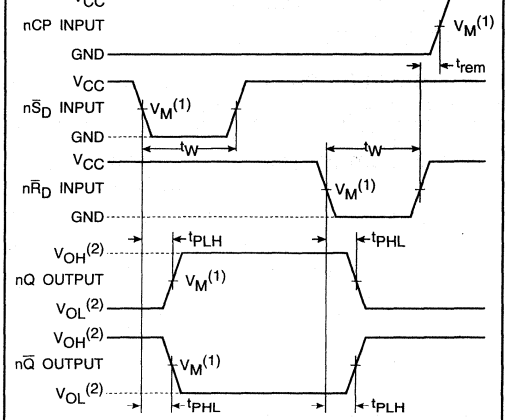


Fig.7 Waveforms showing the set ($n\overline{S}_D$) and reset ($n\overline{R}_D$) input to output (nQ, nQ̄) propagation delays, the set and reset pulse widths and the $n\overline{R}_D$ to nCP removal time.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

Quad 2-input EXCLUSIVE-OR gate | 74LV86

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Output capability: standard**
- **I_{CC} category: SSI**

DESCRIPTION

The 74LV86 a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT86.

The 74LV86 provides the 2-input EXCLUSIVE-OR function.

FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF; V_{CC} = 3.3 V	11	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	30	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV86N	14	DIL	plastic	DIL14/SOT27
74LV86D	14	SO	plastic	SO14/SOT108A
74LV86DB	14	SSOP	plastic	SSOP14/SOT337
74LV86PW	14	TSSOP	plastic	TSSOP14/SOT402

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

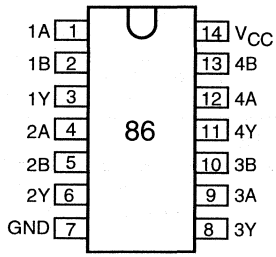


Fig.1 Pin configuration.

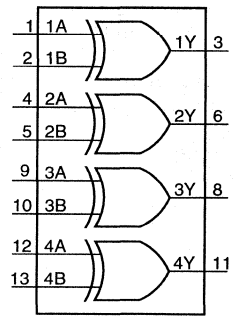


Fig.2 Logic symbol.

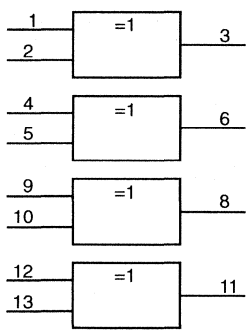


Fig.3 IEC Logic symbol.

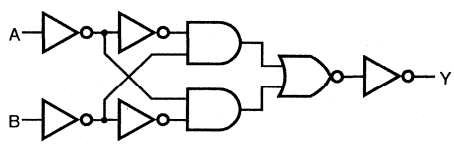


Fig.4 Logic diagram (one gate).

DC CHARACTERISTICS FOR 74LV86

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74LV86

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	–	70	–	–	–	ns	1.2	Fig.5
		–	24	44	–	54		2.0	
		–	18	33	–	40		2.7	
		–	13*	26	–	32		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

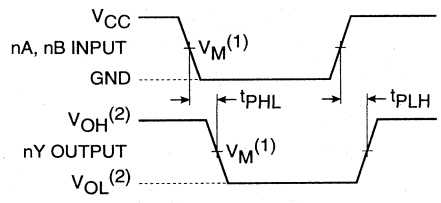


Fig. 5 Waveforms showing the input (nA, nB) to output (nY) propagation delays.

Notes: (1) $V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
$V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

Dual JK flip-flop with reset; negative-edge trigger | 74LV107

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Output capability: standard**
- **I_{CC} category: flip-flops**

DESCRIPTION

The 74LV107 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT107.

The 74LV107 is a dual negative-edge triggered JK-type flip-flop featuring individual J, K, clock ($n\overline{CP}$) and reset ($n\overline{R}$) inputs; also complementary Q and $\overline{Q}$ outputs.

The J and K inputs must be stable one set-up time prior to the HIGH-to-LOW clock transition for predictable operation.

The reset ($n\overline{R}$) is an asynchronous active LOW input. When LOW, it overrides the clock and data inputs, forcing the Q output LOW and the $\overline{Q}$ output HIGH.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to nQ $n\overline{CP}$ to $n\overline{Q}$ $n\overline{R}$ to nQ, $n\overline{Q}$	C_L = 15 pF V_{CC} = 3.3 V	 15 15 15	ns
f_{max}	maximum clock frequency		77	MHz
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	30	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV107N	14	DIL	plastic	DIL14/SOT27
74LV107D	14	SO	plastic	SO14/SOT108A
74LV107DB	14	SSOP	plastic	SSOP14/SOT337
74LV107PW	14	TSSOP	plastic	TSSOP14/SOT402

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1, 8, 4, 11	1J, 2J, 1K, 2K	synchronous inputs; flip-flops 1 and 2
2, 6	$1\overline{Q}$, $2\overline{Q}$	complement flip-flop outputs
3, 5	1Q, 2Q	true flip-flop outputs
7	GND	ground (0 V)
12, 9	$1\overline{CP}$, $2\overline{CP}$	clock input (HIGH-to-LOW, edge-triggered)
13, 10	$1\overline{R}$, $2\overline{R}$	asynchronous reset inputs (active LOW)
14	V_{CC}	positive supply voltage

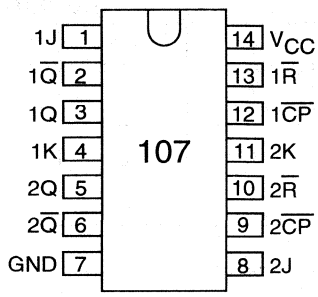


Fig.1 Pin configuration.

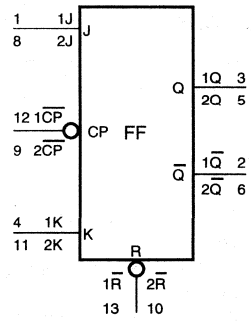


Fig.2 Logic symbol.

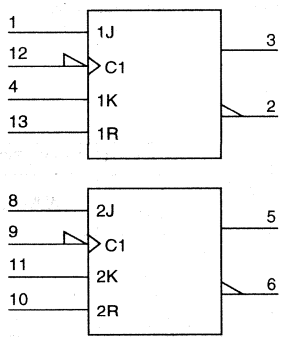


Fig3. IEC logic symbol.

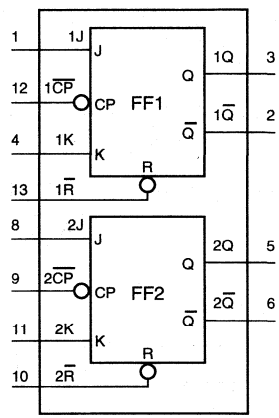


Fig.4 Functional diagram.

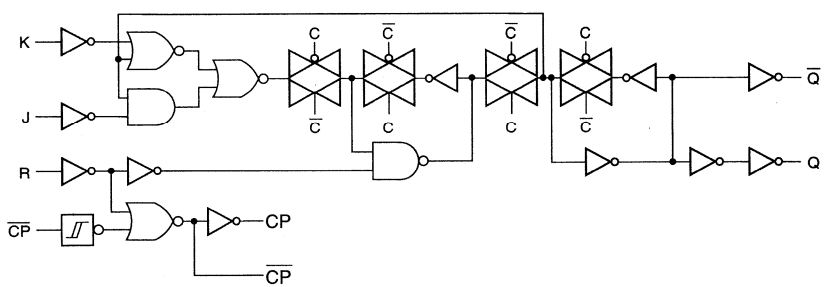


Fig.5 Logic diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS				OUTPUTS	
	$n\overline{R}$	$n\overline{CP}$	nJ	nK	nQ	$n\overline{Q}$
asynchronous reset	L	X	X	X	L	H
toggle	H	↓	h	h	$\overline{q}$	q
load "0" (reset)	H	↓	l	h	L	H
load "1" (set)	H	↓	h	l	H	L
hold "no change"	H	↓	l	l	q	$\overline{q}$

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW CP transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the HIGH-to-LOW CP transition.
X = don't care
↓ = HIGH-to-LOW CP transition

DC CHARACTERISTICS FOR 74LV107

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: standard
I_{CC} category: flip-flops

AC CHARACTERISTICS FOR 74LV107

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to nQ, $n\overline{Q}$	–	95	–	–	–	ns	1.2	Fig.6
		–	32	61	–	75		2.0	
		–	24	45	–	55		2.7	
		–	18*	36	–	44		3.0 to 3.6	
t_{PHL}/t_{PLH}	propagation delay $n\overline{R}$ to nQ, $n\overline{Q}$	–	95	–	–	–	ns	1.2	Fig.7
		–	32	61	–	75		2.0	
		–	24	45	–	55		2.7	
		–	18*	36	–	44		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC CHARACTERISTICS FOR 74LV107 ***(Continued)***

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_W	clock pulse width HIGH or LOW	34	14	–	41	–	ns	2.0	Fig.6
		25	10	–	30	–		2.7	
		20	8*	–	24	–		3.0 to 3.6	
t_W	reset pulse width LOW	34	14	–	41	–	ns	2.0	Fig.7
		25	10	–	30	–		2.7	
		20	8*	–	24	–		3.0 to 3.6	
t_{rem}	removal time $n\overline{R}$ to $n\overline{CP}$	–	35	–	–	–	ns	1.2	Fig.7
		24	12	–	29	–		2.0	
		18	9	–	21	–		2.7	
		14	7*	–	17	–		3.0 to 3.6	
t_{su}	set-up time nJ, nK to $\overline{CP}$	–	40	–	–	–	ns	1.2	Fig.6
		26	14	–	31	–		2.0	
		19	10	–	23	–		2.7	
		15	8*	–	18	–		3.0 to 3.6	
t_h	hold time nJ, nK to $\overline{CP}$	–	−10	–	–	–	ns	1.2	Fig.6
		5	−3	–	5	–		2.0	
		5	−2	–	5	–		2.7	
		5	−2*	–	5	–		3.0 to 3.6	
f_{max}	maximum clock pulse frequency	14	40	–	12	–	MHz	2.0	Fig.6
		19	58	–	16	–		2.7	
		24	70*	–	20	–		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.

* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

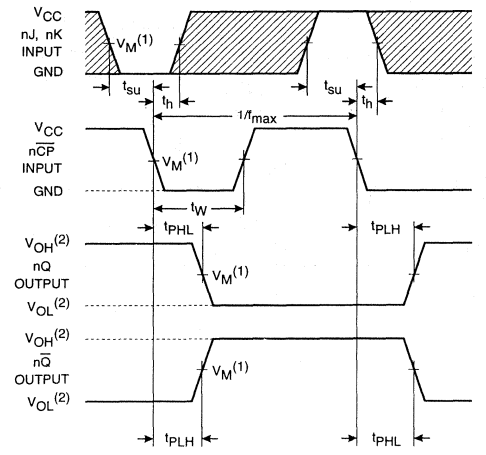


Fig.6 Waveforms showing the clock ($n\overline{CP}$) to output (nQ, $n\overline{Q}$) propagation delays, the clock pulse width, the J and K to $n\overline{CP}$ set-up and hold times and the maximum clock pulse frequency.

Note to Fig.6: The shaded areas indicate when the input is permitted to change for predictable output performance.

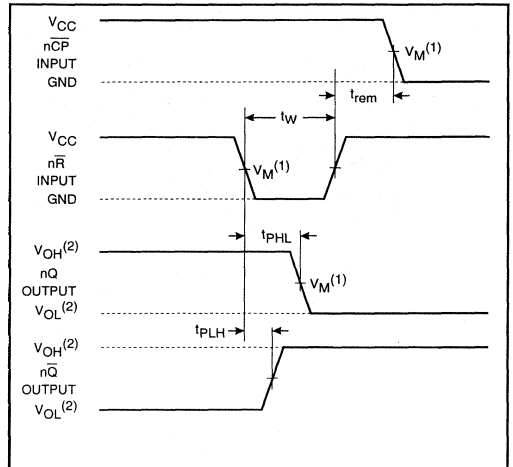


Fig.7 Waveforms showing the reset ($n\overline{R}$) input to output (nQ, $n\overline{Q}$) propagation delays, the reset pulse width and the $n\overline{R}$ to $n\overline{CP}$ removal time.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

Dual $J\overline{K}$ flip-flop with set and reset; positive-edge trigger 74LV109

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Output capability: standard**
- **I_{CC} category: flip-flops**

DESCRIPTION

The 74LV109 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT109.

The 74LV109 is a dual positive-edge triggered $J\overline{K}$-type flip-flop featuring individual J, $\overline{K}$ inputs, clock (CP) inputs, set ($\overline{S}_D$) and reset ($\overline{R}_D$) inputs; also complementary Q and $\overline{Q}$ outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input.

The J and $\overline{K}$ inputs control the state changes of the flip-flops as described in the mode select function table.
The J and $\overline{K}$ inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

The $J\overline{K}$ design allows operation as a D-type flip-flop by tying the J and $\overline{K}$ inputs together.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nCP to nQ, n$\overline{Q}$ n$\overline{S}_D$ to nQ, n$\overline{Q}$ n$\overline{R}_D$ to nQ, n$\overline{Q}$	C_L = 15 pF V_{CC} = 3.3 V	 14 12 12	ns
f_{max}	maximum clock frequency		77	MHz
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	20	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV109N	16	DIL	plastic	DIL16/SOT38Z
74LV109D	16	SO	plastic	SO16/SOT109A
74LV109DB	16	SSOP	plastic	SSOP16/SOT338
74LV109PW	16	TSSOP	plastic	TSSOP16/SOT403

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1, 15	1$\overline{R}_D$, 2$\overline{R}_D$	asynchronous reset input (active LOW)
2, 14, 3, 13	1J, 2J, 1$\overline{K}$, 2$\overline{K}$	synchronous inputs; flip-flops 1 and 2
4, 12	1CP, 2CP	clock input (LOW-to-HIGH, edge-triggered)
5, 11	1$\overline{S}_D$, 2$\overline{S}_D$	asynchronous set inputs (active LOW)
6, 10	1Q, 2Q	true flip-flop outputs
7, 9	1$\overline{Q}$, 2$\overline{Q}$	complement flip-flop outputs
8	GND	ground (0 V)
16	V_{CC}	positive supply voltage

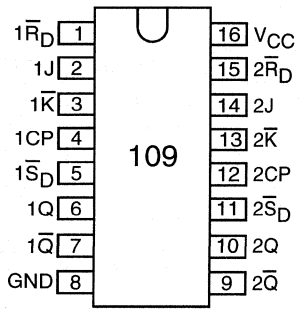


Fig.1 Pin configuration.

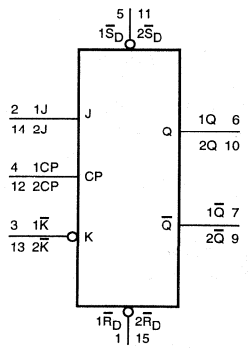


Fig.2 Logic symbol.

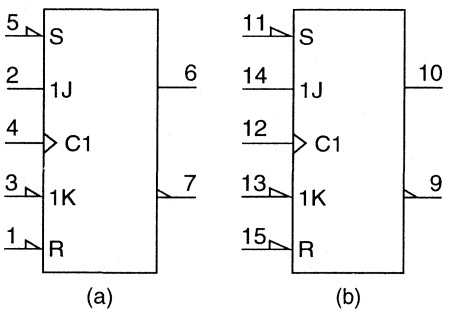


Fig3. IEC logic symbol.

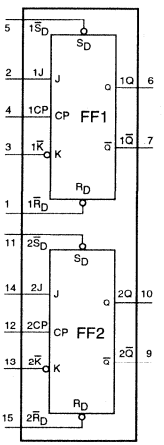


Fig.4 Functional diagram.

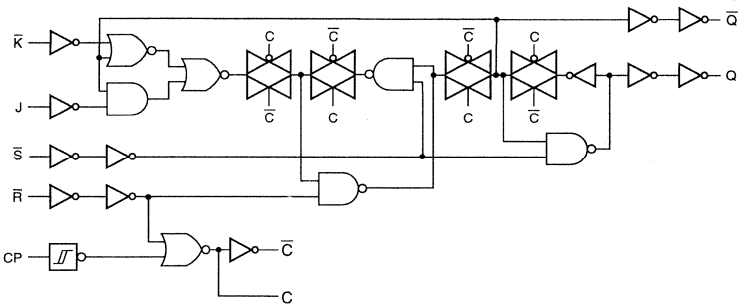


Fig.5 Logic diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS					OUTPUTS	
	$n\overline{S}_D$	$n\overline{R}_D$	nCP	nJ	$n\overline{K}$	nQ	$n\overline{Q}$
asynchronous set	L	H	X	X	X	H	L
asynchronous reset	H	L	X	X	X	L	H
undetermined	L	L	X	X	X	H	H
toggle	H	H	↑	h	l	$\overline{q}$	q
load "0" (reset)	H	H	↑	l	l	L	H
load "1" (set)	H	H	↑	h	h	H	L
hold "no change"	H	H	↑	l	h	q	$\overline{q}$

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition.
X = don't care
↑ = LOW-to-HIGH CP transition

DC CHARACTERISTICS FOR 74LV109

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: standard
I_{CC} category: flip-flops

AC CHARACTERISTICS FOR 74LV109

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay nCP to nQ, $n\overline{Q}$	–	90	–	–	–	ns	1.2	Fig.6
		–	31	58	–	70		2.0	
		–	23	43	–	51		2.7	
		–	17*	34	–	41		3.0 to 3.6	
t_{PLH}	propagation delay $n\overline{S}_D$ to nQ	–	55	–	–	–	ns	1.2	Fig.7
		–	19	36	–	44		2.0	
		–	14	26	–	33		2.7	
		–	10*	21	–	26		3.0 to 3.6	
t_{PHL}	propagation delay $n\overline{S}_D$ to $n\overline{Q}$	–	75	–	–	–	ns	1.2	Fig.7
		–	26	46	–	60		2.0	
		–	19	36	–	44		2.7	
		–	14*	29	–	35		3.0 to 3.6	
t_{PHL}	propagation delay $n\overline{R}_D$ to nQ	–	75	–	–	–	ns	1.2	Fig.7
		–	26	46	–	60		2.0	
		–	19	36	–	44		2.7	
		–	14*	29	–	35		3.0 to 3.6	
t_{PLH}	propagation delay $n\overline{R}_D$ to $n\overline{Q}$	–	70	–	–	–	ns	1.2	Fig.7
		–	24	44	–	54		2.0	
		–	18	33	–	40		2.7	
		–	13*	26	–	32		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC CHARACTERISTICS FOR 74LV109 *(Continued)*

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_W	clock pulse width HIGH or LOW	34	12	–	41	–	ns	2.0	Fig.6
		25	9	–	30	–		2.7	
		20	7*	–	24	–		3.0 to 3.6	
t_W	set or reset pulse width HIGH or LOW	34	9	–	41	–	ns	2.0	Fig.7
		25	6	–	30	–		2.7	
		20	5*	–	24	–		3.0 to 3.6	
t_{rem}	removal time $n\overline{S}_D$, $n\overline{R}_D$ to nCP	–	35	–	–	–	ns	1.2	Fig.7
		24	12	–	29	–		2.0	
		18	9	–	21	–		2.7	
		14	7*	–	17	–		3.0 to 3.6	
t_{su}	set-up time nJ, n$\overline{K}$ to nCP	–	30	–	–	–	ns	1.2	Fig.6
		22	10	–	26	–		2.0	
		16	8	–	19	–		2.7	
		13	6*	–	15	–		3.0 to 3.6	
t_h	hold time nJ, n$\overline{K}$ to nCP	–	−5	–	–	–	ns	1.2	Fig.6
		5	−2	–	5	–		2.0	
		5	−1	–	5	–		2.7	
		5	0*	–	5	–		3.0 to 3.6	
f_{max}	maximum clock pulse frequency	14	40	–	12	–	MHz	2.0	Fig.6
		19	58	–	16	–		2.7	
		24	70*	–	20	–		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

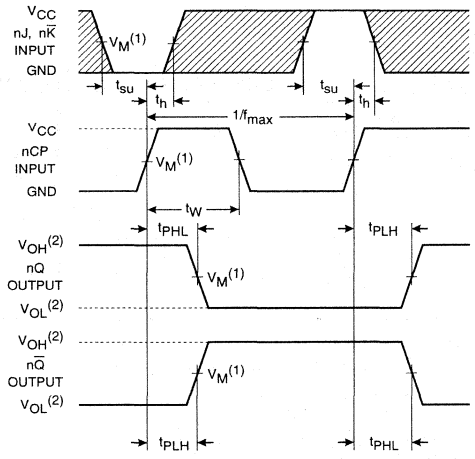


Fig.6 Waveforms showing the clock (nCP) to output (nQ, $n\overline{Q}$) propagation delays, the clock pulse width, the nJ, $n\overline{K}$ to nCP set-up, the nCP to nJ, $n\overline{K}$ hold times and the maximum clock pulse frequency.

Note to Fig.6: The shaded areas indicate when the input is permitted to change for predictable output performance.

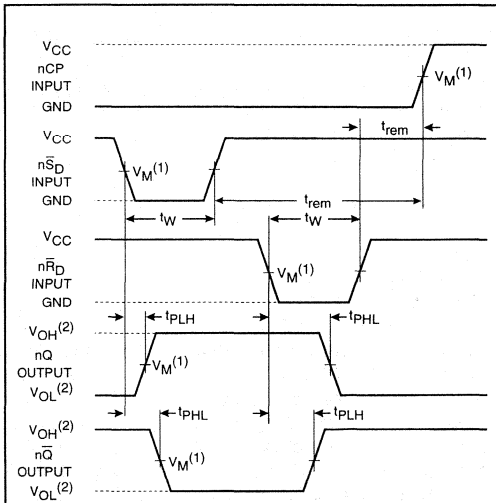


Fig.7 Waveforms showing the set ($n\overline{S}_D$) and reset ($n\overline{R}_D$) input to output (nQ, $n\overline{Q}$) propagation delays, the set and reset pulse widths and the $n\overline{R}_D$, $n\overline{S}_D$ to nCP removal time.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

Dual retriggerable monostable multivibrator with reset

74LV123

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **DC triggered from active HIGH or active LOW inputs**
- **Retriggerable for very long pulses up to 100% duty factor**
- **Direct reset terminates output pulses**
- **Schmitt-trigger action on all inputs except for the reset input**
- **Output capability: standard (except for nR_{EXT} / C_{EXT}**
- **I_{CC} category: MSI**

DESCRIPTION

The 74LV123 is a low-voltage Si-gate CMOS device and is pin and function compatible with the 74HC/HCT123.

The 74LV123 is a dual retriggerable monostable multivibratorwith output pulse width control by three methods. The basic pulse time is programmed by selection of an external resistor (R_{EXT}) and capacitor (C_{EXT}). are normally connected as shown in Fig. 6. Once triggered, the basic output pulse width may be extended by retriggering the gated active LOW-going edge input ($n\overline{A}$) or the active HIGH-going edge input (nB). By repeating this process, the output pulse period (nQ = HIGH, $n\overline{Q}$ = LOW) can be made as long as desired. Alternatively an output delay can be terminated at any time by a LOW-going edge on input $n\overline{R}_D$, which also inhibits the triggering. An internal connection from $n\overline{R}_D$ to the input gates makes it possible to trigger the circuit by a positive-going signal at input $n\overline{R}_D$ as shown in

(continued on next page)

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay $n\overline{A}$, nB to nQ, $n\overline{Q}$ $n\overline{R}_D$ to nQ, $n\overline{Q}$	C_L = 15 pF V_{CC} = 3.3 V R_{EXT} = 5 kΩ C_{EXT} = 0 pF	16 13	ns ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	V_{CC} = 3.3 V notes 1 and 2	17	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV123N	16	DIL	plastic	DIL16/SOT38Z
74LV123D	16	SO	plastic	SO16/SOT109A
74LV123DB	16	SSOP	plastic	SSOP16/SOT338
74LV123PW	16	TSSOP	plastic	TSSOP16/SOT403

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 9	$1\overline{A}$, $2\overline{A}$	trigger inputs (negative-edge triggered)
2, 10	1B, 2B	trigger inputs (positive-edge triggered)
3, 11	$1\overline{R}_D$, $2\overline{R}_D$	direct reset LOW and trigger action at positive edge
4, 12	$1\overline{Q}$, $2\overline{Q}$	outputs (active LOW)
7	$2R_{EXT}/C_{EXT}$	external resistor/capacitor connection
8	GND	ground (0 V)
13, 5	1Q, 2Q	outputs (active HIGH)
14, 6	$1C_{EXT}$, $2C_{EXT}$	external capacitor connection
15	$1R_{EXT}/C_{EXT}$	external resistor/capacitor connection
16	V_{CC}	positive supply voltage

function table. Figs 7 and 8 illustrate pulse control by retriggering and early reset. The basic output pulse width is essentially determined by the values of the external timing components R_{EXT} and C_{EXT}. For pulse widths, when C_{EXT} < 10 000 pF, see Fig. 9. When C_{EXT} > 10 000 pF, the typical output pulse width is defined as: $t_W = 0.45 \times R_{EXT} \times C_{EXT}$ (typ.), where, t_W = pulse width in ns; R_{EXT}= external resistor in KΩ; and C_{EXT}= external capacitor in pF. Schmitt-trigger action in the $n\overline{A}$ and nB inputs, makes the circuit highly tolerant to slower input rise and fall times.

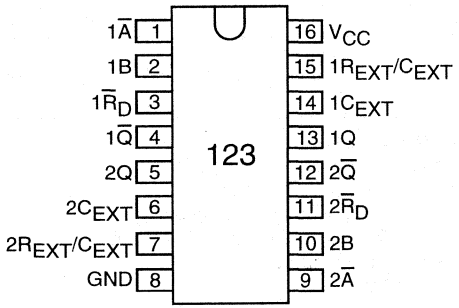


Fig.1 Pin configuration.

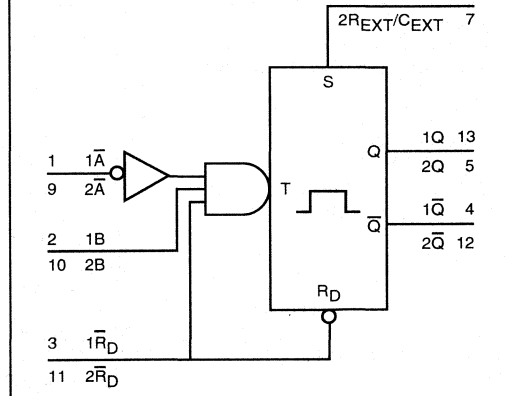


Fig.2 Logic symbol.

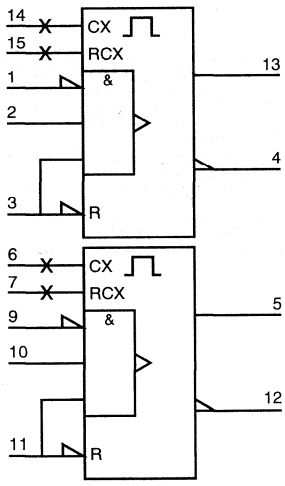


Fig.3 IEC logic symbol.

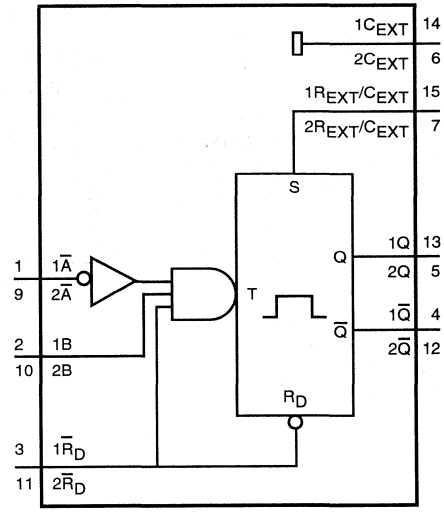


Fig.4 Functional diagram

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Output capability: bus driver**
- **I_{CC} category: MSI**

DESCRIPTION

The 74LV125 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT125.

The 74LV125 consists of four non-inverting buffers/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable input ($n\overline{OE}$). A HIGH at $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state.

FUNCTION TABLE

INPUTS		OUTPUT
$n\overline{OE}$	nA	nY
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 15 pF V_{CC} = 3.3 V	9	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per buffer	V_{CC} = 3.3 V notes 1 and 2	22	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV125N	14	DIL	plastic	DIL14/SOT27
74LV125D	14	SO	plastic	SO14/SOT108A
74LV125DB	14	SSOP	plastic	SSOP14/SOT337
74LV125PW	14	TSSOP	plastic	TSSOP14/SOT402

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	$1\overline{OE}$ to $4\overline{OE}$	output enable inputs (active LOW)
2, 5, 9, 12	1A to 4A	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

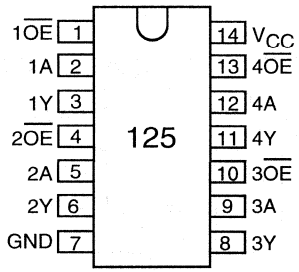


Fig.1 Pin configuration.

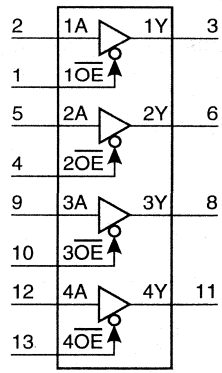


Fig.2 Logic symbol.

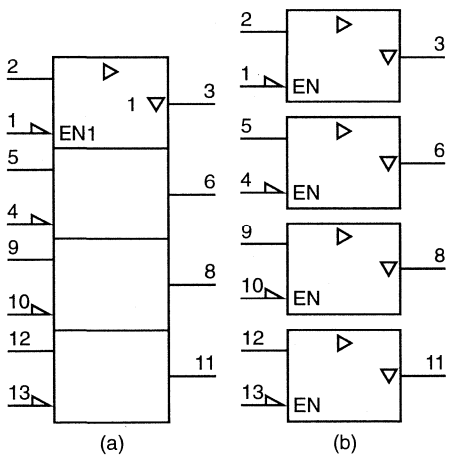


Fig.3 IEC Logic symbol.

DC CHARACTERISTICS FOR 74LV125

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LV125

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay nA to nY	–	55	–	–	–	ns	1.2	Fig.4
		–	19	36	–	44		2.0	
		–	14	26	–	33		2.7	
		–	10*	21	–	26		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time $n\overline{OE}$ to nY	–	75	–	–	–	ns	1.2	Fig.5
		–	26	49	–	60		2.0	
		–	19	36	–	44		2.7	
		–	14*	29	–	35		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time $n\overline{OE}$ to nY	–	65	–	–	–	ns	1.2	Fig.5
		–	24	40	–	49		2.0	
		–	18	32	–	37		2.7	
		–	14*	26	–	30		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

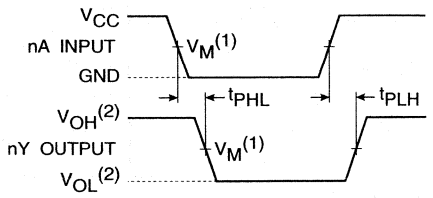


Fig.4 Waveforms showing the input (nA) to output (nY) propagation delays.

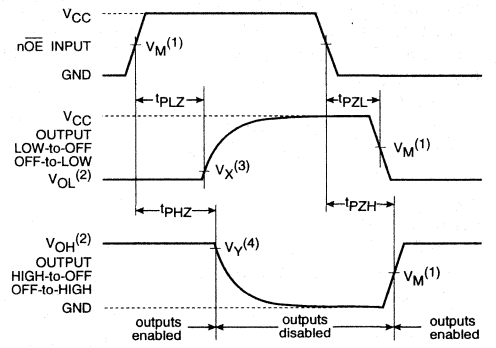
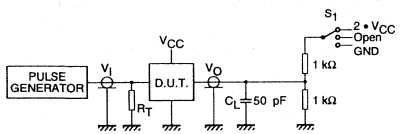


Fig.5 Waveforms showing the 3-state enable and disable times.



Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.6 Load circuitry for switching times.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Output capability: bus driver**
- **I_{CC} category: MSI**

DESCRIPTION

The 74LV126 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT126.

The 74LV126 consists of four non-inverting buffers/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable input (nOE). A LOW at nOE causes the outputs to assume a high impedance OFF-state.

FUNCTION TABLE

INPUTS		OUTPUT
nOE	nA	nY
H	L	L
H	H	H
L	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 15 pF V_{CC} = 3.3 V	9	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per buffer	V_{CC} = 3.3 V notes 1 and 2	23	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV126N	14	DIL	plastic	DIL14/SOT27
74LV126D	14	SO	plastic	SO14/SOT108A
74LV126DB	14	SSOP	plastic	SSOP14/SOT337
74LV126PW	14	TSSOP	plastic	TSSOP14/SOT402

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	1OE to 4OE	output enable inputs (active HIGH)
2, 5, 9, 12	1A to 4A	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

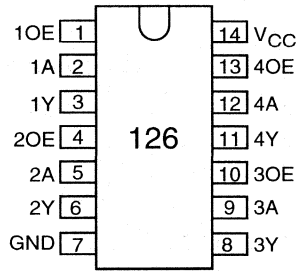


Fig.1 Pin configuration.

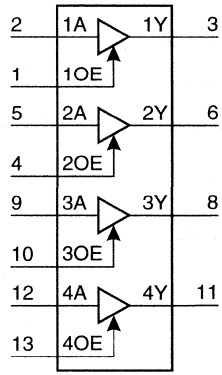


Fig.2 Logic symbol.

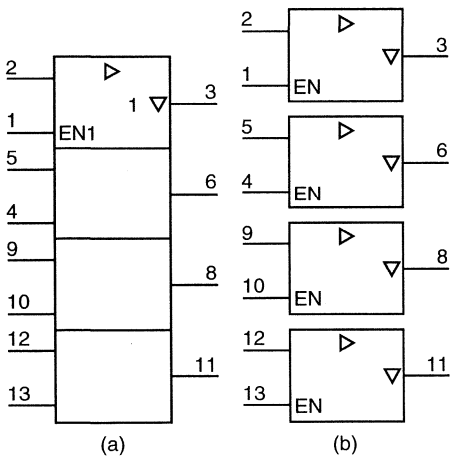


Fig.3 IEC Logic symbol.

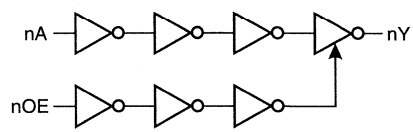


Fig.4 Logic diagram (one buffer).

DC CHARACTERISTICS FOR 74LV126

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LV126

GND = 0 V; $t_r = t_f \leq 2.5$ ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay nA to nY	–	55	–	–	–	ns	1.2	Fig.5
		–	19	36	–	44		2.0	
		–	14	26	–	33		2.7	
		–	10*	21	–	26		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time nOE to nY	–	75	–	–	–	ns	1.2	Fig.6
		–	26	49	–	60		2.0	
		–	19	36	–	44		2.7	
		–	14*	29	–	35		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time nOE to nY	–	65	–	–	–	ns	1.2	Fig.6
		–	24	40	–	49		2.0	
		–	18	32	–	37		2.7	
		–	14*	26	–	30		3.0 to 3.6	

Notes: All typical values are measured at T_{amb} = 25 °C.
* Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

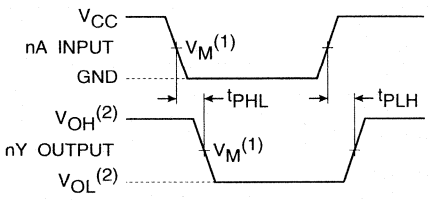


Fig.5 Waveforms showing the input (nA) to output (nY) propagation delays.

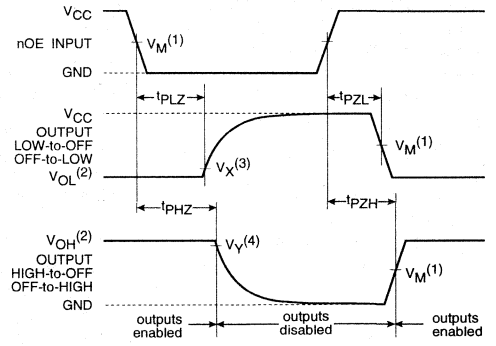
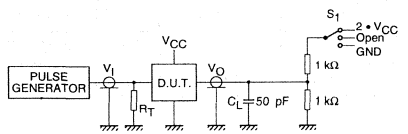


Fig.6 Waveforms showing the 3-state enable and disable times.



Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.7 Load circuitry for switching times.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

eFEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Output capability: standard**
- **I_{CC} category: SSI**

APPLICATIONS

- **Wave and pulse shapers**
- **Astable multivibrators**
- **Monostable multivibrators**

DESCRIPTION

The 74LV132 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT132.

The 74LV132 contains four 2–input NAND gates which accept standard input signals. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.
The gate switches at different points for positive and negative–going signals. The difference between the positive voltage V_{T+} and the negative voltage V_{T-} is defined as the hysteresis voltage V_H.

FUNCTION TABLE

INPUT		OUTPUT
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF; V_{CC} = 3.3 V	10	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	24	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV132N	14	DIL	plastic	DIL14/SOT27
74LV132D	14	SO	plastic	SO14/SOT108A
74LV132DB	14	SSOP	plastic	SSOP14/SOT337
74LV132PW	14	TSSOP	plastic	TSSOP14/SOT402

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

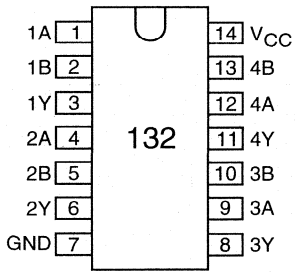


Fig.1 Pin configuration.

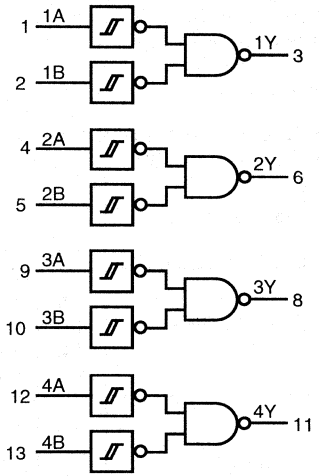


Fig.2 Logic symbol.

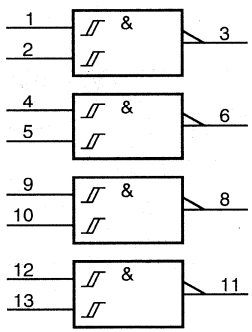


Fig.3 IEC Logic symbol.

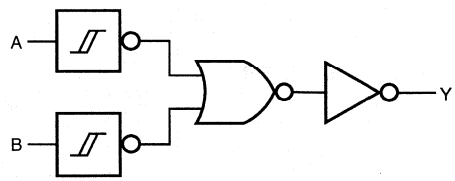


Fig.4 Logic diagram (one Schmitt-trigger).

DC CHARACTERISTICS FOR 74LV132

For the DC characteristics see chapter "LV family characteristics", section "Family specifications". Transfer characteristics are given below.
Output capability: standard
I_{CC} category: SSI

TRANSFER CHARACTERISTICS FOR 74LV132

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
V_{T+}	positive–going threshold	–	0.70	–	–	–	V	1.2	Figs 5 and 6
		0.8	1.10	1.4	0.8	1.4		2.0	
		1.0	1.45	2.0	1.0	2.0		2.7	
		1.2	1.60	2.2	1.2	2.2		3.0	
		1.5	1.95	2.4	1.5	2.4		3.6	
V_{T-}	negative–going threshold	–	0.34	–	–	–	V	1.2	Figs 5 and 6
		0.3	0.65	0.9	0.3	0.9		2.0	
		0.4	0.90	1.4	0.4	1.4		2.7	
		0.6	1.05	1.5	0.6	1.5		3.0	
		0.8	1.30	1.8	0.8	1.8		3.6	
V_H	hysteresis ($V_{T+} - V_{T-}$)	–	0.30	–	–	–	V	1.2	Figs 5 and 6
		0.2	0.55	0.8	0.2	0.8		2.0	
		0.3	0.60	1.1	0.3	1.1		2.7	
		0.4	0.65	1.2	0.4	1.2		3.0	
		0.4	0.70	1.2	0.4	1.2		3.6	

Note: All typical values are measured at T_{amb} = 25 °C.
The V_{IH} and V_{IL} from the DC family characteristics are superseeded by the V_{T+} and V_{T-}.

AC characteristics for 74LV132

GND = 0 V; $t_r = t_f \leq 2.5$ ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	–	65	–	–	–	ns	1.2	Fig.10
		–	22	43	–	51		2.0	
		–	16	31	–	38		2.7	
		–	12*	25	–	30		3.0 to 3.6	

Notes: All typical values are measured at T_{amb} = 25 °C.
* Typical values are measured at V_{CC} = 3.3 V.

TRANSFER CHARACTERISTIC WAVEFORMS

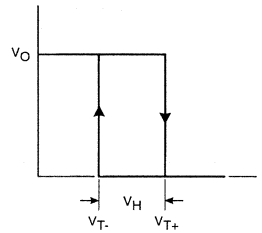


Fig.5 Transfer characteristic.

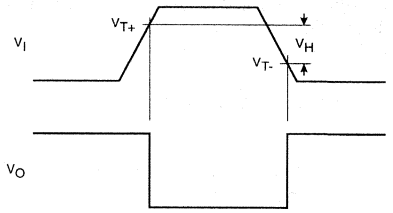


Fig. 6 Waveforms showing the definition of V_{T+}, V_{T-} and V_H; where V_{T+} and V_{T-} are between limits of 20% and 70%.

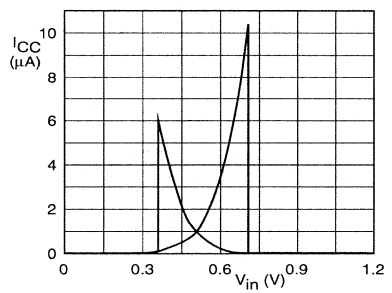


Fig.7 Typical LV132 transfer characteristics; V_{CC} = 1.2 V.

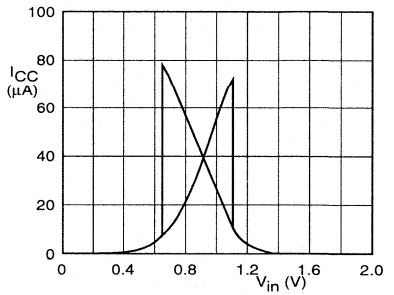


Fig.8 Typical LV132 transfer characteristics; V_{CC} = 2.0 V.

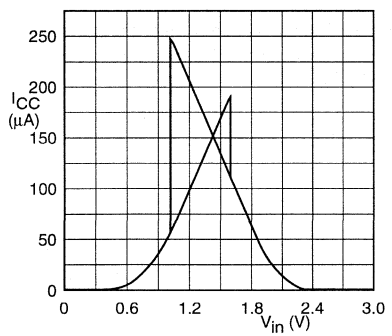


Fig.9 Typical LV132 transfer characteristics; V_{CC} = 3.0 V.

AC WAVEFORMS

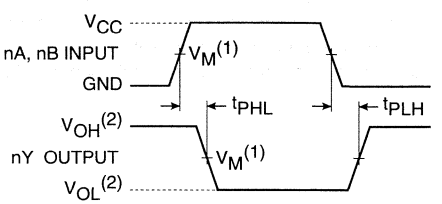


Fig.10 Waveforms showing the input (nA, nB) to output (nY) propagation delays.

Notes to the AC waveforms

(1) V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
$V_M = 0.5 \cdot V_{CC}$ at V_{CC} < 2.7 V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

APPLICATION INFORMATION

The slow input rise and fall times cause additional power dissipation, this can be calculated using the following formula:

$P_{ad} = f_i \times (t_r \times I_{CCa} + t_f \times I_{CCa}) \times V_{CC}$.

Where:

P_{ad} = additional power dissipation (μW)
f_i = input frequency (MHz)
t_r = input rise time (ns); 10% – 90%
t_f = input fall time (ns); 10% – 90%
I_{CCa} = average additional supply current (μA)

Average I_{CCa} differs with positive or negative input transitions, as shown in fig.11.

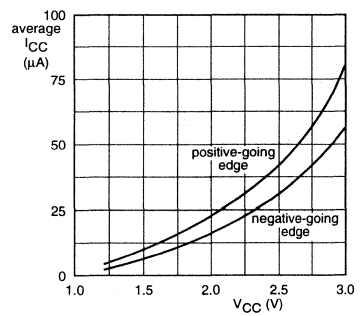


Fig.11 Average I_{CC} for LV Schmitt-trigger devices; linear change of V_i between 0.1 V_{CC} to 0.9 V_{CC}.

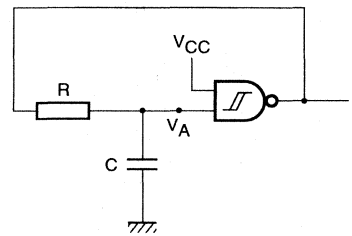


Fig.12 Relaxation oscillator using the LV132.

Note to the application information
All values given are typical unless otherwise specified.

Note to Fig.12

$$f = \frac{1}{T} \approx \frac{1}{0.8RC}$$

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Demultiplexing capability**
- **Multiple input enable for easy expansion**
- **Ideal for memory chip select decoding**
- **Active LOW mutually exclusive outputs**
- **Output capability: standard**
- **I_{CC} category: MSI**

DESCRIPTION

The 74LV138 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT138.

The 74LV138 accepts three binary weighted address inputs (A_0, A_1, A_2) and when enabled, provide 8 mutually exclusive active LOW outputs ($\overline{Y}_0$ to $\overline{Y}_7$).
The '138' features three enable inputs: two active LOW ($\overline{E}_1$ and $\overline{E}_2$ and one active HIGH (E_3). Every output will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH.

This multiple enable function allows easy parallel expansion of the '138' to a 1-of-32 (5 lines to 32 lines) decoder with just four '138' ICs and one inverter. The '138' can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Unused enable inputs must be permanently tied to their appropriate active HIGH or LOW state.

The '138' is identical to the '238' but has non-inverting (true) outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay An to $\overline{Y}n$, E3 to $\overline{Y}n$, $\overline{E}n$ to $\overline{Y}n$	C_L = 15 pF V_{CC} = 3.3 V	12 14	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per package	V_{CC} = 3.3 V notes 1 and 2	45	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV138N	14	DIL	plastic	DIL14/SOT27
74LV138D	14	SO	plastic	SO14/SOT108A
74LV138DB	14	SSOP	plastic	SSOP14/SOT337
74LV138PW	14	TSSOP	plastic	TSSOP14/SOT402

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	A_0 to A_2	address inputs
4, 5	$\overline{E}_1$, $\overline{E}_2$	enable inputs (active LOW)
6	E_3	enable inputs (active HIGH)
15, 14, 13, 12, 11, 10, 9, 7	$\overline{Y}_0$ to $\overline{Y}_7$	outputs
8	GND	ground (0 V)
16	V_{CC}	positive supply voltage

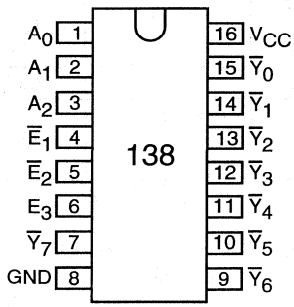


Fig.1 Pin configuration.

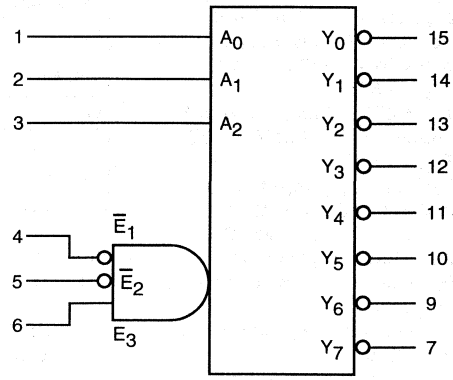


Fig.2 Logic diagram.

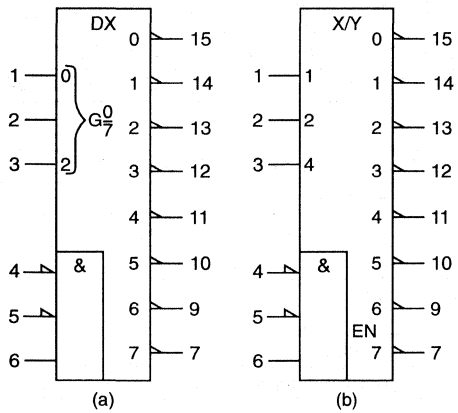


Fig.3 IEC logic symbol.

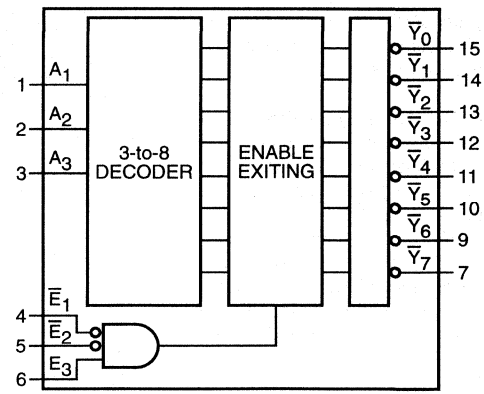


Fig.4 Functional diagram.

FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	$\overline{Y}_4$	$\overline{Y}_5$	$\overline{Y}_6$	$\overline{Y}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care

DC CHARACTERISTICS FOR 74LV138

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LV138

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay A_n to $\overline{Y}_n$	–	75	–	–	–	ns	1.2	Fig.5
		–	26	49	–	60		2.0	
		–	19	36	–	44		2.7	
		–	14*	29	–	35		3.0 to 3.6	
t_{PHL}/t_{PLH}	propagation delay E_3 to $\overline{Y}_n$	–	85	–	–	–	ns	1.2	Fig.5
		–	29	56	–	66		2.0	
		–	21	41	–	49		2.7	
		–	16*	33	–	39		3.0 to 3.6	
t_{PHL}/t_{PLH}	propagation delay $\overline{E}_n$ to $\overline{Y}_n$	–	85	–	–	–	ns	1.2	Fig.6
		–	29	56	–	66		2.0	
		–	21	41	–	49		2.7	
		–	16*	33	–	39		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

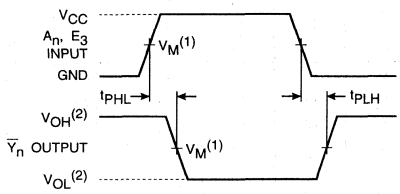


Fig. 5 Waveforms showing the address input (An) and enable input (E_3) to output ($\overline{Y}n$) propagation delays.

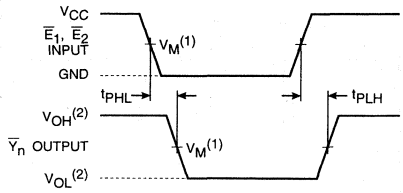


Fig. 6 Waveforms showing the enable input ($\overline{E}_n$) to output ($\overline{Y}n$) propagation delays.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

Dual 2-to-4 line decoder/demultiplexer — 74LV139

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Demultiplexing capability**
- **Two independent 2-to-4 decoders**
- **Multifunction capability**
- **Active LOW mutually exclusive outputs**
- **Output capability: standard**
- **I_{CC} category: MSI**

APPLICATIONS

- **Memory decoding or data-routing**
- **Code conversion**

DESCRIPTION

The 74LV139 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT139.

The 74LV139 is a dual 2-to-4 line decoder/demultiplexer. This device has two independent decoders, each accepting two binary weighted inputs (nA_0 and nA_1) and providing four mutually exclusive active LOW outputs ($n\overline{Y}_0$ to $n\overline{Y}_3$). Each decoder has an active LOW enable input ($n\overline{E}$).
When $n\overline{E}$ is HIGH, every output is forced HIGH. The enable can be used as the data input for a 1-to-4 demultiplexer application.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA_n to $n\overline{Y}_n$, $n\overline{E}$ to $n\overline{Y}_n$	C_L = 15 pF V_{CC} = 3.3 V	11 10	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per multiplexer	V_{CC} = 3.3 V notes 1 and 2	42	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV139N	16	DIL	plastic	DIL16/SOT38Z
74LV139D	16	SO	plastic	SO16/SOT109A
74LV139DB	16	SSOP	plastic	SSOP16/SOT338
74LV139PW	16	TSSOP	plastic	TSSOP16/SOT403

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$1\overline{E}$, $2\overline{E}$	enable inputs (active LOW)
2, 3	$1A_0$, $1A_1$	address inputs
4, 5, 6, 7	$1\overline{Y}_0$ to $1\overline{Y}_3$	outputs (active LOW)
8	GND	ground (0 V)
12, 11, 10, 9	$2\overline{Y}_0$ to $2\overline{Y}_3$	outputs (active LOW)
14, 13	$2A_0$, $2A_1$	address inputs
16	V_{CC}	positive supply voltage

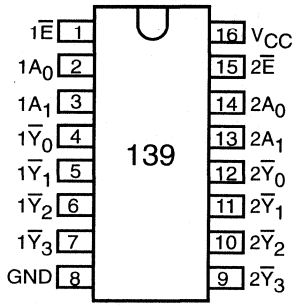


Fig.1 Pin configuration.

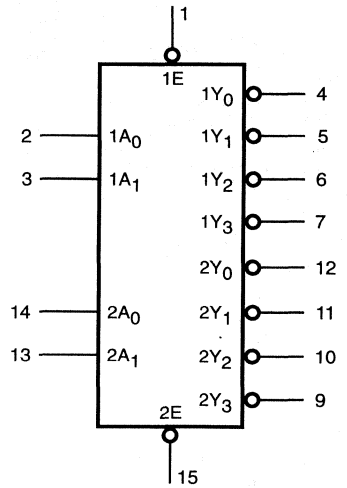


Fig.2 Logic diagram.

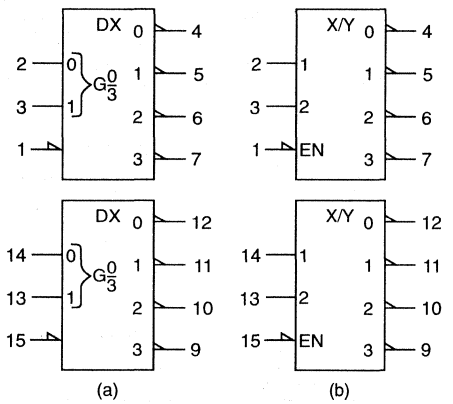


Fig.3 IEC logic symbol.

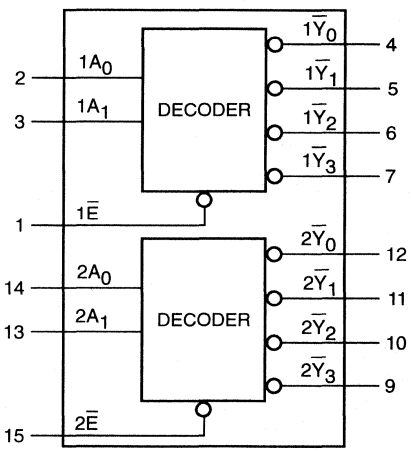


Fig.4 Functional diagram.

FUNCTION TABLE

INPUTS			OUTPUTS			
$n\overline{E}$	nA_0	nA_1	$n\overline{Y}_0$	$n\overline{Y}_1$	$n\overline{Y}_2$	$n\overline{Y}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care

DC CHARACTERISTICS FOR 74LV139

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LV139

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		-40 to +85			-40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay nA_n to $\overline{Y}_n$	–	70	–	–	–	ns	1.2	Fig.5
		–	24	44	–	54		2.0	
		–	18	33	–	40		2.7	
		–	13*	26	–	32		3.0 to 3.6	
t_{PHL}/t_{PLH}	propagation delay $n\overline{E}$ to $\overline{Y}_n$	–	60	–	–	–	ns	1.2	Fig.6
		–	20	39	–	46		2.0	
		–	15	29	–	34		2.7	
		–	11*	23	–	27		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

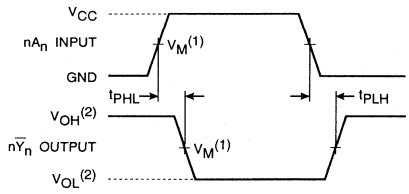


Fig. 5 Waveforms showing the address input (nA_n) to output ($n\overline{Y}n$) propagation delays.

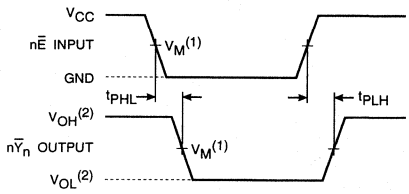


Fig. 6 Waveforms showing the enable input ($n\overline{E}$) to output ($n\overline{Y}_n$) propagation delays.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Non-inverting outputs**
- **Separate enable for each output**
- **Common select inputs**
- **Permits multiplexing from n lines to 1 line**
- **Enable line provided for cascading (n lines to 1 line)**
- **Output capability: standard**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74LV153 is a low-voltage CMOS device and is pin and function compatible with 74HC/HCT153.

The 74LV153 is a dual 4-input multiplexer which select 2 bits of data from up to four sources selected by common data select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active LOW output enable inputs ($1\overline{E}$, $2\overline{E}$) which can be used to strobe the outputs independently. The outputs (1Y, 2Y) are forced LOW when the corresponding output enable inputs are HIGH. The "153" is the logic implementation of a 2-pole, 4-position switch, where the position of the switch, is determined by the logic levels applied to S_0 and S_1. The logic equations for the outputs are:

$$1Y = 1\overline{E}.(1I_0.\overline{S}_1.\overline{S}_0+1I_1.\overline{S}_1.S_0 +1I_2.S_1.\overline{S}_0+1I_3.S_1.S_0)$$

$$2Y = 2\overline{E}.(2I_0.\overline{S}_1.\overline{S}_0+2I_1.\overline{S}_1.S_0 +2I_2.S_1.\overline{S}_0+2I_3.S_1.S_0)$$

(continued on next page)

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay $1I_n$, $2I_n$ to nY Sn to nY $n\overline{E}$ to nY	C_L = 15 pF V_{CC} = 3.3 V	 14 15 10	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	70	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV153N	16	DIL	plastic	DIL16/SOT38Z
74LV153D	16	SO	plastic	SO16/SOT109A
74LV153DB	16	SSOP	plastic	SSOP16/SOT338
74LV153PW	16	TSSOP	plastic	TSSOP16/SOT403

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$1\overline{E}$, $2\overline{E}$	output enable inputs (active LOW)
14, 2	S_0, S_1	common data select inputs
6, 5, 4, 3	$1I_0$ to $1I_3$	data inputs from source 1
7	1Y	multiplexer output from source 1
8	GND	ground (0 V)
9	2Y	multiplexer output from source 2
10, 11, 12, 13	$2I_0$, $2I_3$	data inputs from source 2
16	V_{CC}	positive supply voltage

The "153" can be used to move data to a common output bus from a group of registers. The state of the select inputs would determine the particular register from which the data came. An alternative application is a function generator. The device can generate two functions or three variables. This is useful for implementing highly irregular random logic.

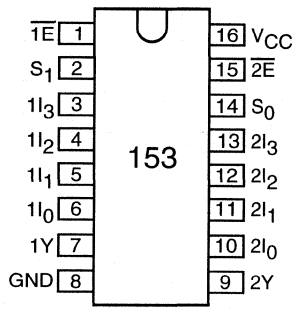


Fig.1 Pin configuration

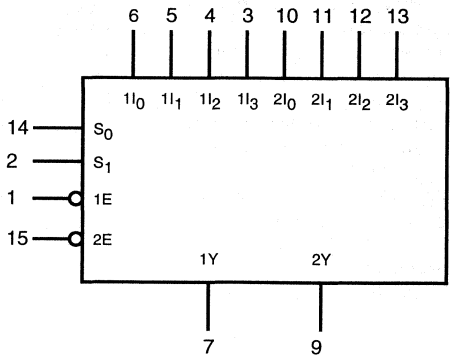


Fig.2 Logic symbol

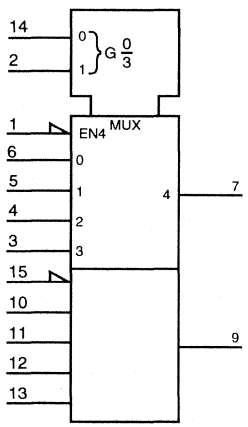


Fig.3 IEC Logic symbol

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Output capability: standard**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74LV157 is a low-voltage CMOS device and is pin and function compatible with 74HC/HCT157.

The 74LV157 is a quad 2-input multiplexer which selects 4 bits of data from two sources under the control of a common data select input (S).
The four outputs present the selected data in the true (non-inverted) form. The enable input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs (1Y to 4Y) are forced LOW regardless of all other input conditions.
Moving the data from two groups of registers to four common output buses is a common use of the "157". The state of the common data select input (S) determines the particular register from which the data comes. It can also be used as function generator.

The device is useful for implementing highly irregular logic by generating any four of the 16 different functions of two variables with one variable common.

The "157" is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nI_0, nI_1 to nY $\overline{E}$ to nY S to nY	C_L = 15 pF V_{CC} = 3.3 V	 10 11 12	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	70	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV157N	16	DIL	plastic	DIL16/SOT38Z
74LV157D	16	SO	plastic	SO16/SOT109A
74LV157DB	16	SSOP	plastic	SSOP16/SOT338
74LV157PW	16	TSSOP	plastic	TSSOP16/SOT403

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	S	common data select input
2, 5, 11, 14	$1I_0$ to $4I_0$	data inputs from source 0
3, 6, 10, 13	$1I_1$ to $4I_1$	data inputs from source 1
4, 7, 9, 12	1Y to 4Y	multiplexer outputs
8	GND	ground (0 V)
15	$\overline{E}$	enable input (active LOW)
16	V_{CC}	positive supply voltage

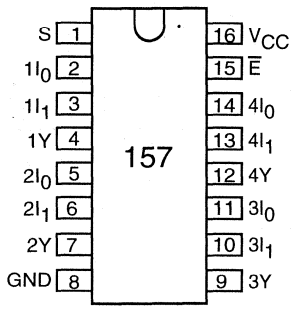


Fig.1 Pin configuration

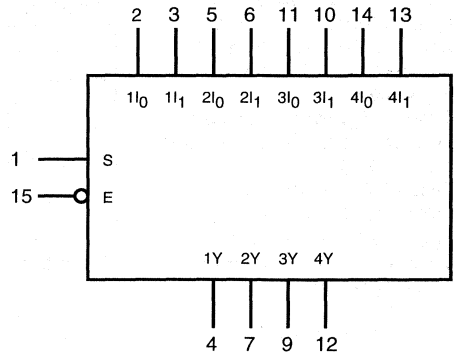


Fig.2 Logic symbol

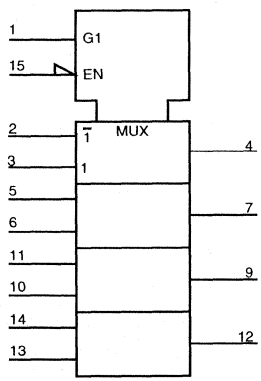


Fig.3 IEC Logic symbol

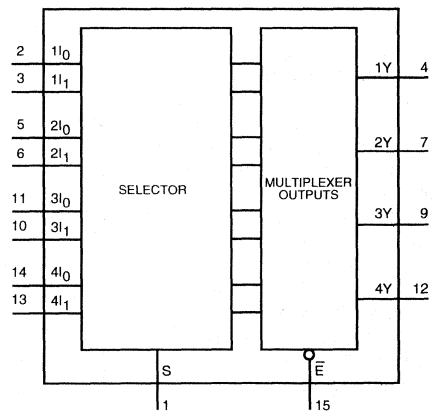


Fig.4 Functional diagram

DC CHARACTERISTICS FOR 74LV157

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LV157

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay nI_0 to nY; nI_1 to nY	–	65	–	–	–	ns	1.2	Fig.6
		–	22	43	–	51		2.0	
		–	16	31	–	38		2.7	
		–	12*	25	–	30		3.0 to 3.6	
t_{PHL}/t_{PLH}	propagation delay $\overline{E}$ to nY	–	70	–	–	–	ns	1.2	Fig.5
		–	24	44	–	54		2.0	
		–	18	33	–	40		2.7	
		–	13*	26	–	32		3.0 to 3.6	
t_{PHL}/t_{PLH}	propagation delay S to nY	–	75	–	–	–	ns	1.2	Fig.6
		–	26	49	–	60		2.0	
		–	19	36	–	44		2.7	
		–	14*	29	–	35		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

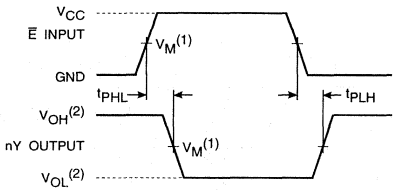


Fig.5 Waveforms showing the enable input ($\overline{E}$) to output (nY) propagation delays and the output transition times.

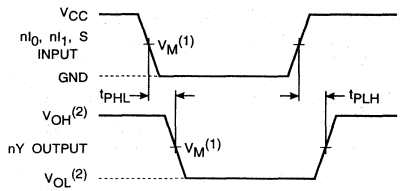


Fig.6 Waveforms showing the data inputs (nI_n) and common data select input (S) to output (nY) propagation delays.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

8-bit serial-in/parallel-out shift register | 74LV164

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Gated serial data inputs**
- **Asynchronous master reset**
- **Output capability: standard**
- **I_{CC} category: MSI**

DESCRIPTION

The 74LV164 is a low-voltage Si-gate CMOS device and is pin and function compatible with the 74HC/HCT164.

The 74LV164 is an 8-bit edge-triggered shift register with serial data entry and an output from each of the eight stages.
Data is entered serially through one of two inputs (D_{sa} or D_{sb}); either input can be used as an active HIGH enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied HIGH.

Data shifts one place to the right on each LOW-to-HIGH transition of the clock (CP) input and enters into Q_0, which is the logical AND of the two data inputs (D_{sa}, D_{sb}) that existed one set-up time prior to the rising clock edge.

A LOW on the master reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all outputs LOW.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay CP to Q_n $\overline{MR}$ to Q_n	C_L = 15 pF V_{CC} = 3.3 V	12 11	ns ns
f_{max}	maximum clock frequency		78	MHz
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per gate	V_{CC} = 3.3 V notes 1 and 2	40	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV164N	14	DIL	plastic	DIL14/SOT27
74LV164D	14	SO	plastic	SO14/SOT108A
74LV164DB	14	SSOP	plastic	SSOP14/SOT337
74LV164PW	14	TSSOP	plastic	TSSOP14/SOT402

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2	D_{sa}, D_{sb}	data inputs
3, 4, 5, 6, 10, 11, 12, 13	Q_0 to Q_7	outputs
7	GND	ground (0 V)
8	CP	clock input (LOW-to-HIGH, edge-triggered)
9	$\overline{MR}$	master reset input (active LOW)
14	V_{CC}	positive supply voltage

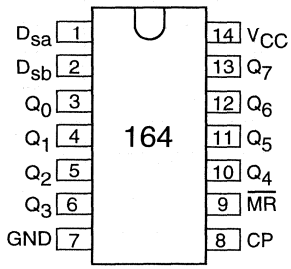


Fig.1 Pin configuration.

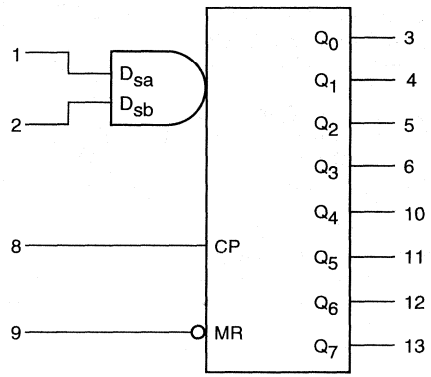


Fig.2 Logic symbol.

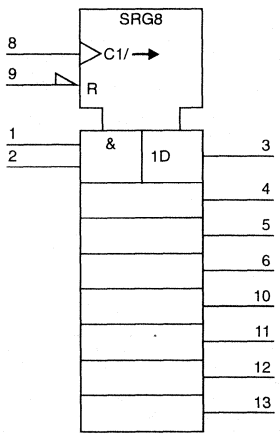


Fig.3 IEC logic symbol.

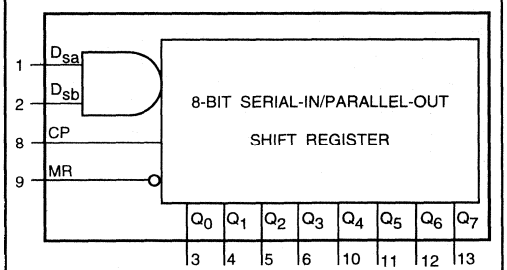


Fig.4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS				OUTPUTS	
	$\overline{MR}$	CP	D_{sa}	D_{sb}	Q_0	$Q_1 - Q_7$
reset (clear)	L	X	x	x	L	L – L
shift	H	↑	l	l	L	$q_0 - q_6$
	H	↑	l	h	L	$q_0 - q_6$
	H	↑	h	l	L	$q_0 - q_6$
	H	↑	h	h	H	$q_0 - q_6$

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
q = lower case letters indicate the state of referenced input one set-up time prior to the LOW-to-HIGH clock transition
↑ = LOW-to-HIGH clock transition

DC CHARACTERISTICS FOR 74LV164

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LV164

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		–40 to +85			–40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	–	75	–	–	–	ns	1.2	Fig.5
		–	26	49	–	60		2.0	
		–	19	36	–	44		2.7	
		–	14*	29	–	35		3.0 to 3.6	
t_{PHL}	propagation delay $\overline{MR}$ to Q_n	–	70	–	–	–	ns	1.2	Fig.6
		–	24	44	–	54		2.0	
		–	18	33	–	40		2.7	
		–	13*	26	–	32		3.0 to 3.6	
t_W	clock pulse width HIGH or LOW	34	9	–	41	–	ns	2.0	Fig.5
		25	6	–	30	–		2.7	
		20	5*	–	24	–		3.0 to 3.6	
t_W	master reset pulse width; LOW	34	10	–	41	–	ns	2.0	Fig.6
		25	8	–	30	–		2.7	
		20	6*	–	24	–		3.0 to 3.6	
t_{rem}	removal time $\overline{MR}$ to CP	–	30	–	–	–	ns	1.2	Fig.6
		19	10	–	24	–		2.0	
		14	8	–	18	–		2.7	
		11	6*	–	14	–		3.0 to 3.6	
t_{su}	set-up time D_{sa}, D_{sb} to CP	–	15	–	–	–	ns	1.2	Fig.7
		22	5	–	26	–		2.0	
		16	4	–	19	–		2.7	
		13	3*	–	15	–		3.0 to 3.6	
t_h	hold time D_{sa}, D_{sb} to CP	–	–10	–	–	–	ns	1.2	Fig.7
		5	–3	–	5	–		2.0	
		5	–2	–	5	–		2.7	
		5	–2*	–	5	–		3.0 to 3.6	
f_{max}	maximum clock pulse frequency	14	40	–	12	–	MHz	2.0	Fig.5
		19	58	–	16	–		2.7	
		24	70*	–	20	–		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

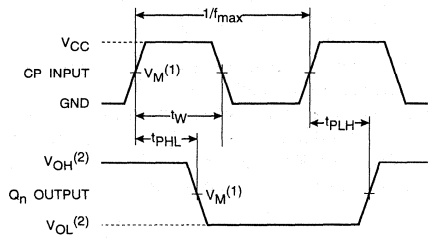


Fig.5 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width and the maximum clock frequency.

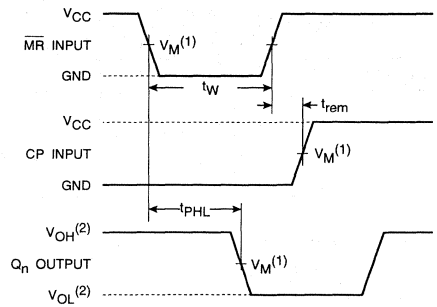


Fig.6 Waveforms showing the master reset ($\overline{MR}$) pulse width, the master reset to ouput (Q_n) propagation delays and the master reset to clock (CP) removal time.

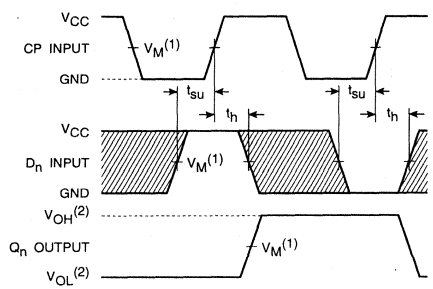


Fig.7 Waveforms showing the data set-up and hold times for D_n inputs.

Note to Fig.7
The shaded areas indicate when the input is permitted to change for predictable output performance.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

8-bit parallel-in/serial-out shift register | 74LV165

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Asynchronous 8-bit parallel load**
- **Synchronous serial input**
- **Output capability: standard**
- **I_{CC} category: MSI**

DESCRIPTION

The 74LV165 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT165.

The 74LV165 is a 8-bit parallel-load or serial-in shift register with complementary serial outputs (Q_7 and $\overline{Q}_7$) available from the last stage. When the parallel load ($\overline{PL}$) input is LOW, parallel data from the D_0 to D_7 inputs are loaded into the register asynchronously. When $\overline{PL}$ is HIGH, data enters the register serially at the D_S input and shifts one place to the right ($Q_0 \rightarrow Q_1 \rightarrow Q_2$, etc.) with each positive-going clock transition. This feature allows parallel-to-serial converter expansion by tying the Q_7 output to the D_S input of the succeeding stage.

The clock input is a gated-OR structure which allows one input to be used as an active LOW clock enable ($\overline{CE}$) input. The pin assignment for the CP and $\overline{CE}$ inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of input $\overline{CE}$ should only take place while CP HIGH for predictable operation. Either the CP or the $\overline{CE}$ should be HIGH before the LOW-to-HIGH transition of $\overline{PL}$ to prevent shifting the data when $\overline{PL}$ is activated.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay $\overline{CE}$, CP to Q_7, $\overline{Q}_7$ PL to Q_7, $\overline{Q}_7$ D_7 to Q_7, $\overline{Q}_7$	C_L = 15 pF V_{CC} = 3.3 V	 18 18 14	ns
f_{MAX}	maximum clock frequency		78	MHz
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per gate	V_{CC} = 3.3 V notes 1 and 2	35	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV165N	16	DIL	plastic	DIL16/SOT38Z
74LV165D	16	SO	plastic	SO16/SOT109A
74LV165DB	16	SSOP	plastic	SSOP16/SOT338
74LV165PW	16	TSSOP	plastic	TSSOP16/SOT403

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{PL}$	asynchronous parallel load input (active LOW)
2	CP	clock input (LOW-to-HIGH edge-triggered)
7	$\overline{Q}_7$	complementary output from the last stage
8	GND	ground (0 V)
9	Q_7	serial output from the last stage
10	D_S	serial data input
11, 12, 13, 14, 3, 4, 5, 6	D_0 to D_7	parallel data inputs
15	$\overline{CE}$	clock enable input (active LOW)
16	V_{CC}	positive supply voltage

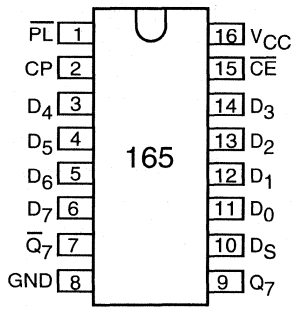


Fig.1 Pin configuration.

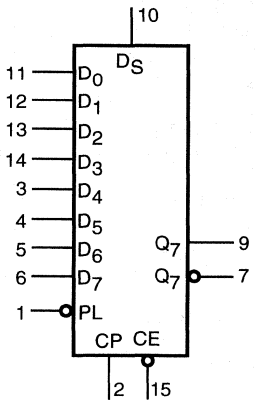


Fig.2 Logic symbol.

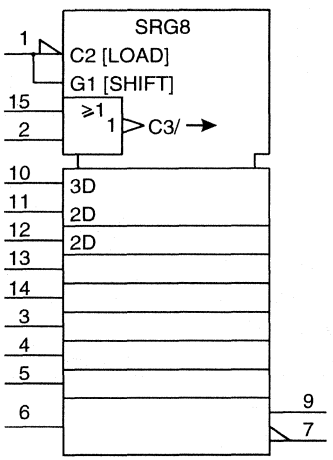


Fig.3 IEC logic symbol.

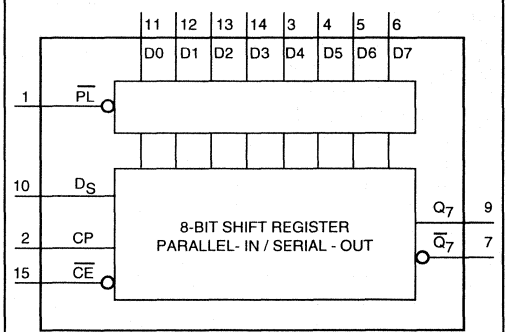


Fig.4 Functional diagram.

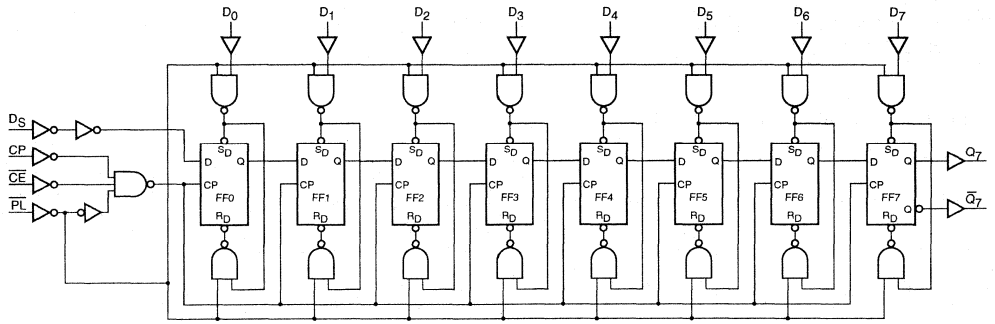


Fig.5 Logic diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS					Qn REGISTERS		OUTPUTS	
	$\overline{PL}$	$\overline{CE}$	CP	D_s	D_0-D_7	Q_0	Q_1-Q_6	Q_7	$\overline{Q}_7$
parallel load	L L	X X	X X	X X	L H	L H	L - L H - H	L H	H L
serial shift	H H	L L	↑ ↑	l h	X X	L H	q_0 - q_5 q_0 - q_5	q_6 q_6	$\overline{q}_6$ $\overline{q}_6$
hold "do nothing"	H	H	X	X	X	q_0	q_1 - q_6	q_7	q_7

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition
X = don't care
↑ = LOW-to-HIGH clock transition

DC CHARACTERISTICS FOR 74LV165

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LV165

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay $\overline{CE}$, CP to Q_7, $\overline{Q}_7$	–	115	–	–	–	ns	1.2	Fig.6
		–	39	75	–	90		2.0	
		–	29	55	–	66		2.7	
		–	22*	44	–	53		3.0 to 3.6	
t_{PHL}/t_{PLH}	propagation delay $\overline{PL}$ to Q_7, $\overline{Q}_7$	–	110	–	–	–	ns	1.2	Fig.7
		–	37	70	–	85		2.0	
		–	28	51	–	63		2.7	
		–	21*	41	–	50		3.0 to 3.6	
t_{PHL}/t_{PLH}	propagation delay D_7 to Q_7, $\overline{Q}_7$	–	90	–	–	–	ns	1.2	Fig.8
		–	31	58	–	70		2.0	
		–	23	43	–	51		2.7	
		–	17*	34	–	41		3.0 to 3.6	
t_W	clock pulse width HIGH or LOW	34	10	–	41	–	ns	2.0	Fig.6
		25	8	–	30	–		2.7	
		20	6*	–	24	–		3.0 to 3.6	
t_W	parallel load pulse width; LOW	34	9	–	41	–	ns	2.0	Fig.7
		25	6	–	30	–		2.7	
		20	5*	–	24	–		3.0 to 3.6	
t_{REM}	removal time $\overline{PL}$ to CP, $\overline{CE}$	–	40	–	–	–	ns	1.2	Fig.7
		26	14	–	31	–		2.0	
		19	10	–	23	–		2.7	
		15	8*	–	18	–		3.0 to 3.6	
t_{su}	set-up time D_S to CP, $\overline{CE}$	–	20	–	–	–	ns	1.2	Fig.9
		22	7	–	26	–		2.0	
		16	5	–	19	–		2.7	
		13	4*	–	15	–		3.0 to 3.6	
t_{su}	set-up time $\overline{CE}$ to CP; CP to $\overline{CE}$	–	30	–	–	–	ns	1.2	Fig.9
		22	10	–	26	–		2.0	
		16	8	–	19	–		2.7	
		13	6*	–	15	–		3.0 to 3.6	
t_{su}	set-up time D_n to $\overline{PL}$	–	40	–	–	–	ns	1.2	Fig.10
		26	14	–	31	–		2.0	
		19	10	–	23	–		2.7	
		15	8*	–	18	–		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC CHARACTERISTICS FOR 74LV165 *(Continued)*

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_h	hold time D_S to CP, $\overline{CE}$ D_n to $\overline{PL}$	– 8 8 8	10 4 3 2*	– – – –	– 8 8 8	– – – –	ns	1.2 2.0 2.7 3.0 to 3.6	Fig.9
t_h	hold time $\overline{CE}$ to CP CP to $\overline{CE}$	– 5 5 5	−30 −10 −8 −6*	– – – –	– 5 5 5	– – – –	ns	1.2 2.0 2.7 3.0 to 3.6	Fig.9
f_{max}	maximum clock pulse frequency	14 19 24	40 58 70*	– – –	12 16 20	– – –	MHz	2.0 2.7 3.0 to 3.6	Fig.6

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

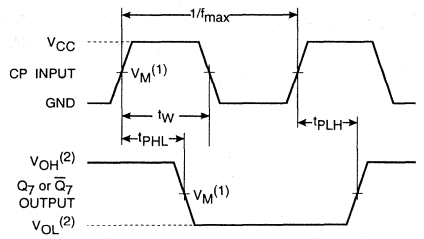


Fig.6 Waveforms showing the clock (CP) to output (Q_7 or $\overline{Q}_7$) propagation delays, the clock pulse width and the maximum clock frequency.

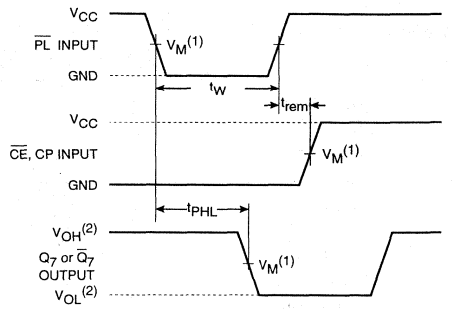


Fig.7 Waveforms showing the parallel load ($\overline{PL}$) pulse width, the parallel load to output (Q_7 or $\overline{Q}_7$) propagation delays, the parallel load to clock (CP) and clock enable ($\overline{CE}$) removal time.

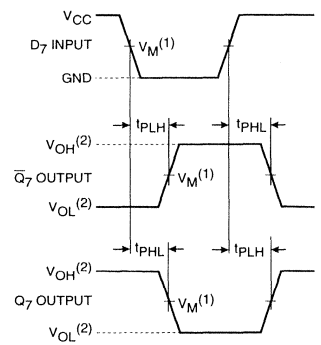


Fig.8 Waveforms showing the data input (D_n) to output (Q_7 or $\overline{Q}_7$) propagation delays when $\overline{PL}$ is LOW.

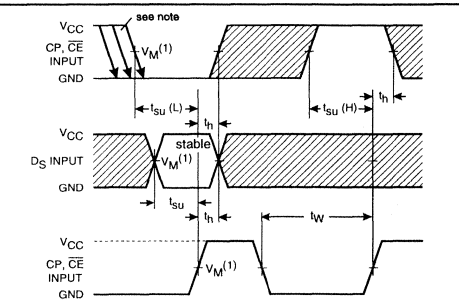


Fig.9 Waveforms showing the set-up and hold times from the serial data input (D_S) to the clock (CP) and clock enable ($\overline{CE}$) inputs, from the clock enable input ($\overline{CE}$) to the clock input (CP) and from the clock input (CP) to the clock enable input ($\overline{CE}$).

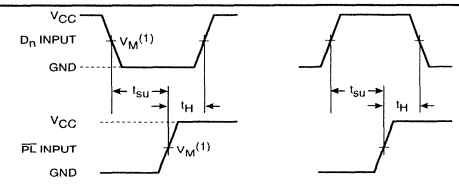


Fig.10 Waveforms showing the set-up and hold times from the data inputs (D_n) to the parallel load input ($\overline{PL}$)

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

Note to Figs 6 and 7
The changing to output assumes internal Q_6 opposite state from Q_7.

Note to Fig. 9
$\overline{CE}$ may change only from HIGH-to-LOW while CP is LOW. The shaded areas indicate when the input is permitted to change for predictable output performance.

Hex D-type flip-flop with reset; positive-edge trigger — 74LV174

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Output capability: standard**
- **I_{CC} category: MSI**

DESCRIPTION

The 74LV174 is a low-voltage Si-gate CMOS device and is pin and function compatible with the 74HC/HCT174.

The 74LV174 has six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common clock (CP) and master reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one set-up time prior to the LOW-to-HIGH clock transition, is transferred to the corresponding output of the flip-flop.

A LOW level on the $\overline{MR}$ input forces all outputs LOW, independently of clock or data inputs.

The device is useful for applications requiring true outputs only and clock and master reset inputs that are common to all storage elements.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay CP to Q_n $\overline{MR}$ to Q_n	C_L = 15 pF V_{CC} = 3.3 V	16 13	ns ns
f_{max}	maximum clock frequency		77	MHz
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	V_{CC} = 3.3 V notes 1 and 2	17	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV174N	16	DIL	plastic	DIL16/SOT38Z
74LV174D	16	SO	plastic	SO16/SOT109A
74LV174DB	16	SSOP	plastic	SSOP16/SOT338
74LV174PW	16	TSSOP	plastic	TSSOP16/SOT403

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	asynchronous master reset (active LOW)
2, 5, 7, 10, 12, 15	Q_0 to Q_5	flip-flop outputs
3, 4, 6, 11, 13, 14	D_0 to D_5	data inputs
8	GND	ground (0 V)
9	CP	clock input (LOW-to-HIGH, edge-triggered)
16	V_{CC}	positive supply voltage

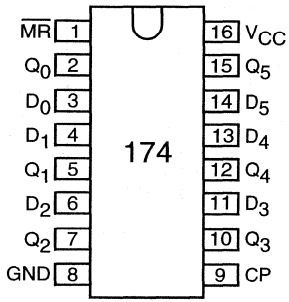


Fig.1 Pin configuration.

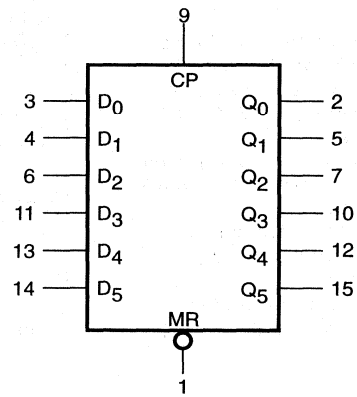


Fig.2 Logic symbol.

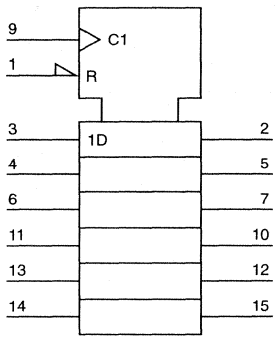


Fig.3 IEC logic symbol.

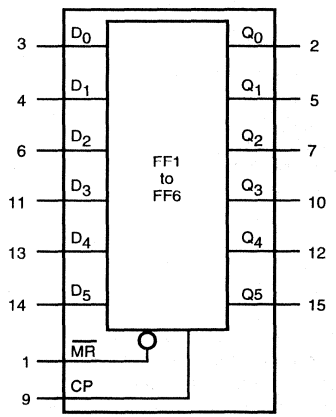


Fig.4 Functional diagram

FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS
	$\overline{MR}$	CP	D_n	Q_n
reset (clear)	L	X	X	L
load '1'	H	↑	h	H
load '0'	H	↑	l	L

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
q = lower case letter indicate the state of referenced input one set-up time prior to the LOW-to-HIGH clock transition
↑ = LOW-to-HIGH clock transition

DC CHARACTERISTICS FOR 74LV174

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LV174

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	–	100	–	–	–	ns	1.2	Fig.5
		–	34	65	–	77		2.0	
		–	25	48	–	56		2.7	
		–	19*	38	–	45		3.0 to 3.6	
t_{PHL}	propagation delay $\overline{MR}$ to Q_n	–	80	–	–	–	ns	1.2	Fig.6
		–	27	51	–	61		2.0	
		–	20	38	–	45		2.7	
		–	15*	30	–	36		3.0 to 3.6	
t_W	clock pulse width HIGH or LOW	34	10	–	41	–	ns	2.0	Fig.5
		25	8	–	30	–		2.7	
		20	6*	–	24	–		3.0 to 3.6	
t_W	master reset pulse width LOW	34	9	–	41	–	ns	2.0	Fig.6
		25	6	–	30	–		2.7	
		20	4*	–	24	–		3.0 to 3.6	
t_{rem}	removal time $\overline{MR}$ to CP	–	−20	–	–	–	ns	1.2	Fig.6
		5	−7	–	5	–		2.0	
		5	−5	–	5	–		2.7	
		5	−4*	–	5	–		3.0 to 3.6	
t_{su}	set-up time D_n to CP	–	10	–	–	–	ns	1.2	Fig.7
		22	4	–	26	–		2.0	
		16	3	–	19	–		2.7	
		13	2*	–	15	–		3.0 to 3.6	
t_h	hold time D_n to CP	–	−10	–	–	–	ns	1.2	Fig.7
		5	−4	–	5	–		2.0	
		5	−2	–	5	–		2.7	
		5	−2*	–	5	–		3.0 to 3.6	
f_{max}	maximum clock pulse frequency	14	40	–	12	–	MHz	2.0	Fig. 5
		19	58	–	16	–		2.7	
		24	70*	–	20	–		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

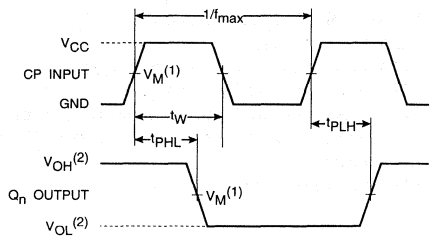


Fig.5 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width and the maximum clock pulse frequency.

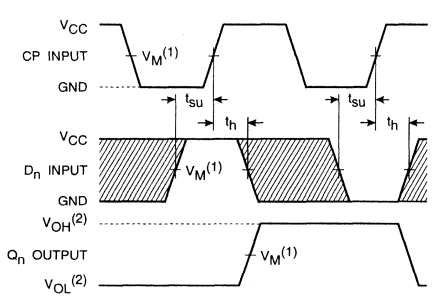


Fig.7 Waveforms showing the data set-up and hold times for the data input (D_n).

Note to Fig.7
The shaded areas indicate when the input is permitted to change for predictable output performance.

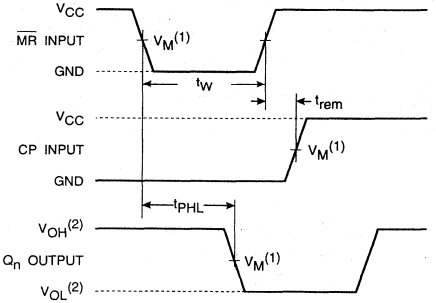


Fig.6 Waveforms showing the master reset ($\overline{MR}$) pulse width, the master reset to output (Q_n) propagation delay and the master reset to clock removal time.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

Octal buffer/line driver; 3-state; inverting — 74LV240

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Output capability: bus driver**
- **I_{CC} category: MSI**

DESCRIPTION

The 74LV240 a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT240.

The 74LV240 is an octal inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state. The '240' is identical to the '244' but has inverting outputs.

FUNCTION TABLE

INPUTS		OUTPUT
$n\overline{OE}$	nA_n	nY_n
L	L	H
L	H	L
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	C_L = 15 pF; V_{CC} = 3.3 V	9.0	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	30	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV240N	20	DIL	plastic	DIL20/SOT146
74LV240D	20	SO	plastic	SO20/SOT163A
74LV240DB	20	SSOP	plastic	SSOP20/SOT339
74LV240PW	20	TSSOP	plastic	TSSOP20/SOT360

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	output enable input (active LOW)
2, 4, 6, 8	$1A_0$ to $1A_3$	data inputs
3, 5, 7, 9	$2Y_0$ to $2Y_3$	bus outputs
10	GND	ground (0 V)
17, 15, 13, 11	$2A_0$ to $2A_3$	data inputs
18, 16, 14, 12	$1Y_0$ to $1Y_3$	bus outputs
19	$2\overline{OE}$	output enable input (active LOW)
20	V_{CC}	positive power supply

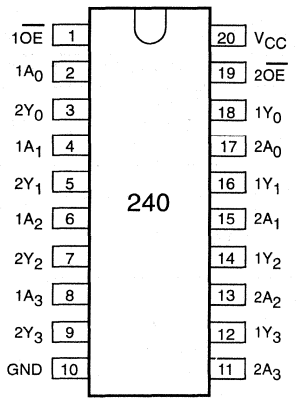


Fig.1 Pin configuration.

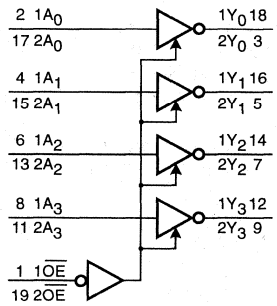


Fig.2 Logic symbol.

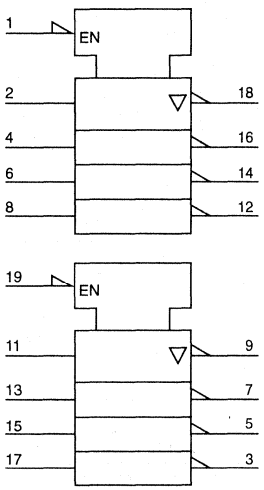


Fig.3 IEC logic symbol.

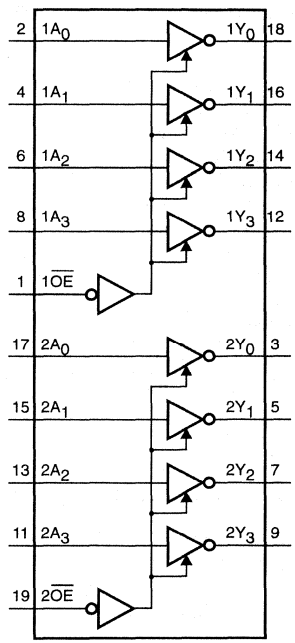


Fig.4 Functional diagram.

DC CHARACTERISTICS FOR 74LV240

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LV240

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	–	55	–	–	–	ns	1.2	Fig. 5
		–	19	36	–	44		2.0	
		–	14	26	–	33		2.7	
		–	10*	21	–	26		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time $1\overline{OE}$ to $1Y_n$; $2\overline{OE}$ to $2Y_n$	–	70	–	–	–	ns	1.2	Fig. 6
		–	24	44	–	54		2.0	
		–	18	33	–	40		2.7	
		–	13*	26	–	32		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time $1\overline{OE}$ to $1Y_n$; $2\overline{OE}$ to $2Y_n$	–	65	–	–	–	ns	1.2	Fig. 6
		–	24	40	–	49		2.0	
		–	18	32	–	37		2.7	
		–	14*	26	–	30		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

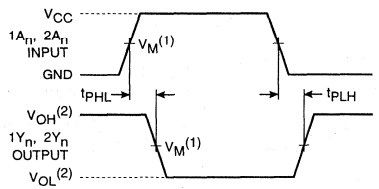


Fig.5 Waveforms showing the input ($1A_n$, $2A_n$) to output ($1Y_n$, $2Y_n$) propagation delays.

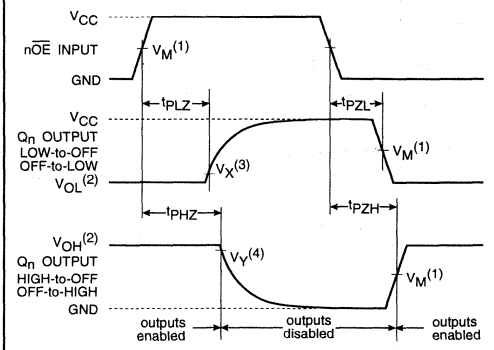
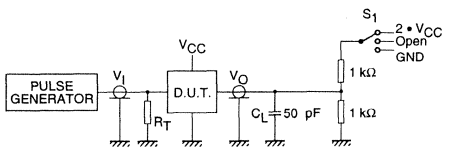


Fig.6 Waveforms showing the 3-state enable and disable times.



Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \cdot V_{CC}$
t_{PHZ}/t_{PZH}	GND

Fig.7 Load circuitry for switching times.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Output capability: bus driver**
- **I_{CC} category: MSI**

DESCRIPTION

The 74LV241 a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT241.

The 74LV241 is an octal non-inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $1\overline{OE}$ and 2OE.

FUNCTION TABLE

INPUTS		OUTPUT
$1\overline{OE}$	$1A_n$	$1Y_n$
L	L	H
L	H	L
H	X	Z

INPUTS		OUTPUT
2OE	$2A_n$	$2Y_n$
H	L	L
H	H	H
L	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	C_L = 15 pF; V_{CC} = 3.3 V	8.0	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	30	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV241N	20	DIL	plastic	DIL20/SOT146
74LV241D	20	SO	plastic	SO20/SOT163A
74LV241DB	20	SSOP	plastic	SSOP20/SOT339
74LV241PW	20	TSSOP	plastic	TSSOP20/SOT360

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	output enable input (active LOW)
2, 4, 6, 8	$1A_0$ to $1A_3$	data inputs
3, 5, 7, 9	$2Y_0$ to $2Y_3$	bus outputs
10	GND	ground (0 V)
17, 15, 13, 11	$2A_0$ to $2A_3$	data inputs
18, 16, 14, 12	$1Y_0$ to $1Y_3$	bus outputs
19	2OE	output enable input (active HIGH)
20	V_{CC}	positive power supply

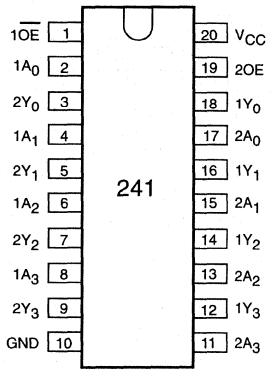


Fig.1 Pin configuration.

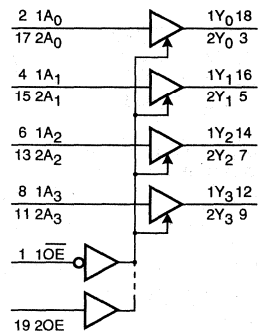


Fig.2 Logic symbol.

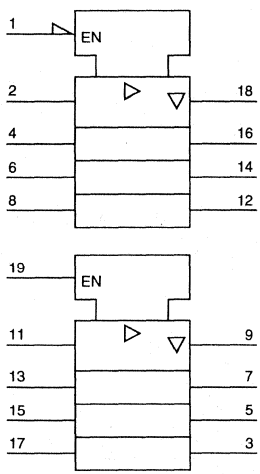


Fig.3 IEC logic symbol.

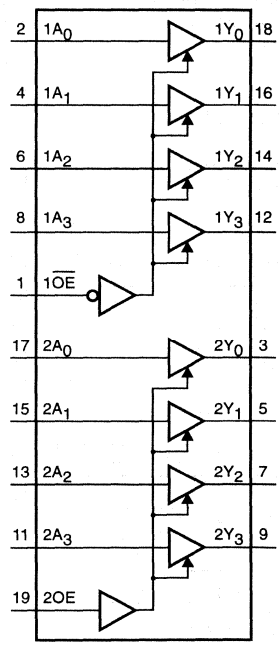


Fig.4 Functional diagram.

DC CHARACTERISTICS FOR 74LV241

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LV241

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	–	45	–	–	–	ns	1.2	Fig. 5
		–	15	31	–	36		2.0	
		–	11	23	–	26		2.7	
		–	9*	18	–	21		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time 1OE to $1Y_n$; 2OE to $2Y_n$	–	55	–	–	–	ns	1.2	Figs 6, 7
		–	19	36	–	44		2.0	
		–	14	26	–	33		2.7	
		–	10*	21	–	26		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time 1$\overline{OE}$ to $1Y_n$; 2OE to $2Y_n$	–	60	–	–	–	ns	1.2	Figs 6, 7
		–	22	39	–	48		2.0	
		–	17	29	–	36		2.7	
		–	13*	24	–	29		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

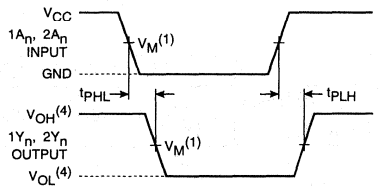


Fig.5 Waveforms showing the input ($1A_n$, $2A_n$) to output ($1Y_n$, $2Y_n$) propagation delays.

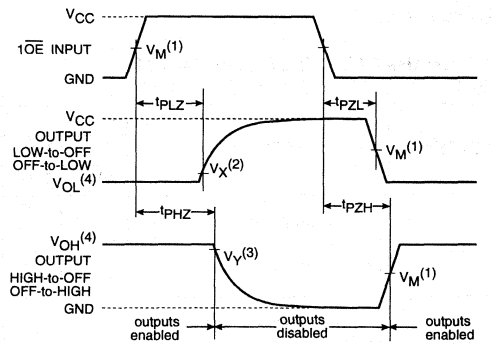


Fig.6 Waveform showing the 3-state enable and disable times.

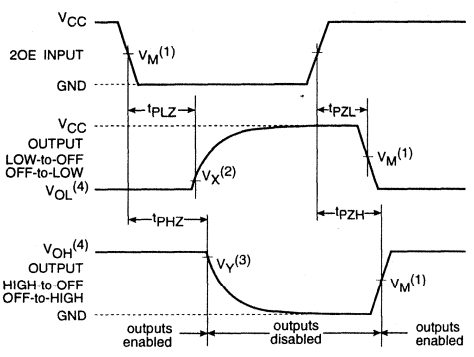


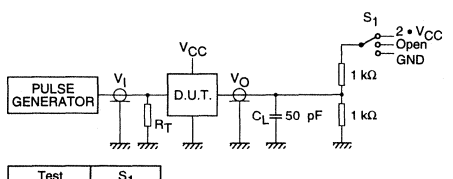
Fig.7 Waveform showing the 3-state enable and disable times for input 2OE.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(3) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load



Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \cdot V_{CC}$
t_{PHZ}/t_{PZH}	GND

Fig.8 Load circuitry for switching times.

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Output capability: bus driver**
- **I_{CC} category: MSI**

DESCRIPTION

The 74LV244 a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT244.

The 74LV244 is an octal non-inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state.
The '244' is identical to the '240' but has non-inverting outputs.

TABLE

INPUTS		OUTPUT
$n\overline{OE}$	nA_n	nY_n
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	C_L = 15 pF; V_{CC} = 3.3 V	8	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	35	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV244N	20	DIL	plastic	DIL20/SOT146
74LV244D	20	SO	plastic	SO20/SOT163A
74LV244DB	20	SSOP	plastic	SSOP20/SOT339
74LV244PW	20	TSSOP	plastic	TSSOP20/SOT360

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	output enable input (active LOW)
2, 4, 6, 8	$1A_0$ to $1A_3$	data inputs
3, 5, 7, 9	$2Y_0$ to $2Y_3$	bus outputs
10	GND	ground (0 V)
17, 15, 13, 11	$2A_0$ to $2A_3$	data inputs
18, 16, 14, 12	$1Y_0$ to $1Y_3$	bus outputs
19	$2\overline{OE}$	output enable input (active LOW)
20	V_{CC}	positive power supply

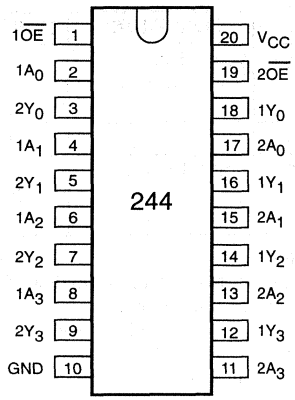


Fig.1 Pin configuration.

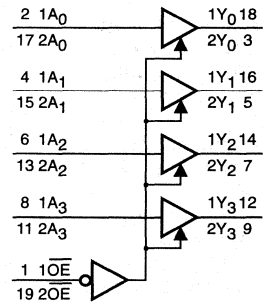


Fig.2 Logic symbol.

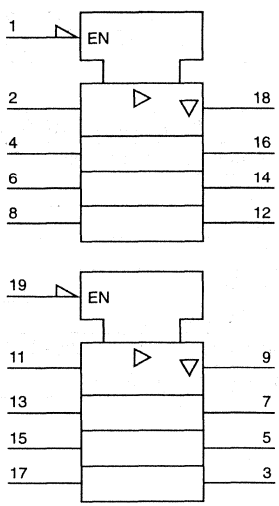


Fig.3 IEC logic symbol.

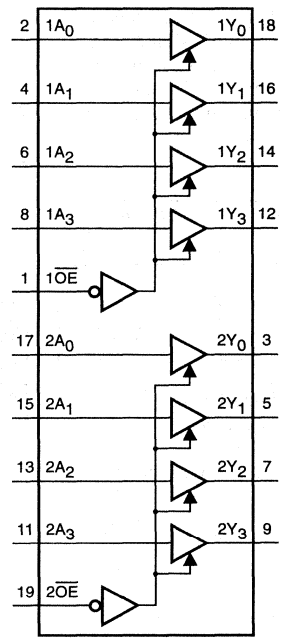


Fig.4 Functional diagram.

DC CHARACTERISTICS FOR 74LV244

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LV244

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	– – – –	50 17 13 9*	– 32 24 19	– – – –	– 39 29 23	ns	1.2 2.0 2.7 3.0 to 3.6	Fig. 5
t_{PZH}/t_{PZL}	3-state output enable time $1\overline{OE}$ to $1Y_n$; $2\overline{OE}$ to $2Y_n$	– – – –	65 22 16 12*	– 44 33 26	– – – –	– 54 40 32	ns	1.2 2.0 2.7 3.0 to 3.6	Fig. 6
t_{PHZ}/t_{PLZ}	3-state output disable time $1\overline{OE}$ to $1Y_n$; $2\overline{OE}$ to $2Y_n$	– – – –	60 22 17 13*	– 40 32 26	– – – –	– 49 37 30	ns	1.2 2.0 2.7 3.0 to 3.6	Fig. 6

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

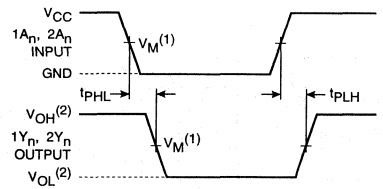


Fig. 5 Waveforms showing the input ($1A_n$, $2A_n$) to output ($1Y_n$, $2Y_n$) propagation delays.

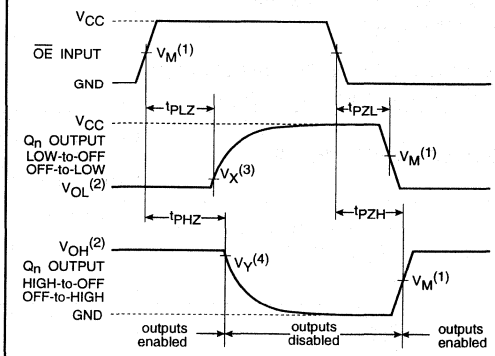
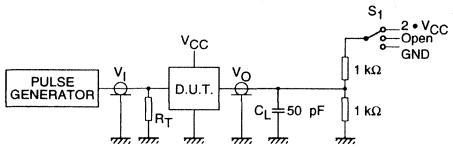


Fig.6 Waveforms showing the 3-state enable and disable times.



Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \cdot V_{CC}$
t_{PHZ}/t_{PZH}	GND

Fig.7 Load circuitry for switching times.

Notes:

(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Output capability: bus driver**
- **I_{CC} category: MSI**

DESCRIPTION

The 74LV245 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT245.

The 74LV245 is an octal transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The '245' features an output enable ($\overline{OE}$) input for easy cascading and a send/receive (DIR) input for direction control. $\overline{OE}$ controls the outputs so that the buses are effectively isolated.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUT	
$\overline{OE}$	DIR	A_n	B_n
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n	C_L = 15 pF V_{CC} = 3.3 V	7	ns
C_I	input capacitance		3.5	pF
$C_{I/O}$	input/output capacitance		10	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	40	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV245N	20	DIL	plastic	DIL20/SOT146
74LV245D	20	SO	plastic	SO20/SOT163A
74LV245DB	20	SSOP	plastic	SSOP20/SOT339
74LV245PW	20	TSSOP	plastic	TSSOP20/SOT360

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	DIR	direction control
2, 3, 4, 5, 6, 7, 8, 9	A_0 to A_7	data inputs/outputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	B_0 to B_7	data inputs/outputs
19	$\overline{OE}$	output enable input (active LOW)
20	V_{CC}	positive supply voltage

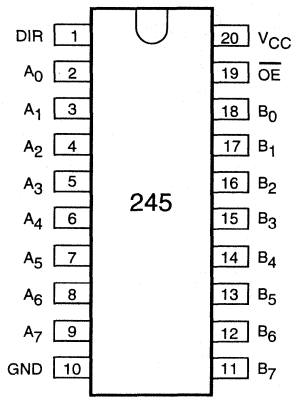


Fig.1 Pin configuration.

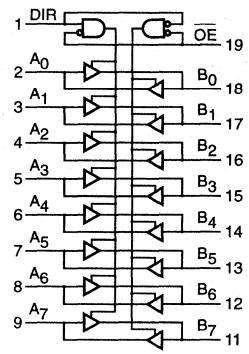


Fig.2 Logic symbol.

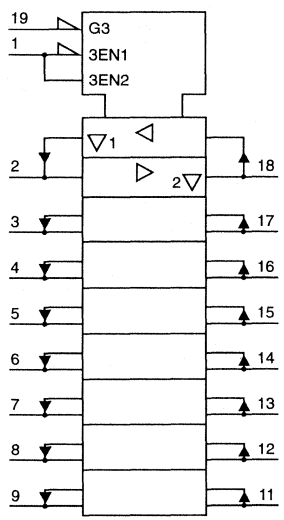


Fig.3 IEC logic symbol.

DC CHARACTERISTICS FOR 74LV245

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LV245

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay	–	45	–	–	–	ns	1.2	Fig.4
	A_n to B_n;	–	15	31	–	36		2.0	
	B_n to A_n	–	11	23	–	26		2.7	
		–	9*	18	–	21		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable	–	55	–	–	–	ns	1.2	Fig.5
	time	–	19	39	–	46		2.0	
	$\overline{OE}$ to A_n;	–	14	29	–	34		2.7	
	$\overline{OE}$ to B_n	–	10*	23	–	27		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output	–	65	–	–	–	ns	1.2	Fig.5
	disable time	–	24	40	–	49		2.0	
	$\overline{OE}$ to A_n;	–	18	32	–	37		2.7	
	$\overline{OE}$ to B_n	–	14*	26	–	30		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

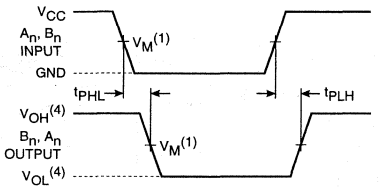


Fig.4 Waveforms showing the input (A_n, B_n) to output (B_n, A_n) propagation delays.

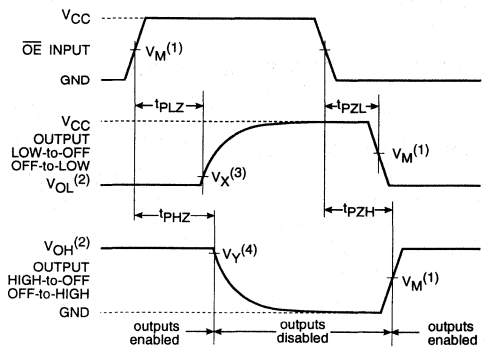
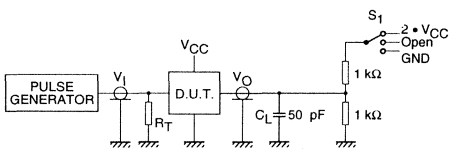


Fig.5 Waveforms showing the 3-state enable and disable times.



Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.6 Load circuitry for switching times.

Notes:

(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

8-input multiplexer; 3-state | 74LV251

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **True and complement outputs**
- **Both outputs are 3-state for further multiplexer expansion**
- **Multifunction capability**
- **Permits multiplexing from n-lines to one line**
- **Output capability: standard**
- **I_{CC} category: MSI**

DESCRIPTION

The 74LV251 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT251.

The 74LV251 is an 8-input multiplexer with 8 binary inputs (I_0 to I_7), an output enable input ($\overline{OE}$) and three select inputs (S_0, S_1, S_2). One of the eight binary inputs is selected by the select inputs and is routed to the outputs ($\overline{Y}$, Y). Both outputs are in the high impedance OFF-state (Z) when the output enable input is HIGH, allowing multiplexer expansion by tying the outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay I_n to Y I_n to $\overline{Y}$ S_n to Y S_n to $\overline{Y}$	C_L = 15 pF V_{CC} = 3.3 V	 14 16 19 20	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	44	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV251N	16	DIL	plastic	DIL16/SOT38Z
74LV251D	16	SO	plastic	SO16/SOT109A
74LV251DB	16	SSOP	plastic	SSOP16/SOT338
74LV251PW	16	TSSOP	plastic	TSSOP16/SOT403

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
4, 3, 2, 1, 15, 14, 13, 12	I_0 to I_7	multiplexer inputs
5	Y	multiplexer output
6	$\overline{Y}$	complementary multiplexer output
7	$\overline{OE}$	3-state output enable input (active LOW)
8	GND	ground (0 V)
11, 10, 9	S_0 to S_2	select inputs
16	V_{CC}	positive supply voltage

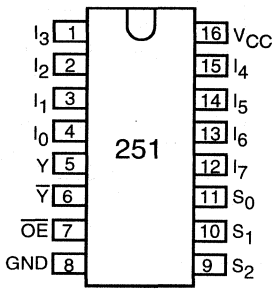


Fig.1 Pin configuration.

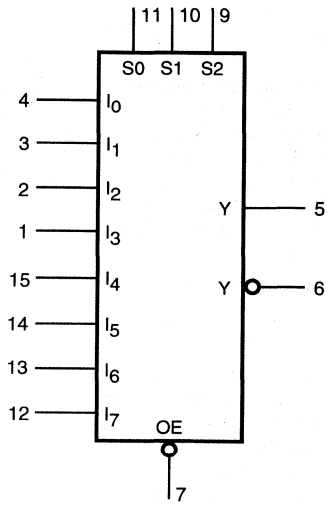


Fig.2 Logic symbol.

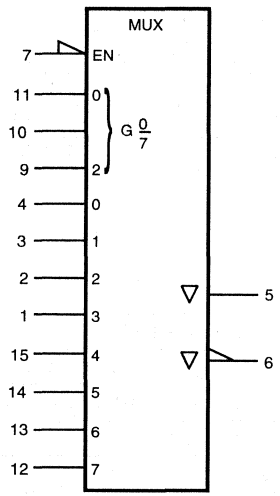


Fig.3 IEC Logic symbol.

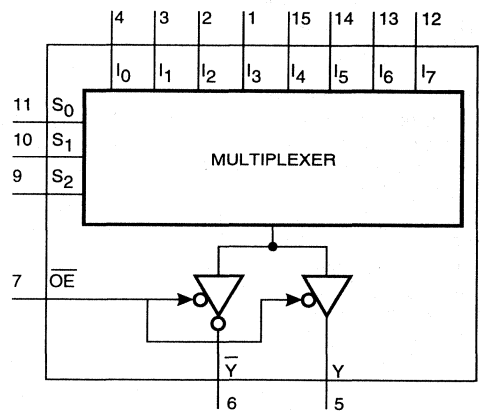


Fig.4 Functional diagram

FUNCTION TABLE

INPUTS												OUTPUTS	
$\overline{OE}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Y}$	Y
H	X	X	X	X	X	X	X	X	X	X	X	Z	Z
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH voltage level
L = LOW voltage level
X = dont't care
Z = HIGH impedance OFF-state

DC CHARACTERISTICS FOR 74LV251

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LV251

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay I_n to Y	–	90	–	–	–	ns	1.2	Fig.5
		–	31	58	–	70		2.0	
		–	23	43	–	51		2.7	
		–	17*	34	–	41		3.0 to 3.6	
t_{PHL}/t_{PLH}	propagation delay I_n to $\overline{Y}$	–	100	–	–	–	ns	1.2	Fig.6
		–	34	65	–	77		2.0	
		–	25	48	–	56		2.7	
		–	19*	38	–	45		3.0 to 3.6	
t_{PHL}/t_{PLH}	propagation delay S_n to Y	–	120	–	–	–	ns	1.2	Fig.5
		–	41	77	–	92		2.0	
		–	30	56	–	68		2.7	
		–	23*	45	–	54		3.0 to 3.6	
t_{PHL}/t_{PLH}	propagation delay S_n to $\overline{Y}$	–	125	–	–	–	ns	1.2	Fig.6
		–	43	82	–	97		2.0	
		–	31	60	–	71		2.7	
		–	24*	48	–	57		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Y, $\overline{Y}$	–	65	–	–	–	ns	1.2	Fig.7
		–	22	43	–	51		2.0	
		–	16	31	–	38		2.7	
		–	12*	25	–	30		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Y, $\overline{Y}$	–	60	–	–	–	ns	1.2	Fig.7
		–	22	39	–	48		2.0	
		–	17	29	–	36		2.7	
		–	13*	24	–	29		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

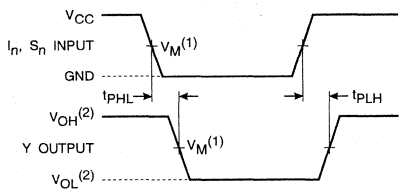


Fig.5 Waveforms showing the multiplexer input (I_n) and select input (S_n) to output (Y) propagation delays.

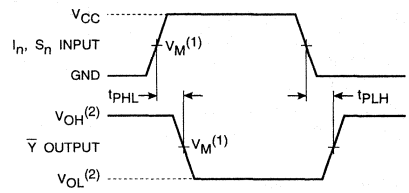


Fig.6 Waveforms showing the multiplexer input (I_n) and the select input (S_n) to output ($\overline{Y}$) propagation delays.

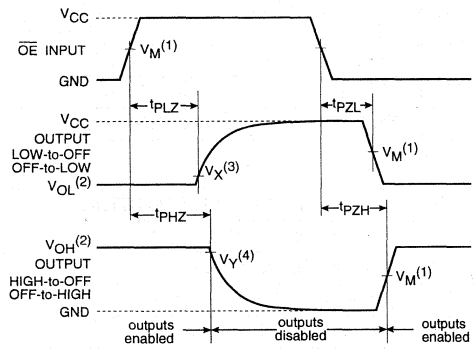
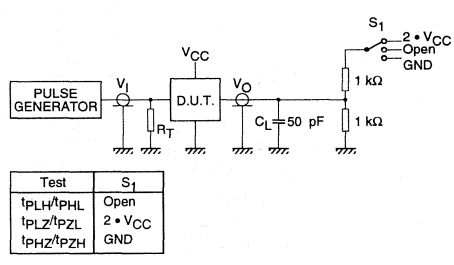


Fig.7 Waveforms showing the 3-state enable and disable times.



Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \cdot V_{CC}$
t_{PHZ}/t_{PZH}	GND

Fig.8 Load circuitry for switching times.

Notes:

(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1.V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1.V_{CC}$ at $V_{CC} < 2.7$ V

Quad 2-input multiplexer; 3-state | 74LV257

FEATURES

- **Optimized for Low Voltage applications: 1.0 V to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C**
- **Non-inverting data path**
- **Output capability: bus driver**
- **I_{CC} category: MSI**

DESCRIPTION

The 74LV257 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT257.

The 74LV257 is a quad 2-input multiplexer with 3-state outputs, which select 4 bits of data from two sources and are controlled by a common data select input (S). The data inputs from source 0 ($1I_0$ to $4I_0$) are selected when input S is LOW and the data inputs from source 1 ($1I_1$ to $4I_1$) are selected when S is HIGH. Data appears at the outputs (1Y to 4Y) in true (non-inverting) form from the selected inputs.
The "257" is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S.
The outputs are forced to a high impedance OFF-state when $\overline{OE}$ is HIGH.

The logic equations for the outputs are:

$1Y = \overline{OE} \cdot (1I_1 \cdot S + 1I_0 \cdot \overline{S})$
$2Y = \overline{OE} \cdot (2I_1 \cdot S + 2I_0 \cdot \overline{S})$
$3Y = \overline{OE} \cdot (3I_1 \cdot S + 3I_0 \cdot \overline{S})$
$4Y = \overline{OE} \cdot (4I_1 \cdot S + 4I_0 \cdot \overline{S})$

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nI_0, nI_1 to nY S to nY	C_L = 15 pF V_{CC} = 3.3 V	10 14	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	30	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV257N	16	DIL	plastic	DIL16/SOT38Z
74LV257D	16	SO	plastic	SO16/SOT109A
74LV257DB	16	SSOP	plastic	SSOP16/SOT338M
74LV257PW	16	TSSOP	plastic	TSSOP16/SOT403

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	S	common data select input
2, 5, 11, 14	$1I_0$ to $4I_0$	data inputs from source 0
3, 6, 10, 13	$1I_1$ to $4I_1$	data inputs from source 1
4, 7, 9, 12	1Y to 4Y	3-state multiplexer outputs
8	GND	ground (0 V)
15	$\overline{OE}$	3-state output enable input (active LOW)
16	V_{CC}	positive supply voltage

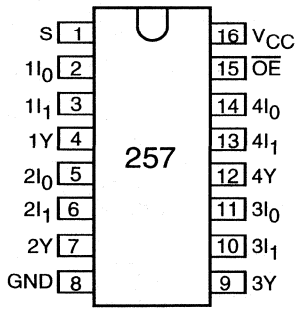


Fig.1 Pin configuration.

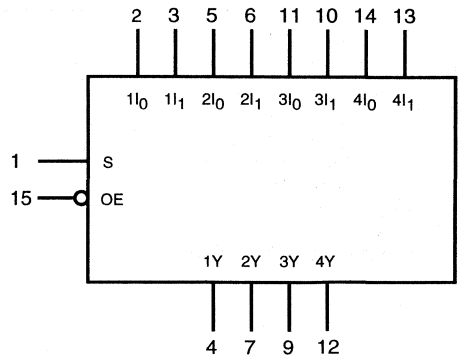


Fig.2 Logic symbol.

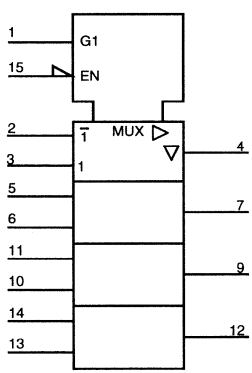


Fig.3 IEC Logic symbol.

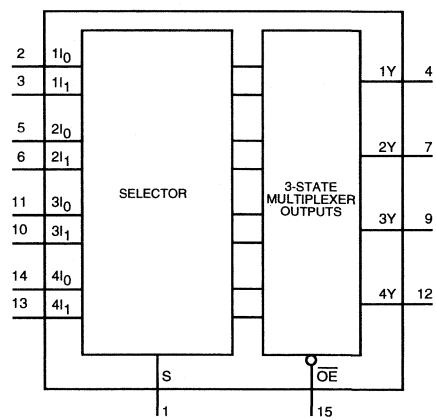


Fig.4 Functional diagram.

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	S	nI_0	nI_1	nY
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = high impedance OFF-state

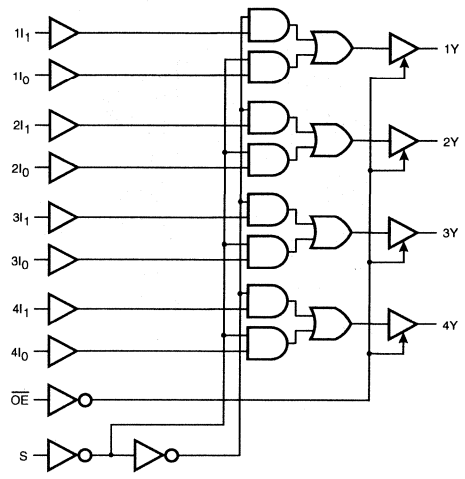


Fig.5 Logic diagram

DC CHARACTERISTICS FOR 74LV257

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74LV257

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay nI_0 to nY; nI_1 to nY	–	65	–	–	–	ns	1.2	Fig.6
		–	22	43	–	51		2.0	
		–	16	31	–	38		2.7	
		–	12*	25	–	30		3.0 to 3.6	
t_{PHL}/t_{PLH}	propagation delay S to nY	–	85	–	–	–	ns	1.2	Fig.6
		–	29	56	–	66		2.0	
		–	21	41	–	49		2.7	
		–	16*	33	–	39		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to nY	–	60	–	–	–	ns	1.2	Fig.7
		–	20	39	–	46		2.0	
		–	15	29	–	34		2.7	
		–	11*	23	–	27		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to nY	–	65	–	–	–	ns	1.2	Fig.7
		–	24	40	–	49		2.0	
		–	18	32	–	37		2.7	
		–	14*	26	–	30		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

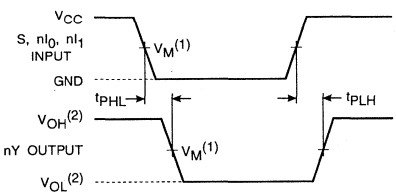


Fig. 6 Waveforms showing the input (S, nI_0, nI_1) to output (nY) propagation delays.

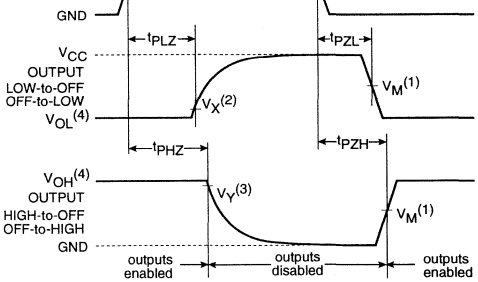
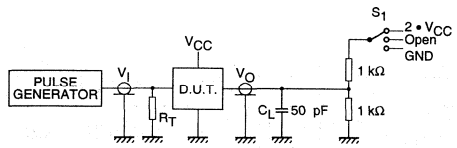


Fig. 7 Waveforms showing the 3-state enable and disable times.

Notes:
(1) $V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
$V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
(2) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
(3) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
(4) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.



Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig. 8 Load circuitry for switching times.

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Combines demultiplexer and 8-bit latch**
- **Serial-to-parallel capability**
- **Output from each storage bit available**
- **Random (addressable) data entry**
- **Easily expandable**
- **Common reset input**
- **Useful as a 3-to-8 active HIGH decoder**
- **Output capability: standard**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74LV259 is a low-voltage CMOS device and is pin and function compatible with 74HC/HCT259.

The 74LV259 is a high-speed 8-bit addressable latch designed for general purpose storage applications in digital systems. The "259" is a multifunctional device capable of storing single-line data in eight addressable latches, and also 3-to-8 decoder and demultiplexer, with active HIGH outputs (Q_0 to Q_7), functions are available.
The "259" also incorporate an active LOW common reset ($\overline{MR}$) for resetting all latches, as well as, an active LOW enable input ($\overline{LE}$).
The "259" has four modes of operation as shown in the mode select table. In the addressable latch mode, data on the data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states.

(continued on next column)

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay D, A_n to Q_n $\overline{LE}$ to Q_n $\overline{MR}$ to Q_n	C_L = 15 pF V_{CC} = 3.3 V	 17 16 14	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	19	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV259N	16	DIL	plastic	DIL16/SOT38Z
74LV259D	16	SO	plastic	SO16/SOT109A
74LV259DB	16	SSOP	plastic	SSOP16/SOT338
74LV259PW	16	TSSOP	plastic	TSSOP16/SOT403

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	A_0 to A_2	address inputs
4, 5, 6, 7, 9, 10, 11, 12	Q_0 to Q_7	latch outputs
8	GND	ground (0 V)
13	D	data input
14	$\overline{LE}$	latch enable input (active LOW)
15	$\overline{MR}$	conditional reset input (active LOW)
16	V_{CC}	positive supply voltage

In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs.

In the 3-to-8 decoding or demultiplexing mode, the addressed output follows the state of the D input with all other outputs in the LOW state. In the reset mode all outputs are LOW and unaffected by the address (A_0 to A_2) and data (D) input. When operating the "259" as an addressable latch, changing more than one bit of address could impose a transient-wrong address. Therefore, this should only be done while in the memory mode. The mode select table summarizes the operations of the "259".

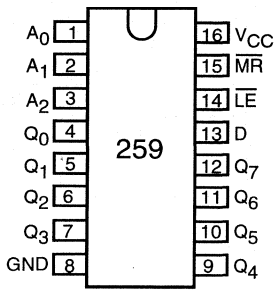


Fig.1 Pin configuration.

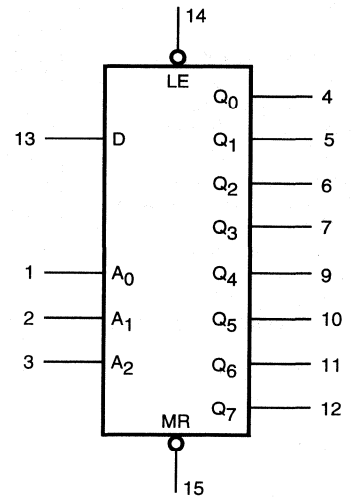


Fig.2 Logic symbol.

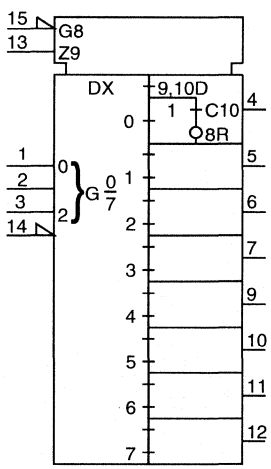


Fig.3 IEC logic symbol.

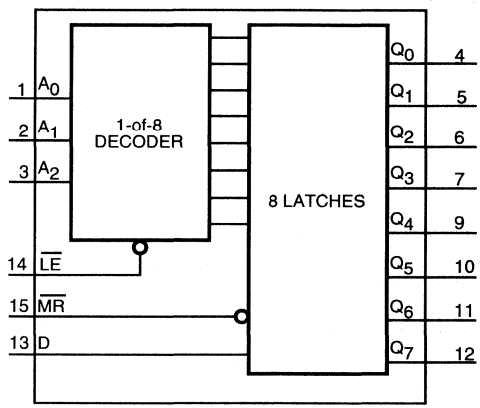


Fig.4 Functional diagram.

MODE SELECT TABLE

$\overline{LE}$	$\overline{MR}$	MODE
L	H	addressable latch
H	H	memory
L	L	active HIGH 8-channel demultiplexer
H	L	reset

FUNCTION TABLE

OPERATING MODES	INPUTS						OUTPUTS							
	$\overline{MR}$	$\overline{LE}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
master reset	L	H	X	X	X	X	L	L	L	L	L	L	L	L
demultiplex (active HIGH) decoder (when D = H)	L	L	d	L	L	L	Q=d	L	L	L	L	L	L	L
	L	L	d	H	L	L	L	Q=d	L	L	L	L	L	L
	L	L	d	L	H	L	L	L	Q=d	L	L	L	L	L
	L	L	d	H	H	L	L	L	L	Q=d	L	L	L	L
	L	L	d	L	L	H	L	L	L	L	Q=d	L	L	L
	L	L	d	H	L	H	L	L	L	L	L	Q=d	L	L
	L	L	d	L	H	H	L	L	L	L	L	L	Q=d	L
	L	L	d	H	H	H	L	L	L	L	L	L	L	Q=d
store (do nothing)	H	H	X	X	X	X	q0	q1	q2	q3	q4	q5	q6	q7
addressable latch	H	L	d	L	L	L	Q=d	q1	q2	q3	q4	q5	q6	q7
	H	L	d	H	L	L	q0	Q=d	q2	q3	q4	q5	q6	q7
	H	L	d	L	H	L	q0	q1	Q=d	q3	q4	q5	q6	q7
	H	L	d	H	H	L	q0	q1	q2	Q=d	q4	q5	q6	q7
	H	L	d	L	L	H	q0	q1	q2	q3	Q=d	q5	q6	q7
	H	L	d	H	L	H	q0	q1	q2	q3	q4	Q=d	q6	q7
	H	L	d	L	H	H	q0	q1	q2	q3	q4	q5	Q=d	q7
	H	L	d	H	H	H	q0	q1	q2	q3	q4	q5	q6	Q=d

H = HIGH voltage level
L = LOW voltage level
X = don't care
d = HIGH or LOW data one set-up time prior to the LOW-to-HIGH $\overline{LE}$ transition
q = lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared

DC CHARACTERISTICS FOR 74LV259

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LV259

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		-40 to +85			-40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay D to Q_n	–	105	–	–	–	ns	1.2	Fig.6
		–	36	68	–	82		2.0	
		–	26	50	–	60		2.7	
		–	20*	40	–	48		3.0 to 3.6	
t_{PHL}/t_{PLH}	propagation delay A_n to Q_n	–	105	–	–	–	ns	1.2	Fig.7
		–	36	68	–	82		2.0	
		–	26	50	–	60		2.7	
		–	20*	40	–	48		3.0 to 3.6	
t_{PHL}/t_{PLH}	propagation delay $\overline{LE}$ to Q_n	–	100	–	–	–	ns	1.2	Fig.5
		–	34	65	–	77		2.0	
		–	25	48	–	56		2.7	
		–	19*	38	–	45		3.0 to 3.6	
t_{PHL}	propagation delay $\overline{MR}$ to Q_n	–	90	–	–	–	ns	1.2	Fig.8
		–	31	58	–	70		2.0	
		–	23	43	–	51		2.7	
		–	17*	34	–	41		3.0 to 3.6	
t_W	$\overline{LE}$ pulse width HIGH or LOW	34	10	–	41	–	ns	2.0	Fig.5
		25	8	–	30	–		2.7	
		20	6*	–	24	–		3.0 to 3.6	
t_W	$\overline{MR}$ pulse width LOW	34	10	–	41	–	ns	2.0	Fig.8
		25	8	–	30	–		2.7	
		20	6*	–	24	–		3.0 to 3.6	
t_{su}	set-up time D, A_n, to $\overline{LE}$	–	35	–	–	–	ns	1.2	Figs 9 and 10
		24	12	–	29	–		2.0	
		18	9	–	21	–		2.7	
		14	7*	–	17	–		3.0 to 3.6	
t_h	hold time D to $\overline{LE}$	–	–30	–	–	–	ns	1.2	Fig.9
		5	–10	–	5	–		2.0	
		5	–8	–	5	–		2.7	
		5	–6*	–	5	–		3.0 to 3.6	
t_h	hold time A_n to $\overline{LE}$	–	–20	–	–	–	ns	1.2	Fig.10
		5	–7	–	5	–		2.0	
		5	–5	–	5	–		2.7	
		5	–4*	–	5	–		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

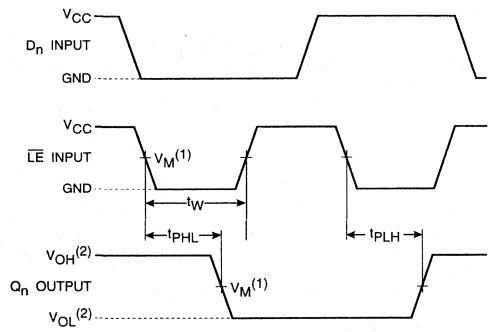


Fig.5 Waveforms showing the enable input ($\overline{LE}$) to output (Q_n) propagation delays and the enable input pulse width.

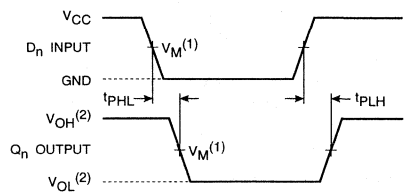


Fig.6 Waveforms showing the data input (D) to output (Q_n) propagation delays.

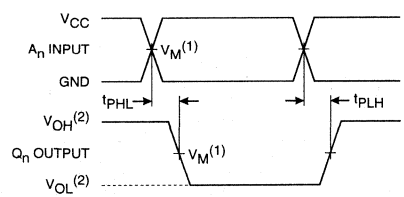


Fig.7 Waveforms showing the address inputs (A_n) to outputs (Q_n) propagation delays.

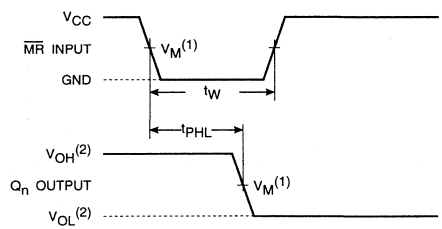


Fig.8 Waveforms showing the conditional reset input ($\overline{MR}$) to output (Q_n) propagation delays.

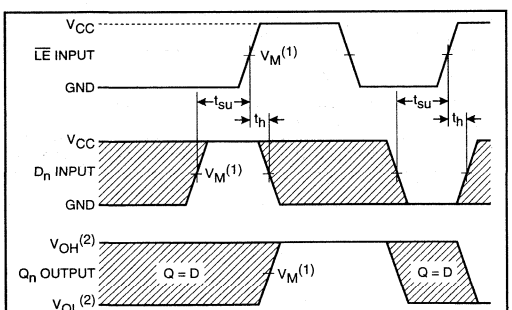


Fig.9 Waveforms showing the data set-up and hold times for D input to $\overline{LE}$ input.

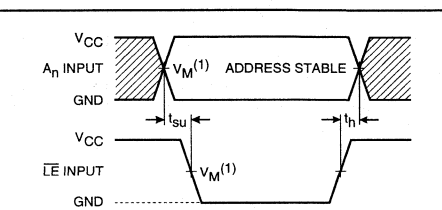


Fig.10 Waveforms showing the address set-up and hold times for A_n inputs to $\overline{LE}$ input.

Note to Figs 9 and 10
The shaded areas indicate when the input is permitted to change for predictable output performance.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

Octal D-type flip-flop with reset; positive-edge trigger 74LV273

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.•**
- **Ideal buffer for MOS microprocessor or memory**
- **Common clock and master reset**
- **Output capability: standard**
- **I_{CC} category: MSI**

DESCRIPTION

The 74LV273 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT273.

The 74LV273 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common clock (CP) and master reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Q_n) of the flip-flop.

All outputs will be forced LOW independently of clock or data inputs by a LOW voltage level on the $\overline{MR}$ input.

The device is useful for applications where the true output only is required and the clock and master reset are common to all storage elements.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay CP to Q_n; $\overline{MR}$ to Q_n	C_L = 15 pF; V_{CC} = 3.3 V	12 13	ns
f_{max}	maximum clock frequency		110	MHz
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	20	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV273N	20	DIL	plastic	DIL20/SOT146
74LV273D	20	SO	plastic	SO20/SOT163A
74LV273DB	20	SSOP	plastic	SSOP20/SOT339
74LV273PW	20	TSSOP	plastic	TSSOP20/SOT360

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	master reset input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q_0 to Q_7	flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	D_0 to D_7	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
20	V_{CC}	positive supply voltage

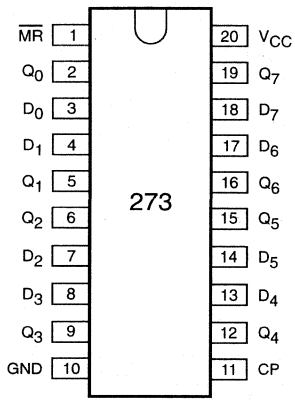


Fig.1 Pin configuration.

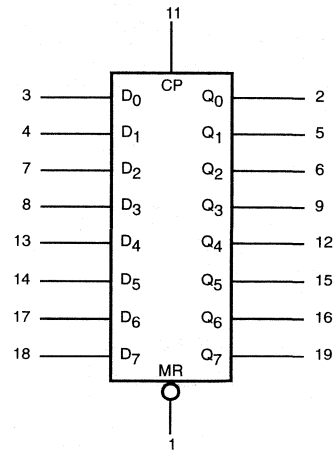


Fig.2 Logic symbol.

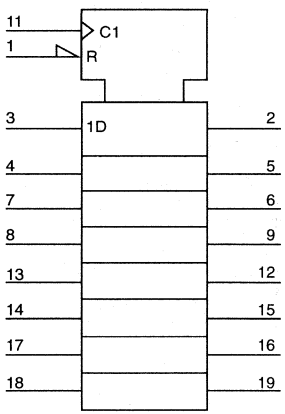


Fig3. IEC logic symbol.

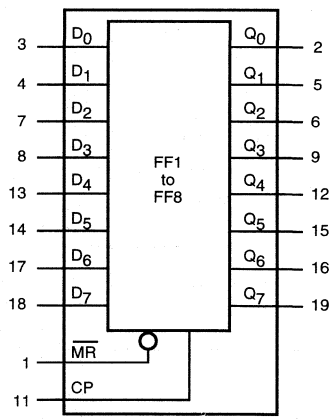


Fig.4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS
	$\overline{MR}$	CP	D_n	Q_0 to Q_7
reset (clear)	L	X	X	L
load '1'	H	↑	h	H
load '0'	H	↑	l	L

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW CP transition
↑ = LOW-to-HIGH transition
X = don't care

DC CHARACTERISTICS FOR 74LV273

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LV273

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		-40 to +85			-40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	–	75	–	–	–	ns	1.2	Fig.5
		–	26	49	–	60		2.0	
		–	19	36	–	44		2.7	
		–	14*	29	–	35		3.0 to 3.6	
t_{PHL}	propagation delay $\overline{MR}$ to Q_n	–	80	–	–	–	ns	1.2	Fig.6
		–	27	51	–	61		2.0	
		–	20	38	–	45		2.7	
		–	15*	30	–	36		3.0 to 3.6	
t_W	clock pulse width HIGH or LOW	34	9	–	41	–	ns	2.0	Fig.5
		25	6	–	30	–		2.7	
		20	5*	–	24	–		3.0 to 3.6	
t_W	master reset pulse width LOW	34	10	–	41	–	ns	2.0	Fig.6
		25	8	–	30	–		2.7	
		20	6*	–	24	–		3.0 to 3.6	
t_{rem}	removal time $\overline{MR}$ to CP	–	−10	–	–	–	ns	1.2	Fig.6
		5	−4	–	5	–		2.0	
		5	−3	–	5	–		2.7	
		5	−2*	–	5	–		3.0 to 3.6	
t_{su}	set-up time D_n to CP	–	20	–	–	–	ns	1.2	Fig.7
		22	7	–	26	–		2.0	
		16	5	–	19	–		2.7	
		13	4*	–	15	–		3.0 to 3.6	
t_h	hold time D_n to CP	–	−10	–	–	–	ns	1.2	Fig.7
		5	−4	–	5	–		2.0	
		5	−3	–	5	–		2.7	
		5	−2*	–	5	–		3.0 to 3.6	
f_{max}	maximum clock pulse frequency	14	40	–	12	–	ns	2.0	Fig. 5
		19	75	–	16	–		2.7	
		24	100*	–	20	–		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

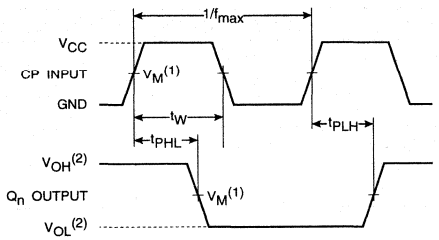


Fig.5 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width and the maximum clock pulse frequency.

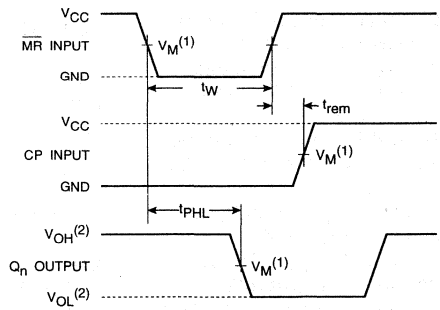


Fig.6 Waveforms showing master reset ($\overline{MR}$) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock (CP) removal time.

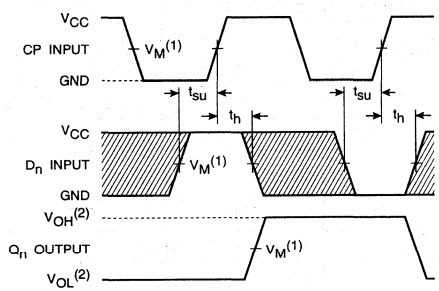


Fig.7 Waveforms showing the data set-up and hold times for the data input (D_n).

Note to Fig.7:
The shaded areas indicate when the input is permitted to change for predictable output performance.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Non-inverting outputs**
- **Output capability: bus driver**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74LV365 is a low-voltage CMOS device and is pin and function compatible with 74HC/HCT365.

The 74LV365 is a hex non-inverting buffer/line driver with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable inputs ($\overline{OE}1$, $\overline{OE}2$).

A HIGH on $\overline{OE}_n$ causes the outputs to assume a high impedance OFF-state.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}_1$	$\overline{OE}_2$	nA	nY
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 15 pF V_{CC} = 3.3 V	9	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	40	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV365N	16	DIL	plastic	DIL16/SOT38Z
74LV365D	16	SO	plastic	SO16/SOT109A
74LV365DB	16	SSOP	plastic	SSOP16/SOT338
74LV365PW	16	TSSOP	plastic	TSSOP16/SOT403

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$\overline{OE}_1$, $\overline{OE}_2$	output enable inputs (active LOW)
2, 4, 6, 10, 12, 14	1A to 6A	data inputs
3, 5, 7, 9, 11, 13	1Y to 6Y	data outputs
8	GND	ground (0 V)
16	V_{CC}	positive supply voltage

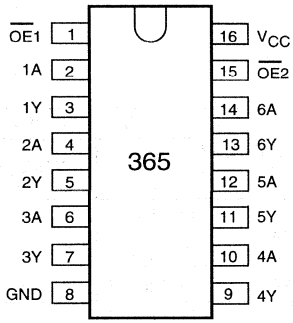


Fig.1 Pin configuration.

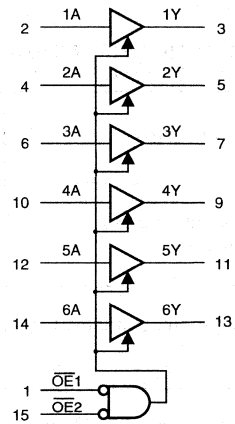


Fig.2 Logic symbol.

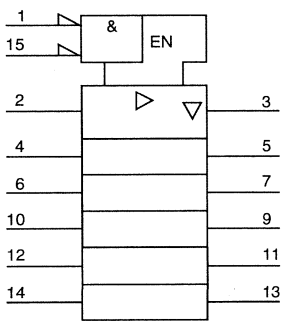


Fig.3 IEC logic symbol.

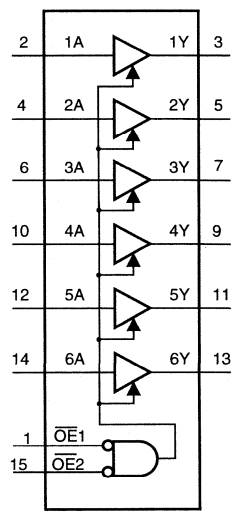


Fig.4 Functional diagram.

DC CHARACTERISTICS FOR 74LV365

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LV365

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay nA to nY	–	55	–	–	–	ns	1.2	Fig. 5
		–	19	36	–	44		2.0	
		–	14	26	–	33		2.7	
		–	10*	21	–	26		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_n$ to nY	–	85	–	–	–	ns	1.2	Fig. 6
		–	29	56	–	66		2.0	
		–	21	41	–	49		2.7	
		–	16*	33	–	39		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_n$ to nY	–	100	–	–	–	ns	1.2	Fig. 6
		–	36	66	–	78		2.0	
		–	27	48	–	58		2.7	
		–	21*	39	–	47		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

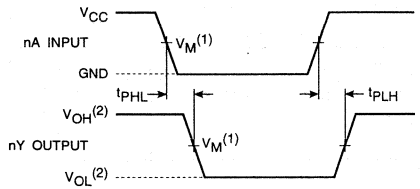


Fig. 5 Waveforms showing the input (nA) to output (nY) propagation delays.

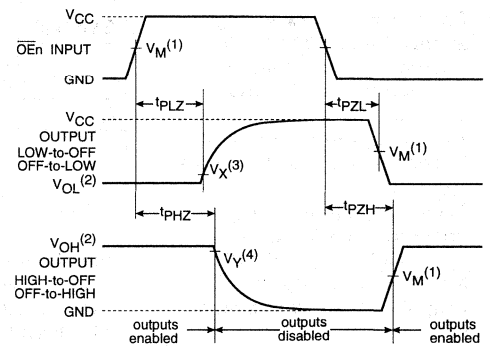
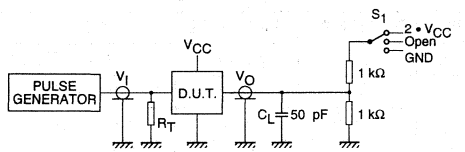


Fig.6 Waveforms showing the 3-state enable and disable times.



Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.7 Load circuitry for switching times.

Notes:

(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Non-inverting outputs**
- **Output capability: bus driver**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74LV367 is a low-voltage CMOS device and is pin and function compatible with 74HC/HCT367.

The 74LV367 is a hex non-inverting buffer/line driver with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable inputs ($1\overline{OE}$, $2\overline{OE}$).

A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state.

FUNCTION TABLE

INPUTS		OUTPUT
$n\overline{OE}$	nA	nY
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 15 pF V_{CC} = 3.3 V	8	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	30	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV367N	16	DIL	plastic	DIL16/SOT38Z
74LV367D	16	SO	plastic	SO16/SOT109A
74LV367DB	16	SSOP	plastic	SSOP16/SOT338
74LV367PW	16	TSSOP	plastic	TSSOP16/SOT403

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$1\overline{OE}$, $2\overline{OE}$	output enable inputs (active LOW)
2, 4, 6, 10, 12, 14	1A to 6A	data inputs
3, 5, 7, 9, 11, 13	1Y to 6Y	data outputs
8	GND	ground (0 V)
16	V_{CC}	positive supply voltage

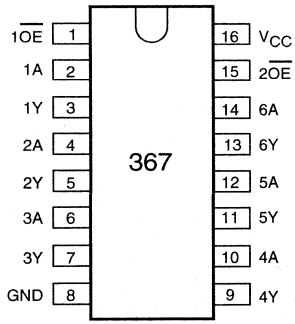


Fig.1 Pin configuration.

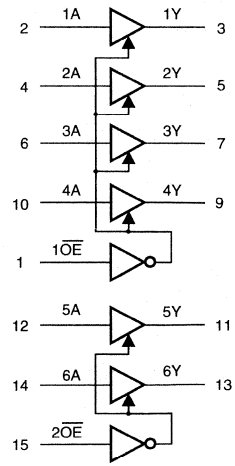


Fig.2 Logic symbol.

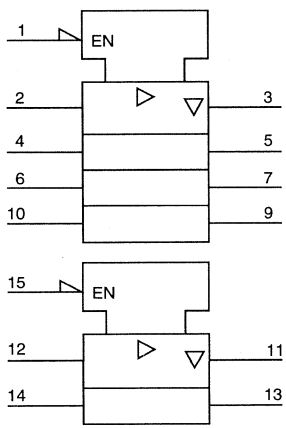


Fig.3 IEC logic symbol.

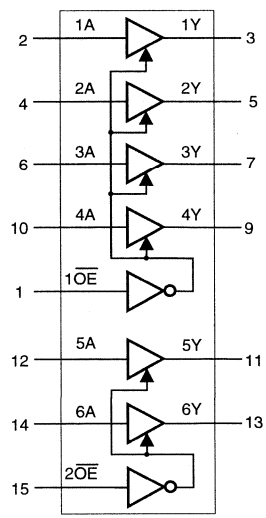


Fig.4 Functional diagram.

DC CHARACTERISTICS FOR 74LV367

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LV367

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay nA to nY	–	50	–	–	–	ns	1.2	Fig. 5
		–	17	32	–	39		2.0	
		–	13	24	–	29		2.7	
		–	10*	19	–	23		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time nOE to nY	–	80	–	–	–	ns	1.2	Fig. 6
		–	27	51	–	60		2.0	
		–	20	38	–	44		2.7	
		–	15*	30	–	36		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time nOE to nY	–	90	–	–	–	ns	1.2	Fig. 6
		–	32	59	–	70		2.0	
		–	24	44	–	52		2.7	
		–	19*	36	–	42		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

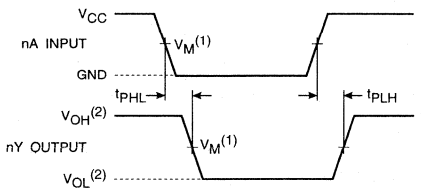


Fig. 5 Waveforms showing the input (nA) to output (nY) propagation delays.

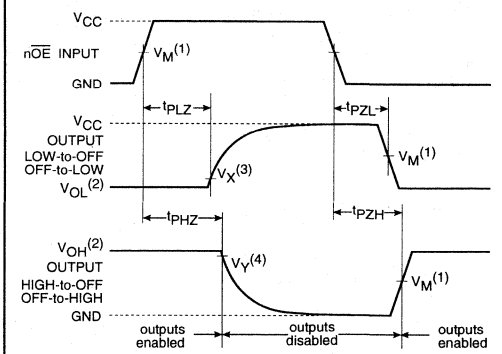
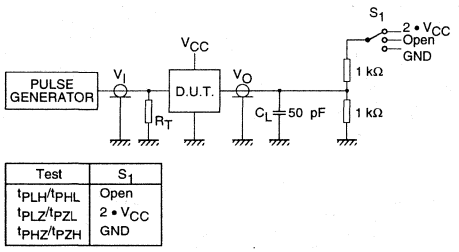


Fig.6 Waveforms showing the 3-state enable and disable times.



Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \cdot V_{CC}$
t_{PHZ}/t_{PZH}	GND

Fig.7 Load circuitry for switching times.

Notes:

(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

Octal D-type transparent latch; 3-state | 74LV373

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Common 3-state output enable input**
- **Output capability: bus driver**
- **I_{CC} category: MSI**

DESCRIPTION

The 74LV373 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT373.

The 74LV373 is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. A latch enable (LE) input and an output enable ($\overline{OE}$) input are common to all internal latches.

The '373' consists of eight D-type transparent latches with 3-state true outputs. When LE is HIGH, data at the D_n inputs enters the latches. In this condition the latches are transparent, i.e. a latch output will change each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the eight latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

The '373' is functionally identical to the '573', but the '573' has a different pin arrangement.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n; LE to Q_n	C_L = 15 pF; V_{CC} = 3.3 V	10 12	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	22	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV373N	20	DIL	plastic	DIL20/SOT146
74LV373D	20	SO	plastic	SO20/SOT163A
74LV373DB	20	SSOP	plastic	SSOP20/SOT339
74LV373PW	20	TSSOP	plastic	TSSOP20/SOT360

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	output enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q_0 to Q_7	3-state latch outputs
3, 4, 7, 8, 13, 14, 17, 18	D_0 to D_7	data inputs
10	GND	ground (0 V)
11	LE	latch enable input (active HIGH)
20	V_{CC}	positive supply voltage

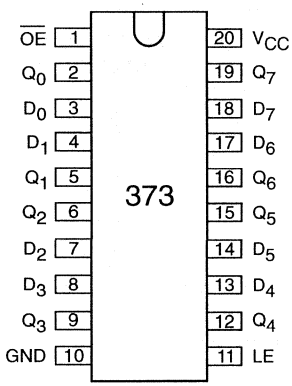


Fig.1 Pin configuration.

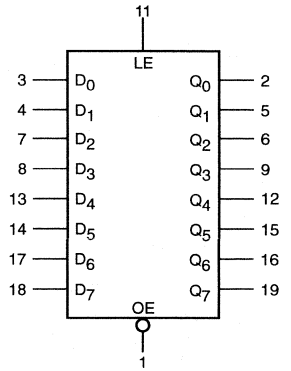


Fig.2 Logic symbol.

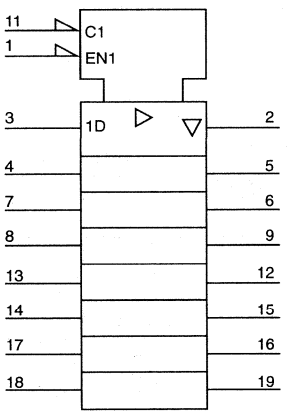


Fig3. IEC logic symbol.

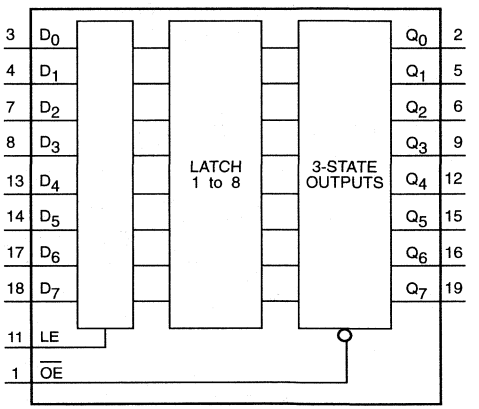


Fig.4 Functional diagram.

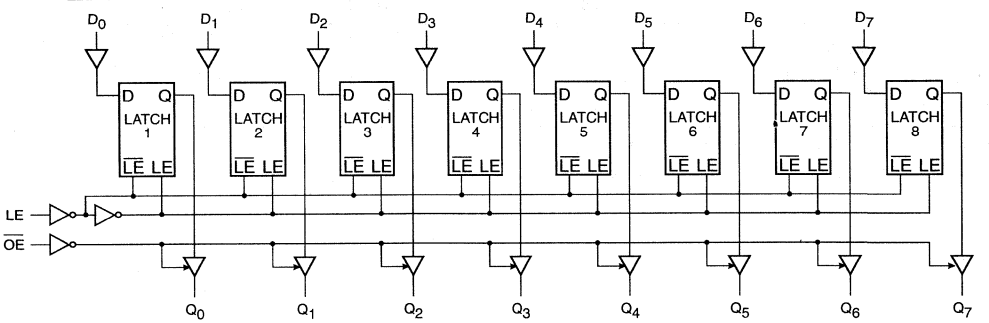


Fig.5 Logic diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$\overline{OE}$	LE	D_n		Q_0 to Q_7
enable and read register (transparent mode)	L L	H H	L H	L H	L H
latch and read register	L L	L L	l h	L H	L H
latch register and disable outputs	H H	L L	l h	L H	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
X = don't care
Z = high impedance OFF-state

DC CHARACTERISTICS FOR 74LV373

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LV373

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n	– – – –	65 22 16 12*	– 43 31 25	– – – –	– 51 38 30	ns	1.2 2.0 2.7 3.0 to 3.6	Fig.6
t_{PHL}/t_{PLH}	propagation delay LE to Q_n	– – – –	75 26 19 14*	– 49 36 29	– – – –	– 60 44 35	ns	1.2 2.0 2.7 3.0 to 3.6	Fig.7
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n	– – – –	75 26 19 14*	– 49 36 29	– – – –	– 60 44 35	ns	1.2 2.0 2.7 3.0 to 3.6	Fig.8
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n	– – – –	75 27 21 16*	– 48 36 29	– – – –	– 58 43 35	ns	1.2 2.0 2.7 3.0 to 3.6	Fig.8

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC CHARACTERISTICS FOR 74LV373 ***(Continued)***

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_W	LE pulse width HIGH	34	10	–	41	–	ns	2.0	Fig.7
		25	8	–	30	–		2.7	
		20	6*	–	24	–		3.0 to 3.6	
t_{su}	set-up time D_n to LE	–	25	–	–	–	ns	1.2	Fig.9
		17	9	–	20	–		2.0	
		13	6	–	15	–		2.7	
		10	5*	–	12	–		3.0 to 3.6	
t_h	hold time D_n to LE	–	−15	–	–	–	ns	1.2	Fig.9
		10	−5	–	10	–		2.0	
		10	−3	–	10	–		2.7	
		10	−3*	–	10	–		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

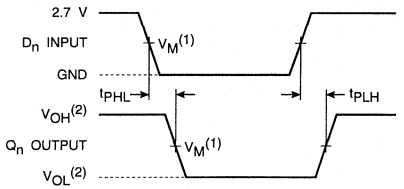


Fig.6 Waveforms showing the data input (D_n) to output (Q_n) propagation delays.

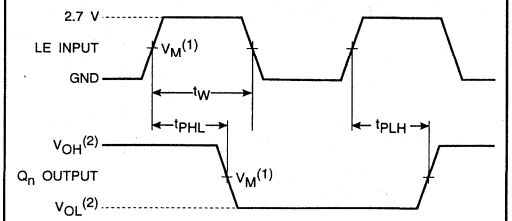


Fig.7 Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output (Q_n) propagation delays.

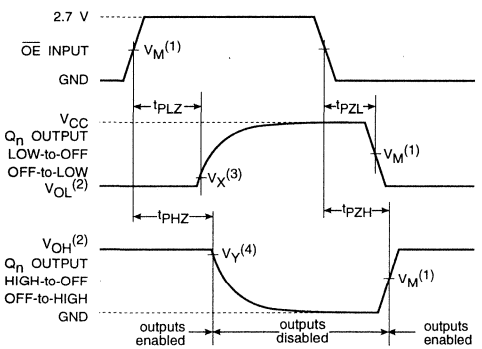


Fig.8 Waveforms showing the 3-state enable and disable times

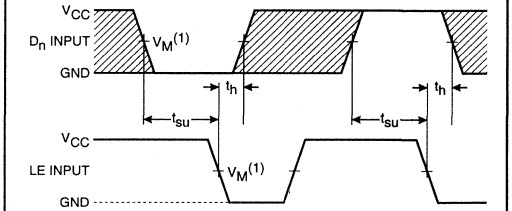
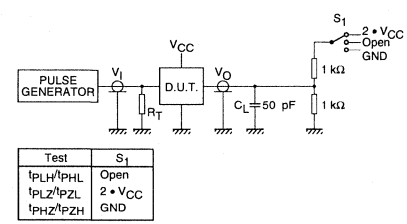


Fig.9 Waveforms showing the data set-up and hold times for the D_n input to the LE input.

Note to Fig.9:

The shaded areas indicate when the input is permitted to change for predictable output performance.



Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \cdot V_{CC}$
t_{PHZ}/t_{PZH}	GND

Fig.10 Load circuitry for switching times.

Notes:

(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

Octal D-type flip-flop; positive-edge trigger; 3-state — 74LV374

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Common 3-state output enable input**
- **Output capability: bus driver**
- **I_{CC} category: MSI**

DESCRIPTION

The 74LV374 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT374.

The 74LV374 is an octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A clock (CP) and an output enable ($\overline{OE}$) input are common to all flip-flops.

The eight flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition.

When $\overline{OE}$ is LOW, the contents of the eight flip-flops is available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 15 pF; V_{CC} = 3.3 V	13	ns
f_{max}	maximum clock frequency		77	MHz
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	25	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV374N	20	DIL	plastic	DIL20/SOT146
74LV374D	20	SO	plastic	SO20/SOT163A
74LV374DB	20	SSOP	plastic	SSOP20/SOT339
74LV374PW	20	TSSOP	plastic	TSSOP20/SOT360

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	output enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q_0 to Q_7	3-state flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	D_0 to D_7	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
20	V_{CC}	positive supply voltage

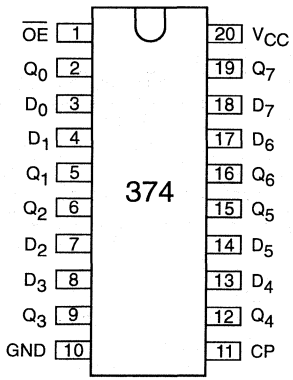


Fig.1 Pin configuration.

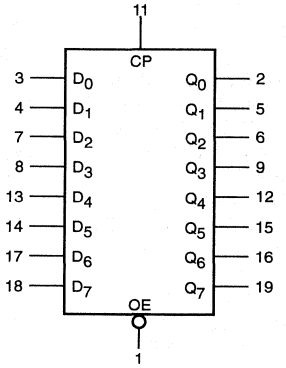


Fig.2 Logic symbol.

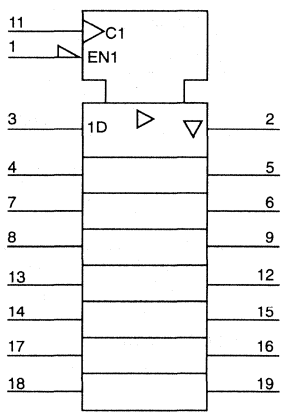


Fig3. IEC logic symbol.

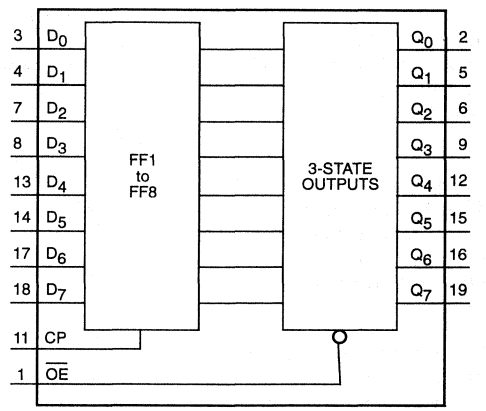


Fig.4 Functional diagram.

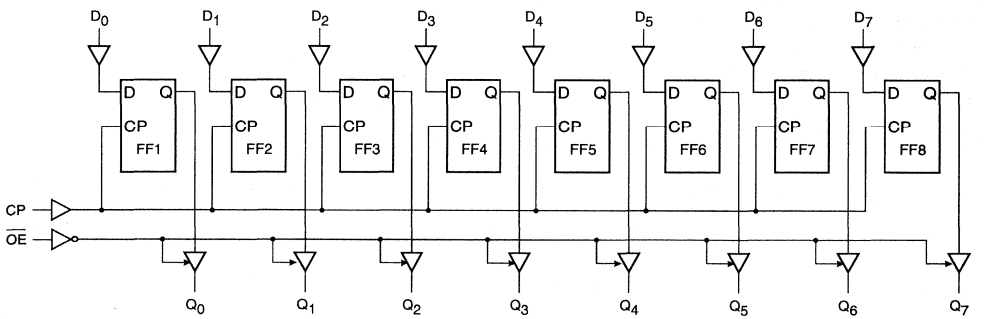


Fig.5 Logic diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	CP	D_n		Q_0 to Q_7
load and read register	L	↑	l	L	L
	L	↑	h	H	H
load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
Z = high impedance OFF-state
↑ = LOW-to-HIGH clock transition

DC CHARACTERISTICS FOR 74LV374

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LV374

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	–	80	–	–	–	ns	1.2	Fig.6
		–	27	51	–	61		2.0	
		–	20	38	–	45		2.7	
		–	15*	30	–	36		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n	–	75	–	–	–	ns	1.2	Fig.7
		–	26	49	–	60		2.0	
		–	19	36	–	44		2.7	
		–	14*	29	–	35		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n	–	80	–	–	–	ns	1.2	Fig.7
		–	29	48	–	58		2.0	
		–	22	36	–	43		2.7	
		–	16*	29	–	35		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC CHARACTERISTICS FOR 74LV374 ***(Continued)***

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_W	clock pulse width HIGH or LOW	34	12	–	41	–	ns	2.0	Fig.6
		25	9	–	30	–		2.7	
		20	7*	–	24	–		3.0 to 3.6	
t_{su}	set-up time D_n to CP	–	25	–	–	–	ns	1.2	Fig.8
		22	9	–	26	–		2.0	
		16	6	–	19	–		2.7	
		13	5*	–	15	–		3.0 to 3.6	
t_h	hold time D_n to CP	–	−10	–	–	–	ns	1.2	Fig.8
		5	−3	–	5	–		2.0	
		5	−2	–	5	–		2.7	
		5	−2*	–	5	–		3.0 to 3.6	
f_{max}	maximum clock pulse frequency	15	40	–	12	–	MHz	2.0	Fig.6
		19	58	–	16	–		2.7	
		24	70*	–	20	–		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.

* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

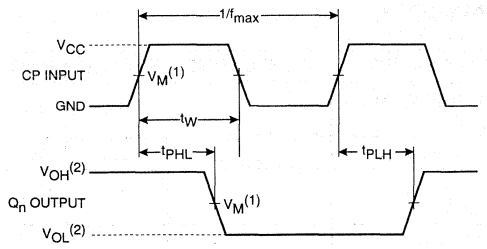


Fig.6 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width and the maximum clock pulse frequency.

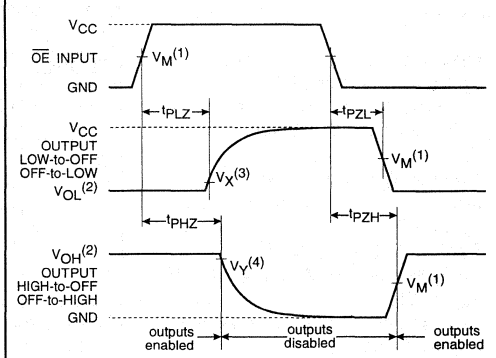


Fig.7 Waveforms showing the 3-state enable and disable times.

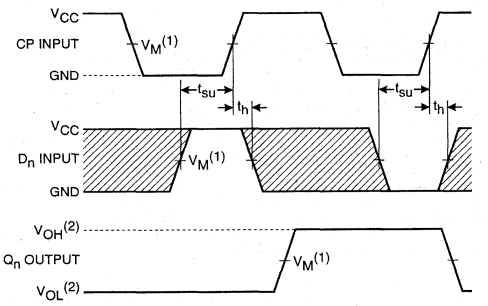
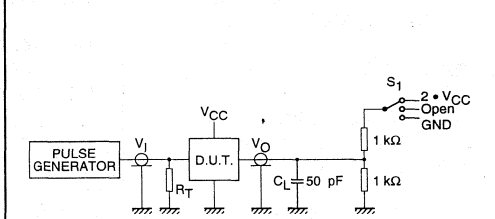


Fig.8 Waveforms showing the data set-up and hold times for the D_n input to the CP input.

Note to Fig.8:

The shaded areas indicate when the input is permitted to change for predictable output performance.



Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.9 Load circuitry for switching times.

Notes:

(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

Octal D-type flip-flop with data enable; positive edge trigger

74LV377

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Ideal for addressable register applications**
- **Data enable for address and data synchronization applications**
- **Eight positive-edge triggered D-type flip-flops**
- **Output capability: standard**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74LV377 is a low-voltage CMOS device and is pin and function compatible with 74HC/HCT377.

The 74LV377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. A common clock (CP) input loads all flip-flops simultaneously when the data enable ($\overline{E}$) is LOW. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Q_n) of the flip-flop. The $\overline{E}$ input must be stable only one set-up time prior to the LOW-to-HIGH transition for predictable operation.

FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS
	CP	$\overline{E}$	D_n	Q_n
load "1"	↑	l	h	H
load "0"	↑	l	l	L
hold (do nothing)	↑	h	X	no change
	X	H	X	no change

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 15 pF; V_{CC} = 3.3 V	13	ns
C_I	input capacitance		3.5	pF
f_{max}	maximum clock frequency		77	MHz
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	20	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV377N	20	DIL	plastic	DIL20/SOT146
74LV377D	20	SO	plastic	SO20/SOT163A
74LV377DB	20	SSOP	plastic	SSOP20/SOT339
74LV377PW	20	TSSOP	plastic	TSSOP20/SOT360

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{E}$	data enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q_0 to Q_7	flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	D_0 to D_7	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
20	V_{CC}	positive supply voltage

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
↑ = LOW-to-HIGH CP transition
X = don't care

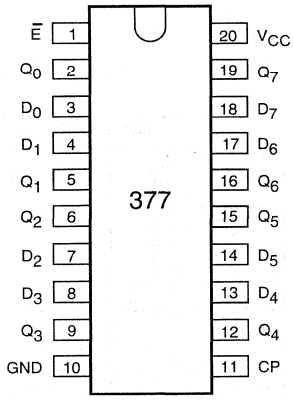


Fig.1 Pin configuration.

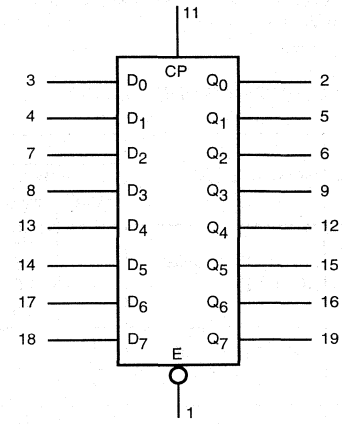


Fig.2 Logic symbol.

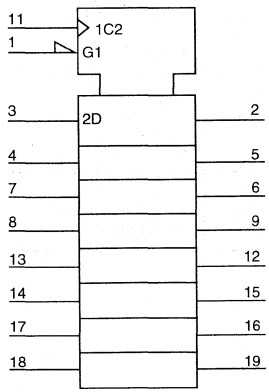


Fig.3 IEC logic symbol.

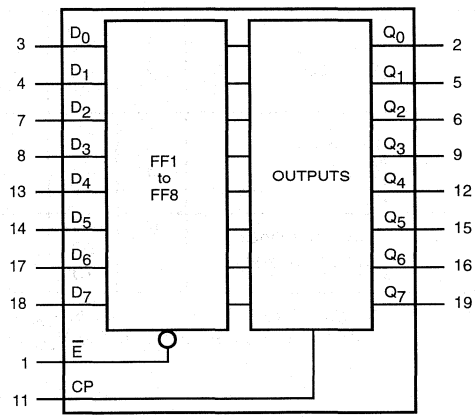


Fig.4 Functional diagram.

DC CHARACTERISTICS FOR 74LV377

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LV377

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	–	80	–	–	–	ns	1.2	Fig.5
		–	27	51	–	61		2.0	
		–	20	38	–	45		2.7	
		–	15*	30	–	36		3.0 to 3.6	
t_W	clock pulse width HIGH or LOW	34	9	–	41	–	ns	2.0	Fig.5
		25	6	–	30	–		2.7	
		20	5*	–	24	–		3.0 to 3.6	
t_{su}	set-up time D_n to CP	–	25	–	–	–	ns	1.2	Fig.6
		22	9	–	26	–		2.0	
		16	6	–	19	–		2.7	
		13	5*	–	15	–		3.0 to 3.6	
t_{su}	set-up time $\overline{E}$ to CP	–	10	–	–	–	ns	1.2	Fig.6
		22	4	–	26	–		2.0	
		16	3	–	19	–		2.7	
		13	2*	–	15	–		3.0 to 3.6	
t_h	hold time D_n to CP	–	−15	–	–	–	ns	1.2	Fig.6
		5	−5	–	5	–		2.0	
		5	−4	–	5	–		2.7	
		5	−3*	–	5	–		3.0 to 3.6	
t_h	hold time $\overline{E}$ to CP	–	−5	–	–	–	ns	1.2	Fig.6
		5	−2	–	5	–		2.0	
		5	−2	–	5	–		2.7	
		5	−1*	–	5	–		3.0 to 3.6	
f_{max}	maximum clock pulse frequency	14	40	–	12	–	MHz	2.0	Fig.5
		19	58	–	16	–		2.7	
		24	70*	–	20	–		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

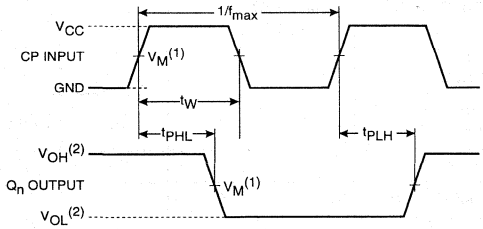


Fig.5 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width and the maximum clock pulse frequency.

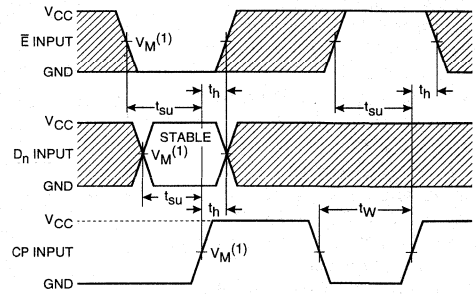


Fig.6 Waveforms showing the data set-up and hold times from the data input (D_n) and from the enable input ($\overline{E}$) to the clock (CP).

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

Note to Fig. 6:

The shaded areas indicate when the input is permitted to change for predictable output performance.

Dual 4-bit binary ripple counter | 74LV393

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Two 4-bit binary counters with individual clocks**
- **Divide-by any binary module up to 28 in one package**
- **Two master resets to clear each 4-bit counter individually**
- **Output capability: standard**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74LV393 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT393.

The 74LV393 is a dual 4-bit binary ripple counter with seperate clocks ($1\overline{CP}$, $2\overline{CP}$) and master reset (1MR, 2MR) inputs to each counter.
The operation of each half of the "393" is the same as the "93" except no external clock connections are required. The counters are triggered by a HIGH-to-LOW transition of the clock inputs. The counter outputs are internally connected to provide clock inputs to succeeding stages. The outputs of the ripple counter do not change synchronously and should not be used for high-speed addres decoding.

The master resets are active-HIGH asynchronous inputs to each 4-bit counter identified by the "1" and "2" in the pin description.
A HIGH level on the nMR input overides the clock and sets the outputs LOW.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to nQ_0 nQ to nQ_{n+1} nMR to nQ_n	C_L = 15 pF V_{CC} = 3.3 V	 12 4 11	ns
f_{max}	maximum clock frequency		99	MHz
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	23	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV393N	14	DIL	plastic	DIL14/SOT27
74LV393D	14	SO	plastic	SO14/SOT108A
74LV393DB	14	SSOP	plastic	SSOP14/SOT337
74LV393PW	14	TSSOP	plastic	TSSOP14/SOT402

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 13	$1\overline{CP}$, $2\overline{CP}$	clock inputs (HIGH-to-LOW, edge-triggered)
2, 12	1MR, 2MR	asynchronous master reset inputs (active HIGH)
3, 4, 5, 6, 11, 10, 9, 8	$1Q_0$ to $1Q_3$ $2Q_0$ to $2Q_3$	flip-flop outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

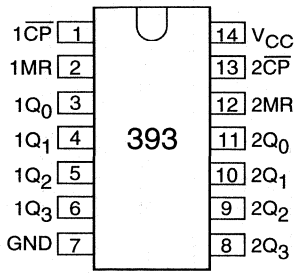


Fig.1 Pin configuration.

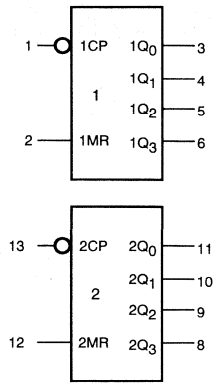


Fig.2 Logic symbol.

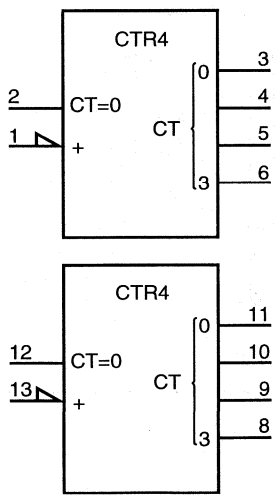


Fig.3 IEC Logic symbol.

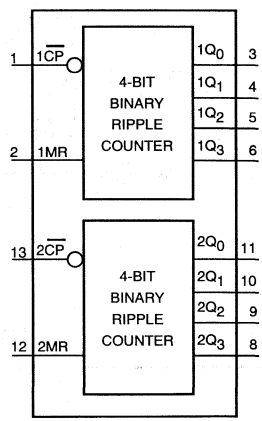


Fig.4 Functional diagram.

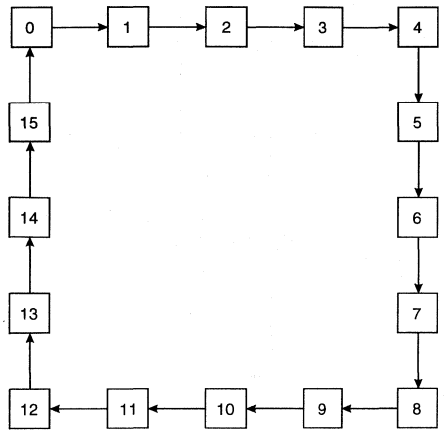


Fig.5 State diagram

COUNT SEQUENCE FOR 1 COUNTER

COUNT	OUTPUTS			
	Q_0	O_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

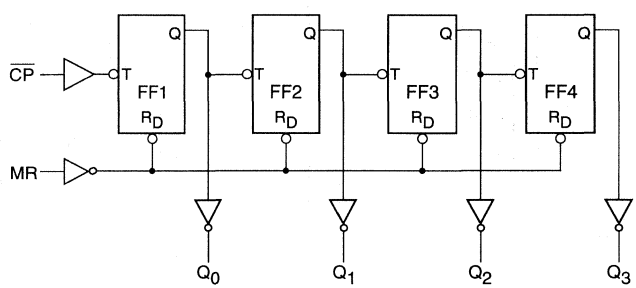


Fig.6 Logic diagram (one counter).

DC CHARACTERISTICS FOR 74LV393

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LV393

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay $n\overline{CP}$ to nQ_0	–	75	–	–	–	ns	1.2	Fig. 7
		–	26	49	–	60		2.0	
		–	19	36	–	44		2.7	
		–	14*	29	–	35		3.0 to 3.6	
t_{PHL}/t_{PLH}	propagation delay nQ_n to nQ_{n+1}	–	25	–	–	–	ns	1.2	Fig. 7
		–	9	17	–	20		2.0	
		–	6	13	–	15		2.7	
		–	5*	10	–	12		3.0 to 3.6	
t_{PHL}	propagation delay nMR to nQ_n	–	70	–	–	–	ns	1.2	Fig. 8
		–	24	44	–	54		2.0	
		–	18	33	–	40		2.7	
		–	13*	26	–	32		3.0 to 3.6	
t_W	clock pulse width HIGH or LOW	34	10	–	41	–	ns	2.0	Fig. 7
		25	8	–	30	–		2.7	
		20	6*	–	24	–		3.0 to 3.6	
t_W	master reset pulse width; HIGH	34	12	–	41	–	ns	2.0	Fig. 8
		25	9	–	30	–		2.7	
		20	7*	–	24	–		3.0 to 3.6	
t_{rem}	removal time nMR to $n\overline{CP}$	–	5	–	–	–	ns	1.2	Fig. 8
		5	2	–	5	–		2.0	
		5	2	–	5	–		2.7	
		5	1*	–	5	–		3.0 to 3.6	
f_{max}	maximum clock pulse frequency	14	53	–	12	–	MHz	2.0	Fig. 7
		19	72	–	16	–		2.7	
		24	90*	–	20	–		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

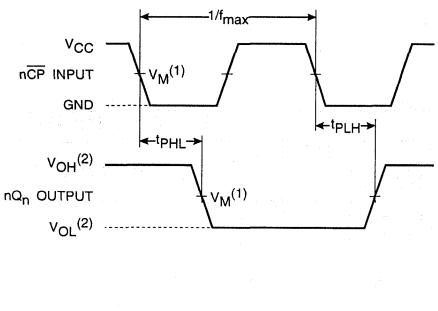


Fig.7 Waveforms showing the clock ($n\overline{CP}$) to output ($1Q_n$, $2Q_n$) propagation delays, the clock pulse width and the maximum clock frequency.

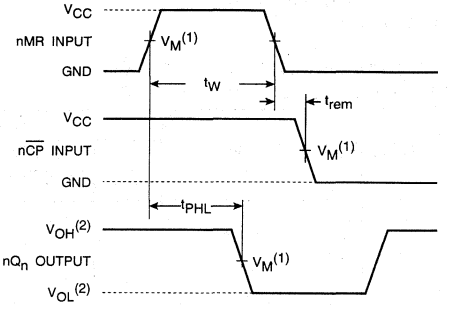


Fig.8 Waveforms showing the master reset (nMR) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock ($n\overline{CP}$) removal time.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

Octal buffer/line driver; 3-state | 74LV541

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Non-inverting outputs**
- **Output capability: bus driver**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74LV541 is a low-voltage CMOS device and is pin and function compatible with 74HC/HCT541.

The 74LV541 is an octal non-inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $\overline{OE}1$ and $\overline{OE}2$.
A HIGH on $\overline{OE}n$ causes the outputs to assume a high impedance OFF-state.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}_1$	$\overline{OE}_2$	nA	nY
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n to Y_n	C_L = 15 pF V_{CC} = 3.3 V	10	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	37	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV541N	20	DIL	plastic	DIL20/SOT146
74LV541D	20	SO	plastic	SO20/SOT163A
74LV541DB	20	SSOP	plastic	SSOP20/SOT339
74LV541PW	20	TSSOP	plastic	TSSOP20/SOT360

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 19	$\overline{OE}_1$, $\overline{OE}_2$	output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	A_0 to A_7	data inputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	Y_0 to Y_7	bus outputs
20	V_{CC}	positive supply voltage

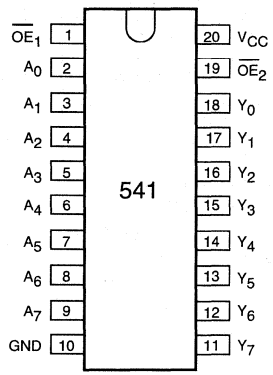


Fig.1 Pin configuration.

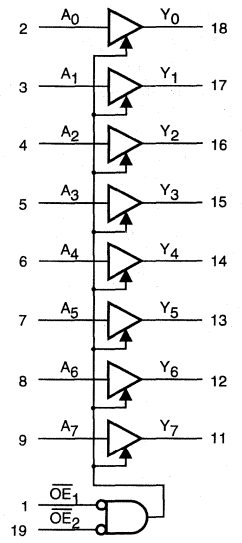


Fig.2 Logic symbol.

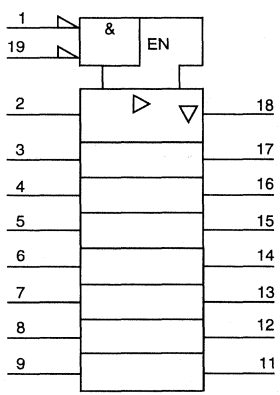


Fig.3 IEC logic symbol.

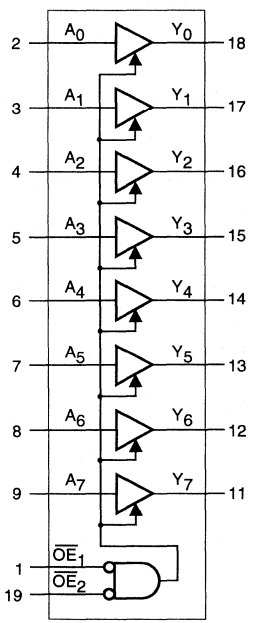


Fig.4 Functional diagram.

DC CHARACTERISTICS FOR 74LV541

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LV541

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay A_n to Y_n	–	60	–	–	–	ns	1.2	Fig. 5
		–	20	39	–	46		2.0	
		–	15	29	–	34		2.7	
		–	11*	23	–	27		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_n$ to Y_n	–	100	–	–	–	ns	1.2	Fig. 6
		–	34	65	–	77		2.0	
		–	25	48	–	56		2.7	
		–	19*	38	–	45		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_n$ to Y_n	–	100	–	–	–	ns	1.2	Fig. 6
		–	36	66	–	78		2.0	
		–	27	48	–	58		2.7	
		–	21*	39	–	47		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

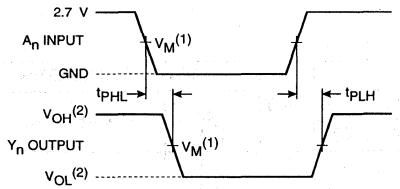


Fig.5 Waveforms showing the input (A_n) to output (Y_n) propagation delays.

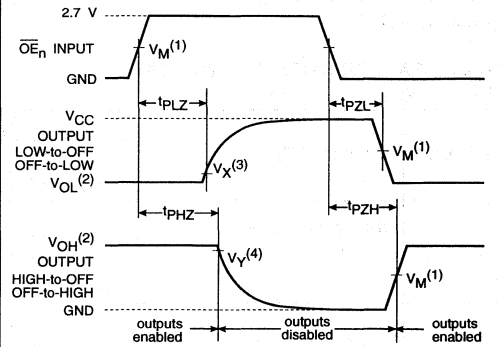
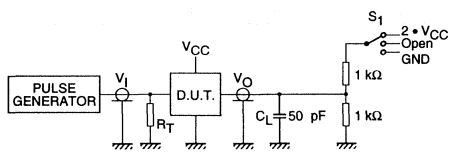


Fig.6 Waveforms showing the 3-state enable and disable times.



Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \cdot V_{CC}$
t_{PHZ}/t_{PZH}	GND

Fig.7 Load circuitry for switching times.

Notes:

(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

Octal D-type transparent latch; 3-state 74LV573

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Inputs and outputs on opposite sides of package allowing easy interface with microprocessors**
- **Useful as input or output port for microprocessors/microcomputer**
- **Common 3-state output enable input**
- **Output capability: bus driver**
- **I_{CC} category: MSI**

DESCRIPTION

The 74LV573 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT573.

The 74LV573 is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. A latch enable (LE) input and an output enable ($\overline{OE}$) are common to all internal latches.
The '573' consists of eight D-type transparent latches with 3-state true outputs. When LE is HIGH, data at the D_n inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes. When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the eight latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.
The '573' is functionally identical to the '563' and the '373', but the '563' has inverted outputs and the '373' has a different pin arrangement.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n; LE to Q_n	C_L = 15 pF; V_{CC} = 3.3 V	12 13	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	26	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV573N	20	DIL	plastic	DIL20/SOT146
74LV573D	20	SO	plastic	SO20/SOT163A
74LV573DB	20	SSOP	plastic	SSOP20/SOT339
74LV573PW	20	TSSOP	plastic	TSSOP20/SOT360

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D_0 to D_7	data inputs
10	GND	ground (0 V)
11	LE	latch enable input (active HIGH)
19, 18, 17, 16, 15, 14, 13, 12	Q_0 to Q_7	data outputs
20	V_{CC}	positive supply voltage

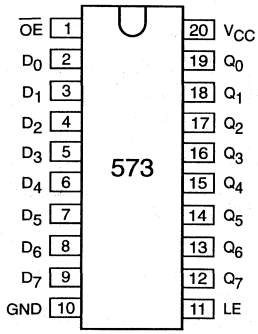


Fig.1 Pin configuration.

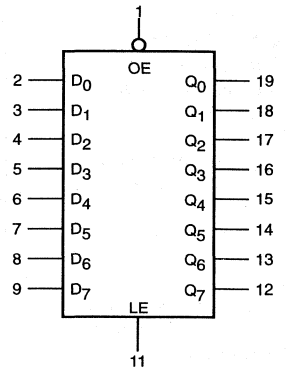


Fig.2 Logic symbol.

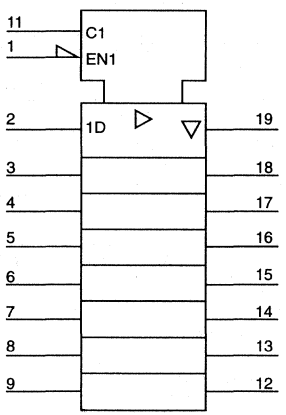


Fig.3 IEC logic symbol.

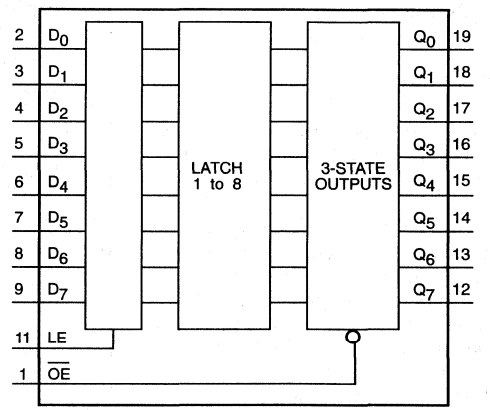


Fig.4 Functional diagram.

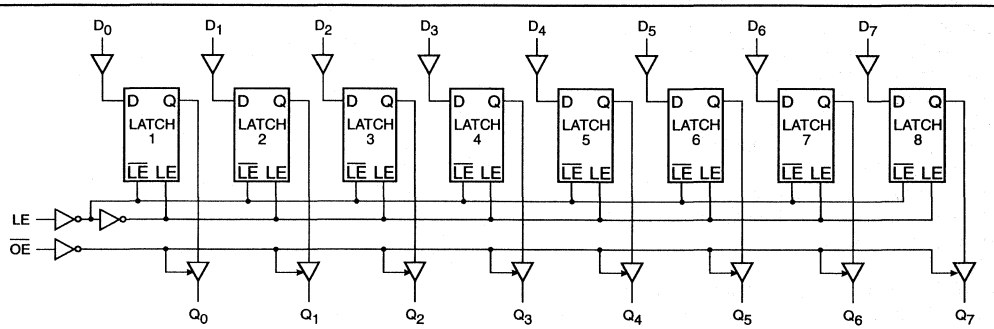


Fig.5 Logic diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$\overline{OE}$	LE	D_n		Q_0 to Q_7
enable and read register (transparent mode)	L L	H H	L H	L H	L H
latch and read register	L L	L L	l h	L H	L H
latch register and disable outputs	H H	L L	l h	L H	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
Z = high impedance OFF-state

DC CHARACTERISTICS FOR 74LV573

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LV573

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n	− − − −	75 26 19 14*	− 49 36 29	− − − −	− 60 44 35	ns	1.2 2.0 2.7 3.0 to 3.6	Fig.6
t_{PHL}/t_{PLH}	propagation delay LE to Q_n	− − − −	80 27 20 15*	− 51 39 31	− − − −	− 61 45 36	ns	1.2 2.0 2.7 3.0 to 3.6	Fig.7
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n	− − − −	70 24 18 13*	− 44 33 26	− − − −	− 54 40 32	ns	1.2 2.0 2.7 3.0 to 3.6	Fig.8
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n	− − − −	80 29 22 17*	− 53 39 32	− − − −	− 63 47 38	ns	1.2 2.0 2.7 3.0 to 3.6	Fig.8

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC CHARACTERISTICS FOR 74LV573 ***(Continued)***

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_W	LE pulse width HIGH	34	9	–	41	–	ns	2.0	Fig.7
		25	6	–	30	–		2.7	
		20	5*	–	24	–		3.0 to 3.6	
t_{su}	set–up time D_n to LE	–	25	–	–	–	ns	1.2	Fig.9
		17	9	–	20	–		2.0	
		13	6	–	15	–		2.7	
		10	5*	–	12	–		3.0 to 3.6	
t_h	hold time D_n to LE	–	5	–	–	–	ns	1.2	Fig.9
		8	2	–	8	–		2.0	
		8	2	–	8	–		2.7	
		8	1*	–	8	–		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.

* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

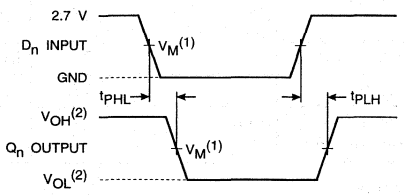


Fig.6 Waveforms showing the data input (D_n) to output (Q_n) propagation delays.

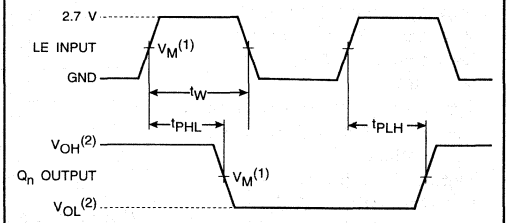


Fig.7 Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output (Q_n) propagation delays.

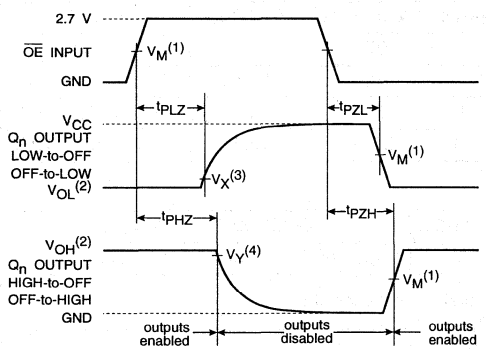


Fig.8 Waveforms showing the 3-state enable and disable times

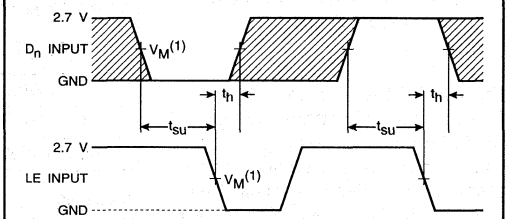
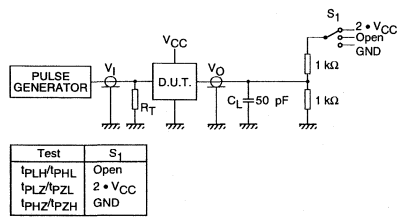


Fig.9 Waveforms showing the data set-up and hold times for the D_n input to the LE input.

Note to Fig.9:

The shaded areas indicate when the input is permitted to change for predictable output performance.



Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.10 Load circuitry for switching times.

Notes:

(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

Octal D-type flip-flop; positive edge-trigger; 3-state — 74LV574

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Common 3-state output enable input**
- **Output capability: bus driver**
- **I_{CC} category: MSI**

DESCRIPTION

The 74LV574 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT574.

The 74LV574 is an octal D-type flip-flop featuring separate D-type inputs for each flip-flop and non-inverting 3-state outputs for bus oriented applications. A clock (CP) and an output enable ($\overline{OE}$) input are common to all flip-flops.

The eight flip-flops will store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH CP transition.

When $\overline{OE}$ is LOW, the contents of the eight flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 15 pF; V_{CC} = 3.3 V	14	ns
f_{max}	maximum clock frequency		77	MHz
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	25	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV574N	20	DIL	plastic	DIL20/SOT146
74LV574D	20	SO	plastic	SO20/SOT163A
74LV574DB	20	SSOP	plastic	SSOP20/SOT339
74LV574PW	20	TSSOP	plastic	TSSOP20/SOT360

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	output enable input (active LOW)
2,3,4,5, 6,7,8,9	D_0 to D_7	data inputs
19,18,17,16, 15,14,13,12	Q_0 to Q_7	3-state flip-flop outputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
20	V_{CC}	positive supply voltage

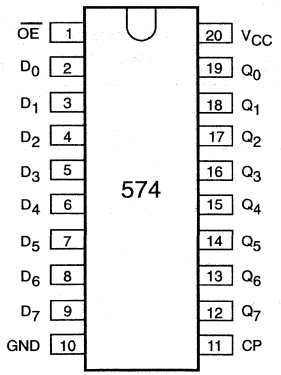


Fig.1 Pin configuration.

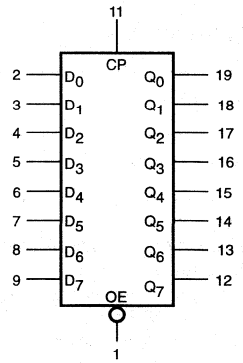


Fig.2 Logic symbol.

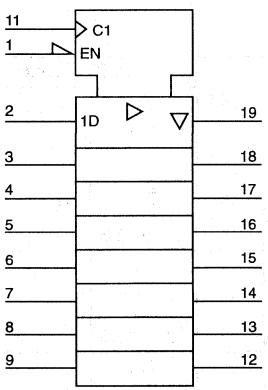


Fig3. IEC logic symbol.

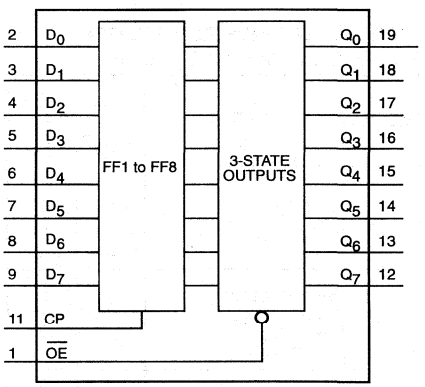


Fig.4 Functional diagram.

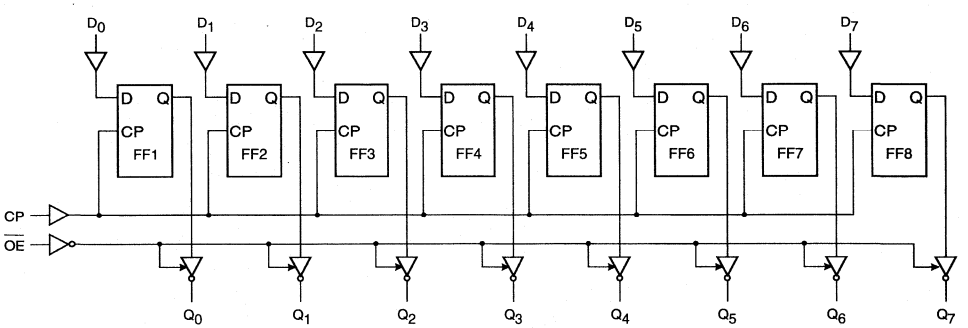


Fig.5 Logic diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	CP	D_n		Q_0 to Q_7
load and read register	L	↑	l	L	L
	L	↑	h	H	H
load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
Z = high impedance OFF-state
↑ = LOW-to-HIGH clock transition

DC CHARACTERISTICS FOR 74LV574

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LV574

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	–	85	–	–	–	ns	1.2	Fig.6
		–	29	56	–	66		2.0	
		–	21	41	–	49		2.7	
		–	16*	33	–	39		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n	–	80	–	–	–	ns	1.2	Fig.7
		–	27	51	–	61		2.0	
		–	20	38	–	45		2.7	
		–	15*	30	–	36		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n	–	60	–	–	–	ns	1.2	Fig.7
		–	22	39	–	48		2.0	
		–	17	29	–	36		2.7	
		–	13*	24	–	29		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC CHARACTERISTICS FOR 74LV574 *(Continued)*

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_W	clock pulse width HIGH or LOW	34	9	–	41	–	ns	2.0	Fig.6
		25	6	–	30	–		2.7	
		20	5*	–	24	–		3.0 to 3.6	
t_{su}	set-up time D_n to CP	–	10	–	–	–	ns	1.2	Fig.8
		22	4	–	26	–		2.0	
		16	3	–	19	–		2.7	
		13	2*	–	15	–		3.0 to 3.6	
t_h	hold time D_n to CP	–	−10	–	–	–	ns	1.2	Fig.8
		5	−4	–	5	–		2.0	
		5	−3	–	5	–		2.7	
		5	−2*	–	5	–		3.0 to 3.6	
f_{max}	maximum clock pulse frequency	15	40	–	12	–	MHz	2.0	Fig.6
		19	58	–	16	–		2.7	
		24	70*	–	20	–		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.

* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

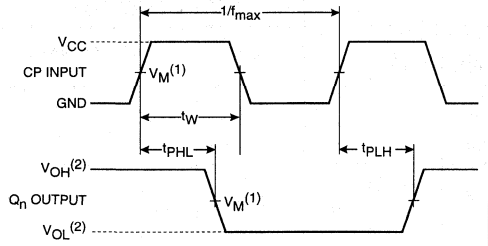


Fig.6 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse (CP) width and the maximum clock pulse frequency.

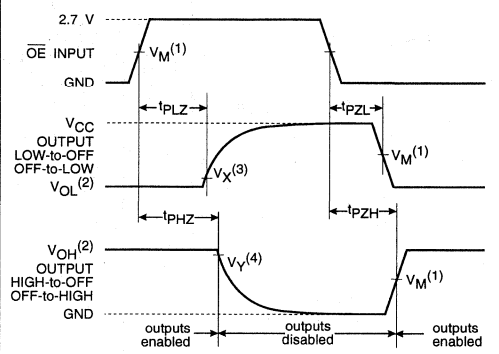


Fig.7 Waveforms showing the 3-state enable and disable times.

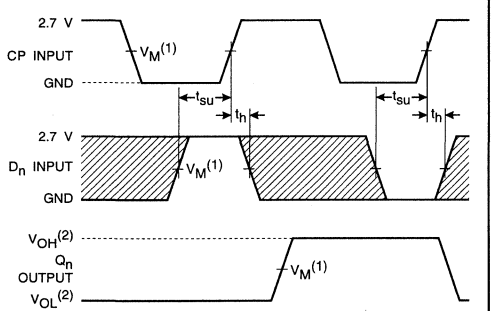
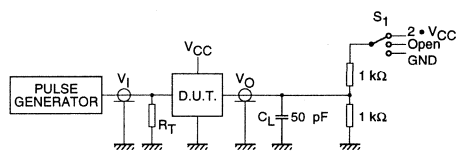


Fig.8 Waveforms showing the data set-up and hold times for the D_n input to the CP input.

Note to Fig.8:

The shaded areas indicate when the input is permitted to change for predictable output performance.



Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.9 Load circuitry for switching times.

Notes:

(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

8-bit serial-in/serial or parallel-out shift register with output latches; 3-state

74LV595

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **8-bit serial input**
- **8-bit serial or parallel output**
- **Storage register with 3-state outputs**
- **Shift register with direct clear**
- **Output capability:**
  - parallel outputs; bus driver
  - serial output; standard
- **I_{CC} category: MSI**

APPLICATIONS

- Serial-to-parallel data conversion
- Remote control holding register

DESCRIPTION

The 74LV595 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT595.

The 74LV595 is an 8-stage serial shift register with a storage register and 3-state outputs. The shift register and storage register have separate clocks.

Data is shifted on the positive-going transitions of the SH_{CP} input. The data in each register is transferred to the storage register on a positive-going transition of the ST_{CP} input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register.

The shift register has a serial input (D_S) and a serial standard output (Q_7') all for cascading. It is also provided with asynchronous reset (active LOW) for alll 8 shift register stages. The storage register has 8 parallel 3-state bus driver outputs. Data in the storage register appears at the output whenever the output enable input ($\overline{OE}$) is LOW.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq$ 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay SH_{CP} to Q_7' ST_{CP} to Q_7' $\overline{MR}$ to Q_7'	C_L = 15 pF V_{CC} = 3.3 V	 15 16 14	ns
f_{MAX}	maximum clock frequency SH_{CP}, ST_{CP}		77	MHz
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per gate	V_{CC} = 3.3 V notes 1 and 2	115	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV595N	16	DIL	plastic	DIL16/SOT38Z
74LV595D	16	SO	plastic	SO16/SOT109A
74LV595DB	16	SSOP	plastic	SSOP16/SOT338
74LV595PW	16	TSSOP	plastic	TSSOP16/SOT403

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
15, 1, 2, 3, 4, 5, 6, 7	Q_0 to Q_7	parallel data output
8	GND	ground (0 V)
9	Q_7'	serial data output
10	$\overline{MR}$	master reset (active LOW)
11	SH_{CP}	shift register clock input
12	ST_{CP}	storage register clock input
13	$\overline{OE}$	output enable input (active LOW)
14	D_S	serial data input
16	V_{CC}	positive supply voltage

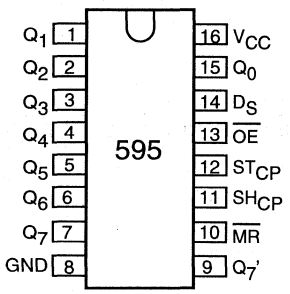


Fig.1 Pin configuration.

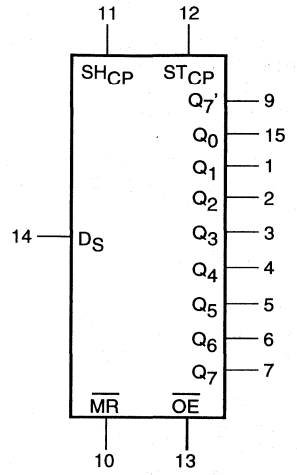


Fig.2 Logic symbol.

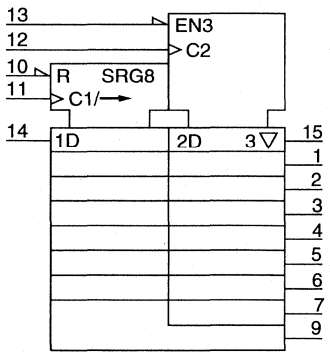


Fig.3 IEC logic symbol.

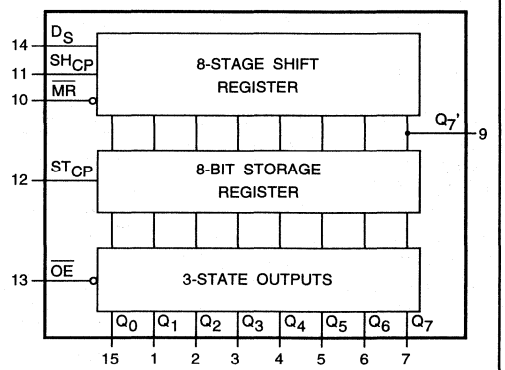


Fig.4 Functional diagram.

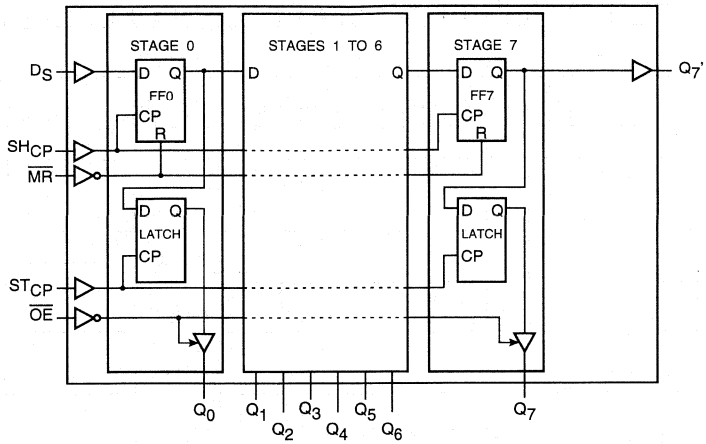


Fig.5 Logic diagram.

FUNCTION TABLE

INPUTS					OUTPUTS		FUNCTION
SH_{CP}	ST_{CP}	$\overline{OE}$	$\overline{MR}$	D_S	Q_7'	Q_n	
X	X	L	L	X	L	NC	a LOW level on $\overline{MR}$ only affects the shift registers
X	↑	L	L	X	L	L	empty shift register loaded into storage register
X	X	H	L	X	L	Z	shift register clear. Parallel outputs in high-impedance OFF-state
↑	X	L	H	H	Q_6'	NC	logic high level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q_6') appears on the serial output (Q_7')
X	↑	L	H	X	NC	Q_n'	contents of shift register stages (internal Q_n') are transferred to the storage register and parallel output stages
↑	↑	L	H	X	Q_6'	Q_n'	contents of shift register shifted through. Previous contents of the shift register are transferred to the storage register and the parallel output stages.

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

NC = no change
↑ = LOW-to-HIGH transition
↓ = HIGH-to-LOW transition

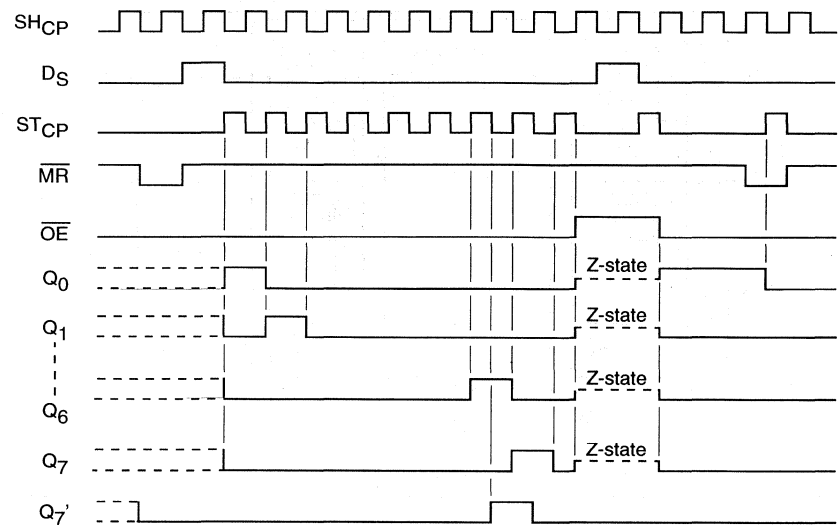


Fig.6 Timing diagram.

DC CHARACTERISTICS FOR 74LV595

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: parallel outputs: bus driver
serial output: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LV595

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay SH_{CP} to Q_7'	–	95	–	–	–	ns	1.2	Fig.7
		–	32	61	–	75		2.0	
		–	24	45	–	55		2.7	
		–	18*	36	–	44		3.0 to 3.6	
t_{PHL}/t_{PLH}	propagation delay ST_{CP} to Q_n	–	100	–	–	–	ns	1.2	Fig.8
		–	34	65	–	77		2.0	
		–	25	48	–	56		2.7	
		–	19*	38	–	45		3.0 to 3.6	
t_{PHL}	propagation delay MR to Q_7'	–	85	–	–	–	ns	1.2	Fig.12
		–	29	56	–	66		2.0	
		–	21	41	–	49		2.7	
		–	16*	33	–	33		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n	–	85	–	–	–	ns	1.2	Fig.9
		–	29	56	–	66		2.0	
		–	21	41	–	49		2.7	
		–	16*	33	–	39		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n	–	65	–	–	–	ns	1.2	Fig.9
		–	24	40	–	49		2.0	
		–	18	32	–	37		2.7	
		–	14*	26	–	30		3.0 to 3.6	
t_W	shift clock pulse width HIGH or LOW	34	10	–	41	–	ns	2.0	Fig.7
		25	8	–	30	–		2.7	
		20	6*	–	24	–		3.0 to 3.6	
t_W	storage clock pulse width HIGH or LOW	34	7	–	41	–	ns	2.0	Fig.8
		25	5	–	30	–		2.7	
		20	4*	–	24	–		3.0 to 3.6	
t_W	master reset pulse width LOW	34	10	–	41	–	ns	2.0	Fig.12
		25	8	–	30	–		2.7	
		20	6*	–	24	–		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC CHARACTERISTICS FOR 74LV4094 ***(Continued)***

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{su}	set-up time D_S to SH_{CP}	– 26 19 15	40 14 10 8*	– – – –	– 31 23 18	– – – –	ns	1.2 2.0 2.7 3.0 to 3.6	Fig.10
t_{su}	set-up time SH_{CP} to ST_{CP}	– 26 19 15	40 14 10 8*	– – – –	– 31 23 18	– – – –	ns	1.2 2.0 2.7 3.0 to 3.6	Fig.8
t_h	hold time D_S to SH_{CP}	– 5 5 5	−10 −4 −3 −2*	– – – –	– 5 5 5	– – – –	ns	1.2 2.0 2.7 3.0 to 3.6	Fig.10
t_{rem}	removal time $\overline{MR}$ to SH_{CP}	– 5 5 5	−35 −12 −9 −7*	– – – –	– 5 5 5	– – – –	ns	1.2 2.0 2.7 3.0 to 3.6	Fig.12
f_{max}	maximum clock pulse frequency SH_{CP} or ST_{CP}	14 19 24	40 58 70*	– – –	12 16 20	– – –	MHz	2.0 2.7 3.0 to 3.6	Figs 7, 8

Notes: All typical values are measured at $T_{amb} = 25$ °C.

* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

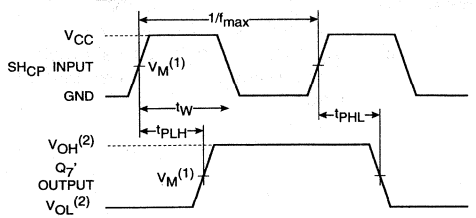


Fig.7 Waveforms showing the clock (SH_{CP}) to output (Q_7'), propagation delays, the shift clock pulse width and the maximum shift clock frequency.

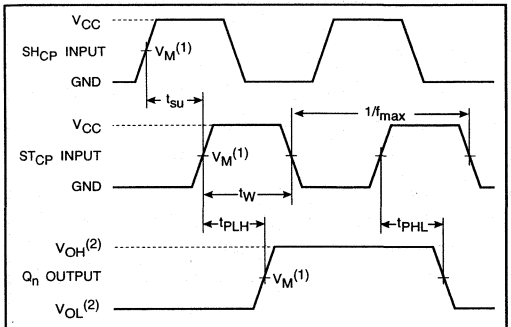


Fig.8 Waveforms showing the storage clock (ST_{CP}) to output (Q_n) propagation delays, the storage clock pulse width and the shift clock to storage clock set-up time.

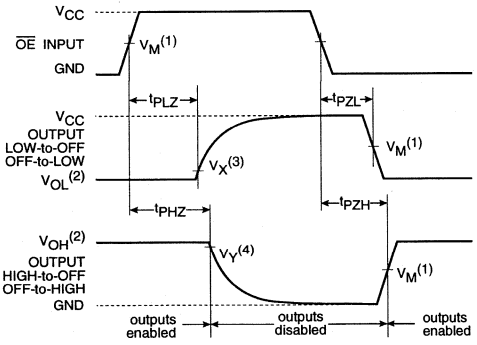


Fig.9 Waveforms showing the 3-state enable and disable times for input $\overline{OE}$.

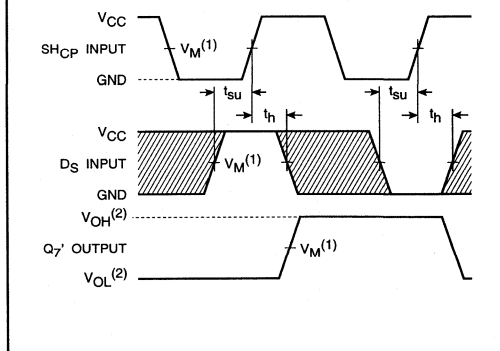
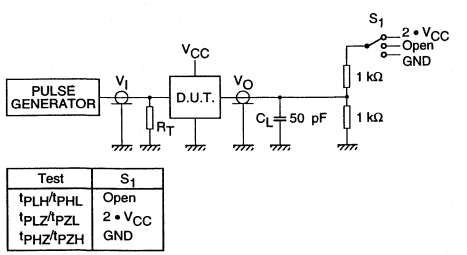


Fig.10 Waveforms showing the data set-up and hold times for the data input (D_S).



Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.11 Load circuitry for switching times.

Note to Fig.10

The shaded areas indicate when the input is permitted to change for predictable output performance.

Notes:

(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

AC WAVEFORMS *(Continued)*

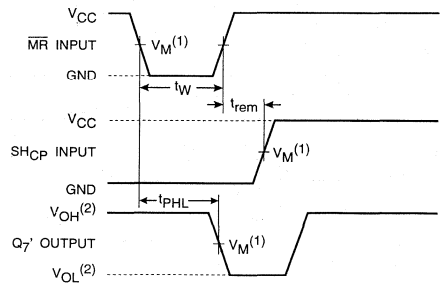


Fig. 12 Waveforms showing the master reset ($\overline{MR}$) pulse width, the master reset to output (Q_7') propagation delay and the master reset to shift clock (SH_{CP}) removal time.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

8-Channel analog multiplexer/demultiplexer 74LV4051

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 6.0 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Low typ "ON" resistance: 50 Ω at V_{CC} - V_{EE} = 4.5 V 70 Ω at V_{CC} - V_{EE} = 3.0 V 120 Ω at V_{CC} - V_{EE} = 2.0 V**
- **Logic level translation: to enable 3 V logic to communicate with ± 3 V analog signals**
- **Typical "break before make" built in**
- **Output capability: non-standard**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74LV4051 is a low-voltage CMOS device and is pin and function compatible with the 74HC/HCT4051.

The 74LV4051 is an 8-channel analog multiplexer/demultiplexer with three digital select inputs (S_0 to S_2), an active LOW enable input ($\overline{E}$), eight independent inputs/outputs (Y_0 to Y_7) and a common input/output (Z).

With $\overline{E}$ LOW, one of the eight switches is selected (low impedance ON-state) by S_0 to S_2. With $\overline{E}$ HIGH, all switches are in the high impedance OFF-state, independent of S_0 to S_2.

V_{CC} and GND are the supply voltage pins for the digital control inputs (S_0 to S_2, and $\overline{E}$). The V_{CC} to GND ranges are 1.0 to 6.0 V. The analog inputs/outputs (Y_0 to Y_7, and Z) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. V_{CC} - V_{EE} may not exceed 6.0 V. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PZH}/t_{PZL}	turn "ON" time $\overline{E}$ to V_{os} S_n to V_{os}	C_L = 15 pF R_L = 1KΩ V_{CC} = 3.3 V	 23 22	ns
t_{PHZ}/t_{PLZ}	turn "OFF" time $\overline{E}$ to V_{os} S_n to V_{os}		 25 20	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per switch	notes 1 and 2	25	pF
C_s	maximum switch capacitance independent (Y) common (Z)		 5 25	 pF pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma ((C_L + C_s) \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; C_s = max. switch capacitance in pF;
   V_{CC} = supply voltage in V;
   $\Sigma ((C_L + C_s) \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV4051N	16	DIL	plastic	DIL16/SOT38Z
74LV4051D	16	SO	plastic	SO16/SOT109A
74LV4051DB	16	SSOP	plastic	SSOP16/SOT338
74LV4051PW	16	TSSOP	plastic	TSSOP16/SOT403

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
3	Z	common input/output
6	$\overline{E}$	enable input (active LOW)
7	V_{EE}	negative supply voltage
8	GND	ground (0 V)
11, 10, 9	S_0 to S_2	select inputs
13, 14, 15, 12, 1, 5, 2, 4	Y_0 to Y_7	independent inputs/outputs
16	V_{CC}	positive supply voltage

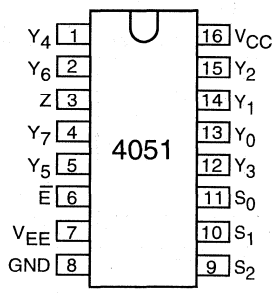


Fig.1 Pin configuration.

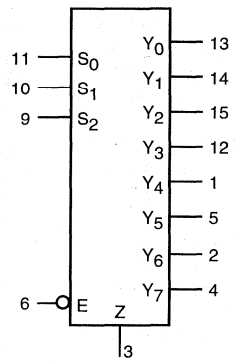


Fig.2 Logic symbol.

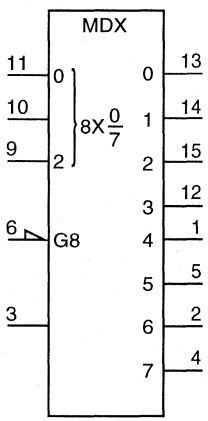


Fig.3 IEC Logic symbol.

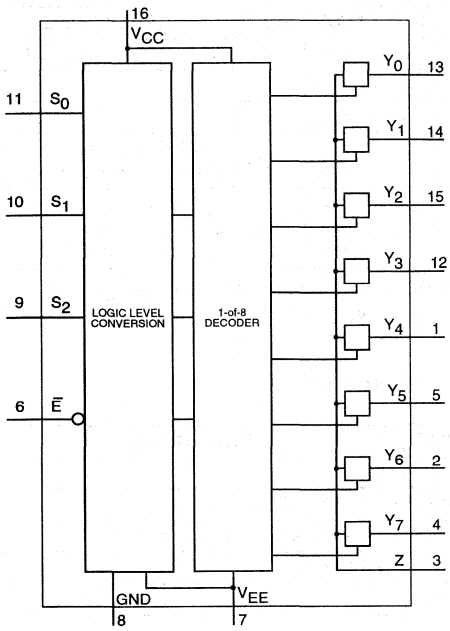


Fig.4 Functional diagram.

FUNCTION TABLE

INPUTS				CHANNEL ON
$\overline{E}$	S_2	S_1	S_0	
L	L	L	L	$Y_0 - Z$
L	L	L	H	$Y_1 - Z$
L	L	H	L	$Y_2 - Z$
L	L	H	H	$Y_3 - Z$
L	H	L	L	$Y_4 - Z$
L	H	L	H	$Y_5 - Z$
L	H	H	L	$Y_6 - Z$
L	H	H	H	$Y_7 - Z$
H	X	X	X	none

H = HIGH voltage level
L = LOW voltage level
X = don't care

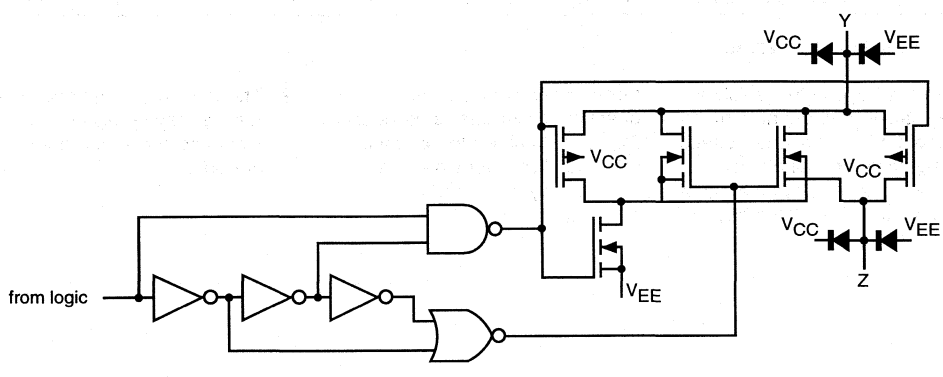


Fig.5 Schematic diagram (one switch).

RECOMMENDED OPERATING CONDITIONS FOR THE LV4051

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	1.0	3.3	6.0	V	see Fig.10 and note 1
V_I	input voltage	0	–	V_{CC}	V	
V_O	output voltage	0	–	V_{CC}	V	
T_{amb}	operating ambient temperature range in free air	−40 −40	– –	+85 +125	°C	see DC and AC characteristics per device
t_r, t_f	input rise and fall times except for Schmitt-trigger inputs	– – –	– – –	500 200 100	ns/V	V_{CC} = 1.0 V to 2.0 V V_{CC} = 2.0 V to 2.7 V V_{CC} = 2.7 V to 6.0 V

Notes: 1. The LV-HCMOS is guaranteed to function down to V_{CC} = 1.0 V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2 V to V_{CC} = 6.0 V.

ABSOLUTE MAXIMUM RATINGS FOR THE LV4051

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7.0	V	
$\pm I_{IK}$	DC input diode current	–	20	mA	$V_I < -0.5$ or $V_I > V_{CC}$ +0.5 V
$\pm I_{SK}$	DC switch diode current	–	20	mA	$V_S < -0.5$ or $V_S > V_{CC}$ +0.5 V
$\pm I_S$	DC switch current	–	25	mA	$-0.5\ V < V_S < V_{CC}$ +0.5 V
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package - plastic DIL - plastic mini-pack (SO) - plastic medium-shrink SO (SSOP)	 – – –	 750 500 500	 mW	for temperature range: −40 to +125 °C above + 70 °C derate linearly with 12 mW/K above + 70 °C derate linearly with 8 mW/K above + 60 °C derate linearly with 8 mW/K

Notes to the limiting values

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operating of the device at these or any other conditions beyond those under 'recommended operating conditions' is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS FOR 74LV4051

Over recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS		
		−40 to +85			−40 to +125			V_{CC} V	V_I	OTHER
		MIN.	TYP.	MAX.	MIN.	MAX.				
V_{IH}	HIGH level input voltage	0.90	–	–	0.90	–	V	1.2	–	
		1.40	–	–	1.40	–		2.0	–	
		2.00	–	–	2.00	–		2.7 to 3.6	–	
		3.15	–	–	3.15	–		4.5	–	
		4.20	–	–	4.20	–		6.0	–	
V_{IL}	LOW level input voltage	–	–	0.30	–	0.30	V	1.2	–	
		–	–	0.60	–	0.60		2.0	–	
		–	–	0.80	–	0.80		2.7 to 3.6	–	
		–	–	1.35	–	1.35		4.5	–	
		–	–	1.80	–	1.80		6.0	–	
$\pm I_I$	input leakage current	–	–	1.0	–	1.0	µA	3.6	V_{CC} or GND	
		–	–	2.0	–	2.0		6.0		
$\pm I_S$	analog switch OFF-state current per channel	–	–	1.0	–	1.0	µA	3.6	V_{IH} or V_{IL}	$\|V_S\| = V_{CC} - GND$ Fig.7
		–	–	2.0	–	2.0		6.0		
$\pm I_S$	analog switch ON-state current	–	–	1.0	–	1.0	µA	3.6	V_{IH} or V_{IL}	$\|V_S\| = V_{CC} - GND$ Fig.8
		–	–	2.0	–	2.0		6.0		
I_{CC}	quiescent supply current	–	–	20	–	40	µA	3.6	V_{CC} or GND	$V_{is} = GND$ or V_{CC}; $V_{os} = V_{CC}$ or GND
		–	–	40	–	80		6.0		
ΔI_{CC}	additional quiescent supply current per input	–	–	500	–	850	µA	2.7 to 3.6	$V_I = V_{CC} - 0.6$ V	

DC CHARACTERISTICS FOR 74LV4051 *(Continued)*

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS			
		−40 to +85			−40 to +125			V_{CC} V	I_S µA	V_{is}	V_I
		MIN.	TYP.	MAX.	MIN.	MAX.					
R_{ON}	ON-resistance (peak)	–	–	–	–	–	Ω	1.2	100	V_{CC} to GND	V_{IH} or V_{IL}
		–	145	270	–	375		2.0	1000		
		–	90	170	–	205		2.7 to 3.6	1000		
		–	60	115	–	135		4.5	1000		
R_{ON}	ON-resistance (rail)	–	225	–	–	–	Ω	1.2	100	GND	V_{IH} or V_{IL}
		–	110	215	–	250		2.0	1000		
		–	70	135	–	160		2.7 to 3.6	1000		
		–	45	90	–	105		4.5	1000		
R_{ON}	ON-resistance (rail)	–	250	–	–	–	Ω	1.2	100	V_{CC}	V_{IH} or V_{IL}
		–	120	240	–	290		2.0	1000		
		–	75	150	–	180		2.7 to 3.6	1000		
		–	50	100	–	120		4.5	1000		
ΔR_{ON}	maximum variation of ON-resistance between any two channels	–	–	–	–	–	Ω	1.2	–	V_{CC} to GND	V_{IH} or V_{IL}
		–	5	–	–	–		2.0	–		
		–	4	–	–	–		2.7 to 3.6	–		
		–	3	–	–	–		4.5	–		

Notes: (1) All typical values are measured at $T_{amb} = 25$ °C.

(2) At supply voltages approaching 1.2 V, the analog switch ON-resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.

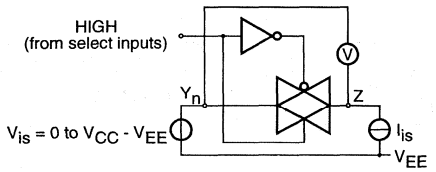


Fig.6 Test circuit for measuring ON-resistance (R_{ON}).

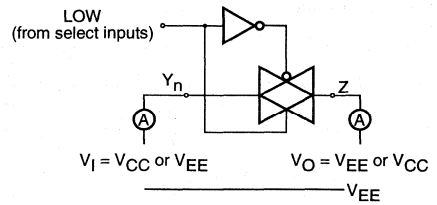


Fig.7 Test circuit for measuring OFF-state current.

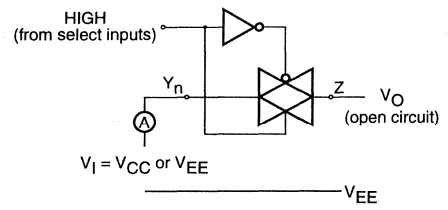


Fig.8 Test circuit for measuring ON-state current.

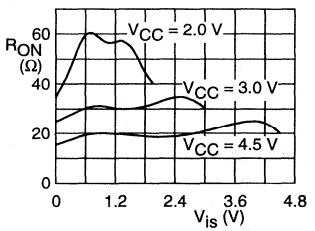


Fig.9 Typical ON-resistance (R_{ON}) as a function of input voltage (V_{is}) for V_{is} = 0 to V_{CC}–V_{EE}.

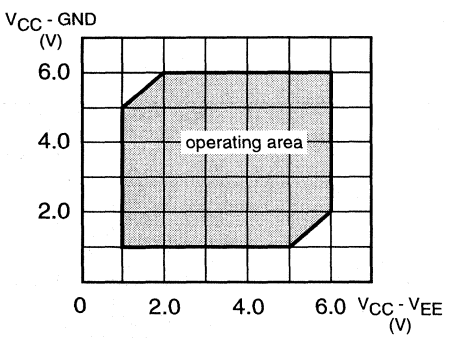


Fig.10 Guaranteed operating area as a function of the supply voltages

AC CHARACTERISTICS FOR 74LV4051

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	OTHER
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay V_{is} to V_{os}	–	25	–	–	–	ns	1.2	$R_L = \infty$; $C_L = 50$ pF Fig.18
		–	9	17	–	20		2.0	
		–	5*	10	–	12		2.7 to 3.6	
		–	4	9	–	10		4.5	
		–	3	8	–	8		6.0	
t_{PZH}/t_{PZL}	turn-on time $\overline{E}$ to V_{os}	–	145	–	–	–	ns	1.2	$R_L = 1$ kΩ; $C_L = 50$ pF Figs19, 20 and 21
		–	49	94	–	112		2.0	
		–	28*	55	–	66		2.7 to 3.6	
		–	25	47	–	56		4.5	
		–	19	38	–	43		6.0	
t_{PZH}/t_{PZL}	turn-on time S_n to V_{os}	–	140	–	–	–	ns	1.2	$R_L = 1$ kΩ; $C_L = 50$ pF Figs19, 20 and 21
		–	48	90	–	107		2.0	
		–	27*	53	–	63		2.7 to 3.6	
		–	24	45	–	54		4.5	
		–	18	34	–	41		6.0	
t_{PHZ}/t_{PLZ}	turn-off time $\overline{E}$ to V_{os}	–	145	–	–	–	ns	1.2	$R_L = 1$ kΩ; $C_L = 50$ pF Figs19, 20 and 21
		–	51	93	–	110		2.0	
		–	30*	56	–	66		2.7 to 3.6	
		–	29	48	–	56		4.5	
		–	21	37	–	44		6.0	
t_{PHZ}/t_{PLZ}	turn-off time S_n to V_{os}	–	115	–	–	–	ns	1.2	$R_L = 1$ kΩ; $C_L = 50$ pF Figs19, 20 and 21
		–	41	73	–	90		2.0	
		–	24*	44	–	54		2.7 to 3.6	
		–	22	37	–	46		4.5	
		–	17	29	–	36		6.0	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

ADDITIONAL AC CHARACTERISTICS FOR THE 74LV4051

Recommended conditions and typical values

GND = 0 V; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	TYP.	UNIT	V_{CC} (V)	$V_{is(p-p)}$ (V)	CONDITIONS
	sine-wave distortion f = 1 kHz	0.80 0.40	%	3.0 6.0	2.75 5.50	R_L = 10 kΩ; C_L = 50 pF Figs15 and 16
	sine-wave distortion f = 10 kHz	2.40 1.20	%	3.0 6.0	2.75 5.50	R_L = 10 kΩ; C_L = 50 pF Figs15 and 16
	switch 'OFF' signal feed through	−50 −50	dB	3.0 6.0	note 1	R_L = 600 Ω; C_L = 50 pF; f = 1 MHz Figs 11 and 17
	crosstalk between any two switches/multiplexers	−60 −60	dB	3.0 6.0	note 1	R_L = 600 Ω; C_L = 50 pF; f = 1 MHz Fig.13
$V_{(p-p)}$	crosstalk voltage between enable or address input to any switch (peak-to-peak value)	110 220	mV	3.0 6.0		R_L = 600 Ω; C_L = 50 pF; f = 1 MHz (S_n or $\overline{E}$, square wave between V_{CC} and GND, $t_r = t_f$ = 6 ns) Fig.14
f_{max}	minimum frequency response (−3 dB)	180 200	MHz	3.0 6.0	note 2	R_L = 50 Ω; C_L = 50 pF Figs 12, 15 and 14
C_S	maximum switch capacitance	5	pF			

Notes to the AC characteristics

General note

V_{is} is the input voltage at nY or nZ terminal, whichever is assigned as an input.

V_{os} is the output voltage at nY or nZ terminal, whichever is assigned as an output.

Notes

1. Adjust input voltage V_{is} is 0 dBm level (0 dBm = 1 mW into 600 Ω).
2. Adjust input voltage V_{is} is 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).

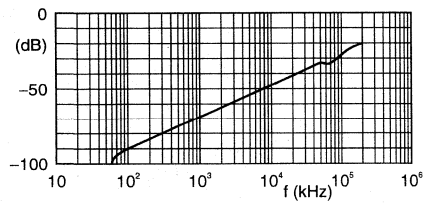


Fig.11 Typical switch 'OFF' signal feed-through as a function of frequency.

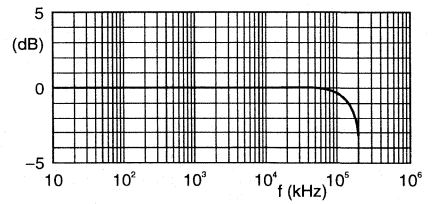


Fig.12 Typical frequency response.

Note to figs 11 and 12

Test conditions: V_{CC} = 3.0 V; GND = 0 V; V_{EE} = −3.0V; R_L = 50 Ω; R_{source} = 1 kΩ.

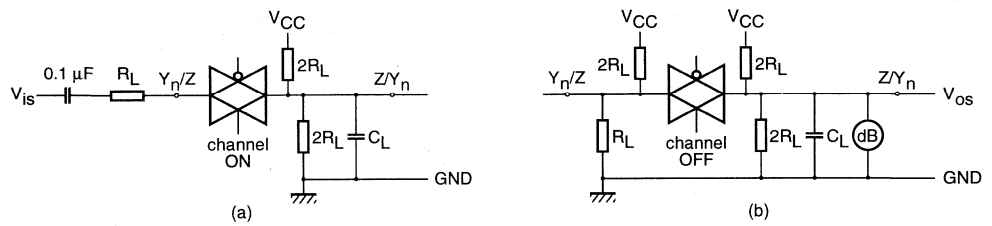


Fig.13 Test circuit for measuring crosstalk between any two switches.
(a) channel ON condition; (b) channel OFF condition.

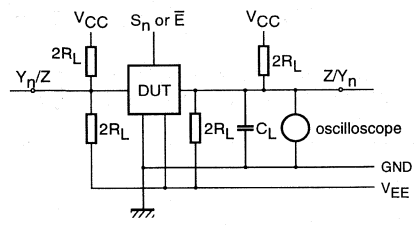
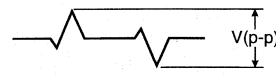


Fig.14 Test circuit for measuring crosstalk between control and any switch.

Note to fig.14

The crosstalk is defined as follows (oscilloscope output):



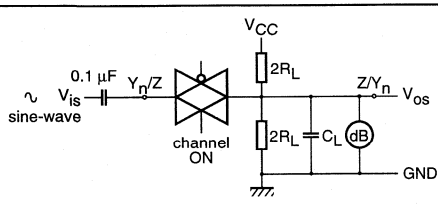


Fig.15 Test circuit for measuring minimum frequency response.

Note to fig.15

Adjust input voltage to obtain 0 dBm at V_{os} when f_{in} = 1 MHz. After set-up frequency of f_{in} is increased to obtain a reading of −3 dB at V_{os}.

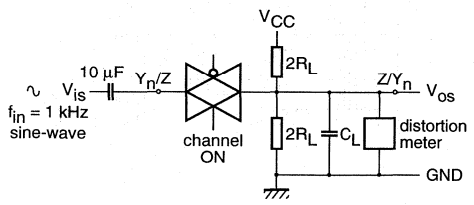


Fig.16 Test circuit for measuring sine-wave distortion.

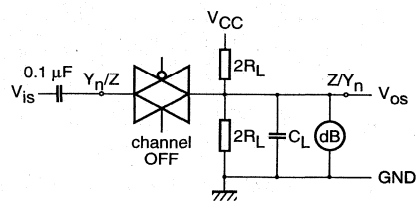


Fig.17 Test circuit for measuring switch 'OFF' signal feed-through.

AC WAVEFORMS

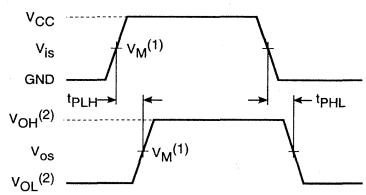


Fig.18 Waveforms showing the input (V_{is}) to output (V_{os}) propagation delays.

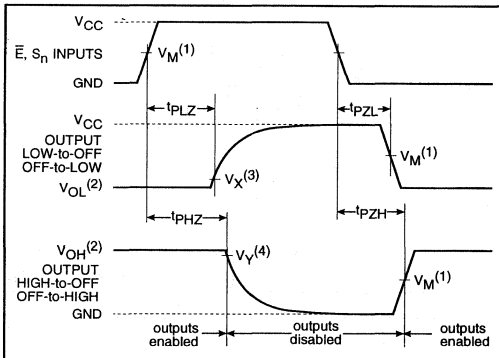


Fig.19 Waveforms showing the turn-on and turn-off times for the inputs (S_n, $\overline{E}$) to the output (V_{os})

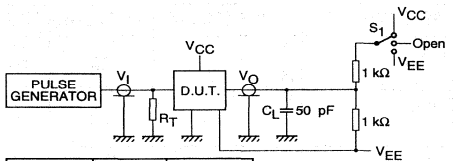
Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

TEST CIRCUIT AND WAVEFORMS



Test	S_1	V_{IS}
t_{PLH}/t_{PHL}	Open	Pulse
t_{PLZ}/t_{PZL}	V_{CC}	V_{EE}
t_{PHZ}/t_{PZH}	V_{EE}	V_{CC}

Fig.20 Test circuit for measuring AC performance.

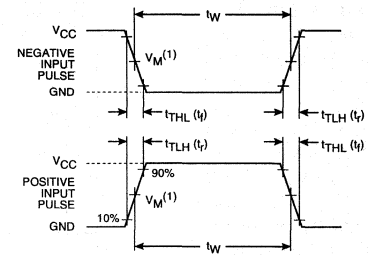


Fig.21 Input (S_n and $\overline{E}$) pulse definitions.

Definitions for figs 20 and 21:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns, when measuring f_{max}, there is no constraint on t_r, t_f with 50% duty factor.

Notes: (1) V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
$V_M = 0.5 \cdot V_{CC}$ at V_{CC} < 2.7 V

Dual 4-channel analog multiplexer/demultiplexer 74LV4052

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 6.0 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Low typ "ON" resistance: 60 Ω at V_{CC} - V_{EE} = 4.5 V 90 Ω at V_{CC} - V_{EE} = 3.0 V 145 Ω at V_{CC} - V_{EE} = 2.0 V**
- **Logic level translation: to enable 3 V logic to communicate with ± 3 V analog signals**
- **Typical "break before make" built in**
- **Analog/Digital multiplexing and demultiplexing**
- **Signal gating**
- **Output capability: non-standard**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74LV4052 is a low-voltage CMOS device and is pin and function compatible with the 74HC/HCT4052.

The 74LV4052 is a dual 4-channel analog multiplexer/demultiplexer with common select logic. Each multiplexer has four independent inputs/outputs (nY_0 to nY_3) and a common input/output (nZ). The common channel select logics include two digital select inputs (S_0 and S_1) and an active LOW enable input ($\overline{E}$). With $\overline{E}$ LOW, one of the four switches is selected (low impedance ON-state) by S_0 and S_1.
With $\overline{E}$ HIGH, all switches are in the high impedance OFF-state, independent of S_0 and S_1. V_{CC} and GND are the supply voltage pins for the digital control inputs (S_0, S_1, and $\overline{E}$). The V_{CC} to GND ranges are 1.0 to 6.0 V. The analog inputs/outputs (nY_0 to nY_3, and nZ) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit.
$V_{CC} - V_{EE}$ may not exeed 6.0 V.
For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PZH}/t_{PZL}	turn "ON" time $\overline{E}$ or S_n V_{os}	C_L = 15 pF, R_L = 1KΩ, V_{CC} = 3.3 V	30	ns
t_{PHZ}/t_{PLZ}	turn "OFF" time $\overline{E}$ or S_n V_{os}		22	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per switch	notes 1 and 2	57	pF
C_s	max. switch capacitance independent (Y) common (Z)		5 12	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma ((C_L + C_s) \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; C_s = max. switch capacitance in pF;
   V_{CC} = supply voltage in V;
   $\Sigma ((C_L + C_s) \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV4052N	16	DIL	plastic	DIL16/SOT38Z
74LV4052D	16	SO	plastic	SO16/SOT109A
74LV4052DB	16	SSOP	plastic	SSOP16/SOT338
74LV4052PW	16	TSSOP	plastic	TSSOP16/SOT403

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 5, 2, 4	$2Y_0$ to $2Y_3$	independent inputs/outputs
6	$\overline{E}$	enable input (active LOW)
7	V_{EE}	negative supply voltage
8	GND	ground (0 V)
10, 9	S_0, S_1	select inputs
12, 14, 15, 11	$1Y_0$ to $1Y_3$	independent inputs/outputs
13, 3	1Z, 2Z	common inputs/outputs
16	V_{CC}	positive supply voltage

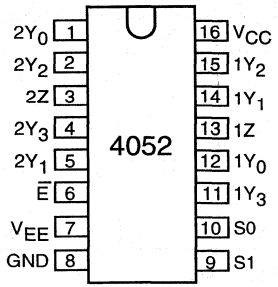


Fig.1 Pin configuration.

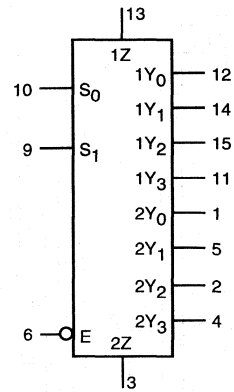


Fig.2 Logic symbol.

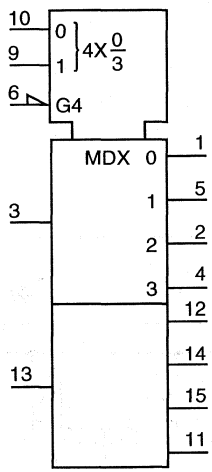


Fig.3 IEC Logic symbol.

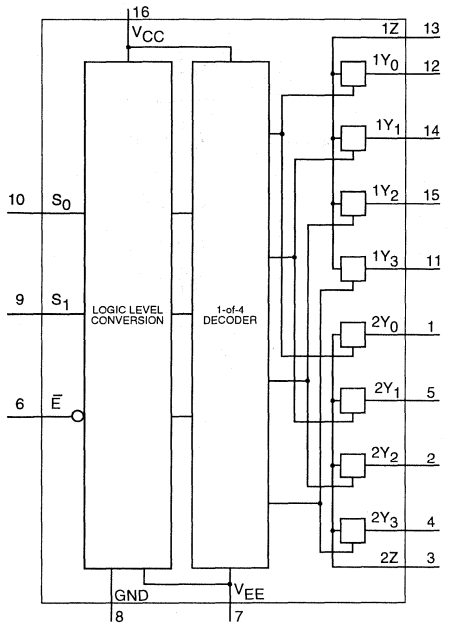


Fig.4 Functional diagram.

FUNCTION TABLE

INPUTS			CHANNEL ON
$\overline{E}$	S_1	S_0	
L	L	L	$nY_0 - nZ$
L	L	H	$nY_1 - nZ$
L	H	L	$nY_2 - nZ$
L	H	H	$nY_3 - nZ$
H	X	X	none

H = HIGH voltage level
L = LOW voltage level
X = don't care

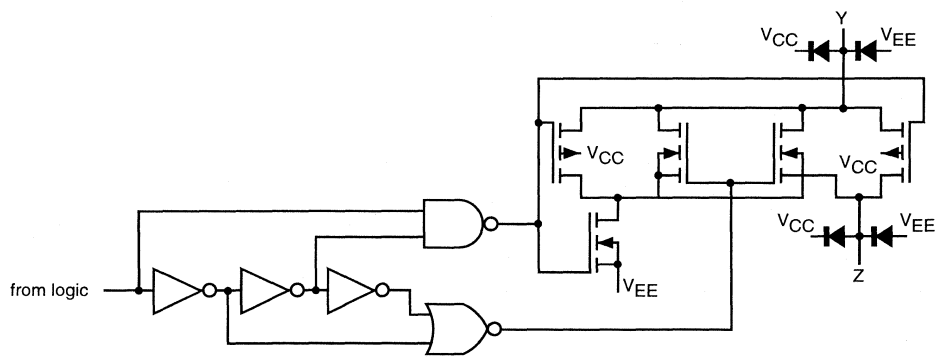


Fig.5 Schematic diagram (one switch).

RECOMMENDED OPERATING CONDITIONS FOR THE LV4052

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	1.0	3.3	6.0	V	see Fig.10 and note 1
V_I	input voltage	0	–	V_{CC}	V	
V_O	output voltage	0	–	V_{CC}	V	
T_{amb}	operating ambient temperature range in free air	–40 –40	– –	+85 +125	°C	see DC and AC characteristics per device
t_r, t_f	input rise and fall times except for Schmitt-trigger inputs	– – –	– – –	500 200 100	ns/V	V_{CC} = 1.0 V to 2.0 V V_{CC} = 2.0 V to 2.7 V V_{CC} = 2.7 V to 6.0 V

Notes: 1. The LV-HCMOS is guaranteed to function down to V_{CC} = 1.0 V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2 V to V_{CC} = 6.0 V.

ABSOLUTE MAXIMUM RATINGS FOR THE LV4052

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	–0.5	+7.0	V	
$\pm I_{IK}$	DC input diode current	–	20	mA	$V_I < -0.5$ or $V_I > V_{CC}$ +0.5 V
$\pm I_{SK}$	DC switch diode current	–	20	mA	$V_S < -0.5$ or $V_S > V_{CC}$ +0.5 V
$\pm I_S$	DC switch current	–	25	mA	–0.5 V < V_S < V_{CC} +0.5 V
T_{stg}	storage temperature range	–65	+150	°C	
P_{tot}	power dissipation per package - plastic DIL - plastic mini-pack (SO) - plastic medium-shrink SO (SSOP)	 – – –	 750 500 500	 mW	for temperature range: –40 to +125 °C above + 70 °C derate linearly with 12 mW/K above + 70 °C derate linearly with 8 mW/K above + 60 °C derate linearly with 8 mW/K

Notes to the limiting values

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operating of the device at these or any other conditions beyond those under 'recommended operating conditions' is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS FOR 74LV4052

Over recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS		
		−40 to +85			−40 to +125			V_{CC}	V_I	OTHER
		MIN.	TYP.	MAX.	MIN.	MAX.		V		
V_{IH}	HIGH level input voltage	0.90	–	–	0.90	–	V	1.2	–	
		1.40	–	–	1.40	–		2.0	–	
		2.00	–	–	2.00	–		2.7 to 3.6	–	
		3.15	–	–	3.15	–		4.5	–	
		4.20	–	–	4.20	–		6.0	–	
V_{IL}	LOW level input voltage	–	–	0.30	–	0.30	V	1.2	–	
		–	–	0.60	–	0.60		2.0	–	
		–	–	0.80	–	0.80		2.7 to 3.6	–	
		–	–	1.35	–	1.35		4.5	–	
		–	–	1.80	–	1.80		6.0	–	
$\pm I_I$	input leakage current	–	–	1.0	–	1.0	µA	3.6	V_{CC} or GND	
		–	–	2.0	–	2.0		6.0		
$\pm I_S$	analog switch OFF-state current per channel	–	–	1.0	–	1.0	µA	3.6	V_{IH} or V_{IL}	$\|V_S\| = V_{CC} - GND$ Fig.7
		–	–	2.0	–	2.0		6.0		
$\pm I_S$	analog switch ON-state current	–	–	1.0	–	1.0	µA	3.6	V_{IH} or V_{IL}	$\|V_S\| = V_{CC} - GND$ Fig.8
		–	–	2.0	–	2.0		6.0		
I_{CC}	quiescent supply current	–	–	20	–	40	µA	3.6	V_{CC} or GND	V_{is} = GND or V_{CC}; V_{os} = V_{CC} or GND
		–	–	40	–	80		6.0		
ΔI_{CC}	additional quiescent supply current per input	–	–	500	–	850	µA	2.7 to 3.6	$V_I = V_{CC} - 0.6$ V	

DC CHARACTERISTICS FOR 74LV4052 ***(Continued)***

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS			
		−40 to +85			−40 to +125			V_{CC}	I_S	V_{is}	V_I
		MIN.	TYP.	MAX.	MIN.	MAX.		V	µA		
R_{ON}	ON-resistance (peak)	–	–	–	–	–	Ω	1.2	100	V_{CC} to GND	V_{IH} or V_{IL}
		–	145	270	–	375		2.0	1000		
		–	90	170	–	205		2.7 to 3.6	1000		
		–	60	115	–	135		4.5	1000		
R_{ON}	ON-resistance (rail)	–	225	–	–	–	Ω	1.2	100	GND	V_{IH} or V_{IL}
		–	110	215	–	250		2.0	1000		
		–	70	135	–	160		2.7 to 3.6	1000		
		–	45	90	–	105		4.5	1000		
R_{ON}	ON-resistance (rail)	–	250	–	–	–	Ω	1.2	100	V_{CC}	V_{IH} or V_{IL}
		–	120	240	–	290		2.0	1000		
		–	75	150	–	180		2.7 to 3.6	1000		
		–	50	100	–	120		4.5	1000		
ΔR_{ON}	maximum variation of ON-resistance between any two channels	–	–	–	–	–	Ω	1.2	–	V_{CC} to GND	V_{IH} or V_{IL}
		–	5	–	–	–		2.0	–		
		–	4	–	–	–		2.7 to 3.6	–		
		–	3	–	–	–		4.5	–		

Notes: (1) All typical values are measured at T_{amb} = 25 °C.

(2) At supply voltages approaching 1.2 V, the analog switch ON-resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.

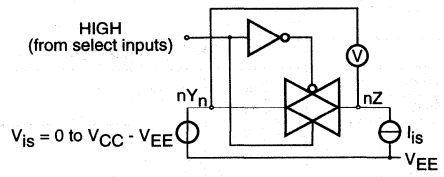


Fig.6 Test circuit for measuring ON-resistance (R_{ON}).

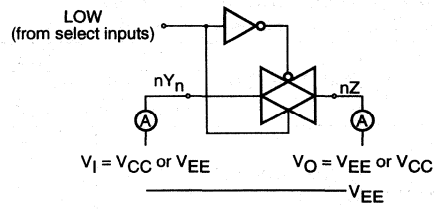


Fig.7 Test circuit for measuring OFF-state current.

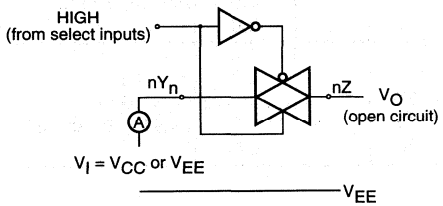


Fig.8 Test circuit for measuring ON-state current.

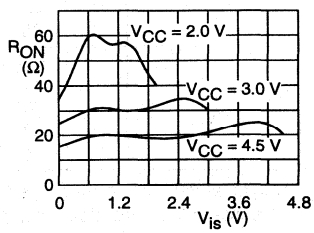


Fig.9 Typical ON-resistance (R_{ON}) as a function of input voltage (V_{is}) for V_{is} = 0 to V_{CC}–V_{EE}.

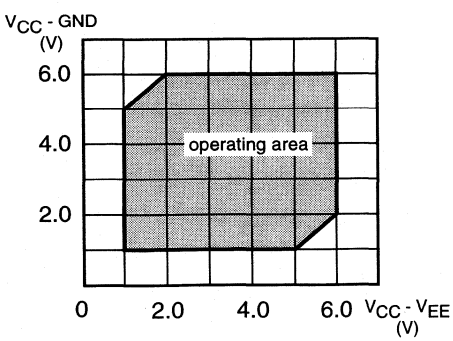


Fig.10 Guaranteed operating area as a function of the supply voltages

AC CHARACTERISTICS FOR 74LV4052

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	OTHER
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay V_{is} to V_{os}	–	25	–	–	–	ns	1.2	$R_L = \infty$; $C_L = 50$ pF Fig.18
		–	9	17	–	20		2.0	
		–	5*	10	–	12		2.7 to 3.6	
		–	4	9	–	10		4.5	
		–	3	8	–	8		6.0	
t_{PZH}/t_{PZL}	turn-on time $\overline{E}$, S_n to V_{os}	–	190	–	–	–	ns	1.2	$R_L = 1$ kΩ; $C_L = 50$ pF Figs19, 20 and 21
		–	65	121	–	146		2.0	
		–	36*	71	–	86		2.7 to 3.6	
		–	32	60	–	73		4.5	
		–	25	46	–	56		6.0	
t_{PHZ}/t_{PLZ}	turn-off time $\overline{E}$, S_n to V_{os}	–	125	–	–	–	ns	1.2	$R_L = 1$ kΩ; $C_L = 50$ pF Figs19, 20 and 21
		–	43	80	–	95		2.0	
		–	26*	48	–	57		2.7 to 3.6	
		–	23	41	–	49		4.5	
		–	18	32	–	38		6.0	

Notes: All typical values are measured at $T_{amb} = 25$ °C.

* Typical values are measured at $V_{CC} = 3.3$ V.

ADDITIONAL AC CHARACTERISTICS FOR THE 74LV4052

Recommended conditions and typical values

GND = 0 V; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	TYP.	UNIT	V_{CC} (V)	$V_{is(p-p)}$ (V)	CONDITIONS
	sine-wave distortion f = 1 kHz	0.80 0.40	%	3.0 6.0	2.75 5.50	R_L = 10 kΩ; C_L = 50 pF Figs15 and 16
	sine-wave distortion f = 10 kHz	2.40 1.20	%	3.0 6.0	2.75 5.50	R_L = 10 kΩ; C_L = 50 pF Figs15 and 16
	switch 'OFF' signal feed through	−50 −50	dB	3.0 6.0	note 1	R_L = 600 Ω; C_L = 50 pF; f = 1 MHz Figs 11 and 17
	crosstalk between any two switches/multiplexers	−60 −60	dB	3.0 6.0	note 1	R_L = 600 Ω; C_L = 50 pF; f = 1 MHz Fig.13
$V_{(p-p)}$	crosstalk voltage between enable or address input to any switch (peak-to-peak value)	110 220	mV	3.0 6.0		R_L = 600 Ω; C_L = 50 pF; f = 1 MHz (S_n or $\overline{E}$, square wave between V_{CC} and GND, $t_r = t_f$ = 6 ns) Fig.14
f_{max}	minimum frequency response (−3 dB)	180 200	MHz	3.0 6.0	note 2	R_L = 50 Ω; C_L = 50 pF Figs 12, 15 and 14
C_S	maximum switch capacitance	5	pF			

Notes to the AC characteristics

General note

V_{is} is the input voltage at nY or nZ terminal, whichever is assigned as an input.

V_{os} is the output voltage at nY or nZ terminal, whichever is assigned as an output.

Notes

1. Adjust input voltage V_{is} is 0 dBm level (0 dBm = 1 mW into 600 Ω).
2. Adjust input voltage V_{is} is 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).

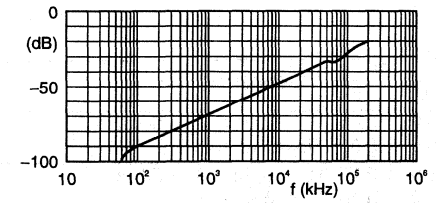


Fig.11 Typical switch 'OFF' signal feed-through as a function of frequency.

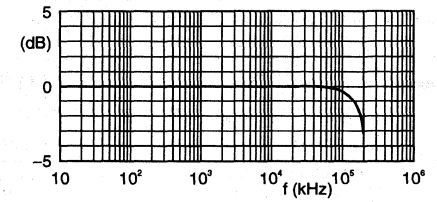


Fig.12 Typical frequency response.

Note to figs 11 and 12

Test conditions: V_{CC} = 3.0 V; GND = 0 V; V_{EE} = −3.0V; R_L = 50 Ω; R_{source} = 1 kΩ.

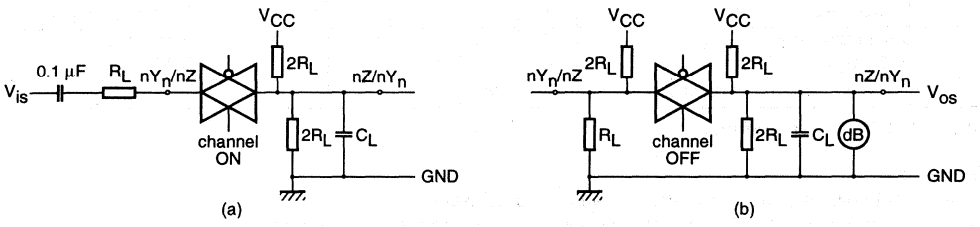


Fig.13 Test circuit for measuring crosstalk between any two switches.
(a) channel ON condition; (b) channel OFF condition.

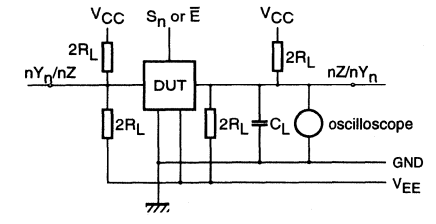
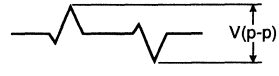


Fig.14 Test circuit for measuring crosstalk between control and any switch.

Note to fig.14

The crosstalk is defined as follows (oscilloscope output):



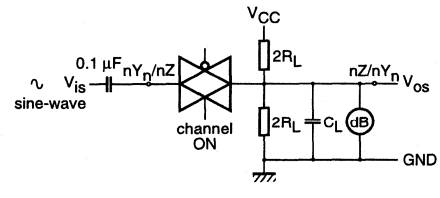


Fig.15 Test circuit for measuring minimum frequency response.

Note to fig.15

Adjust input voltage to obtain 0 dBm at V_{os} when f_{in} = 1 MHz. After set-up frequency of f_{in} is increased to obtain a reading of −3 dB at V_{os}.

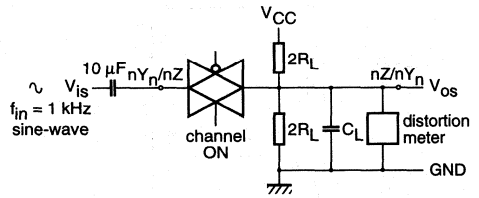


Fig.16 Test circuit for measuring sine-wave distortion.

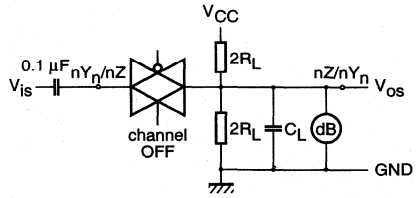


Fig.17 Test circuit for measuring switch 'OFF' signal feed-through.

AC WAVEFORMS

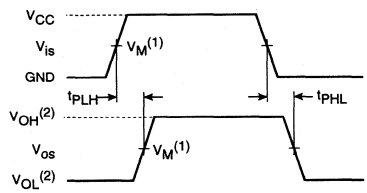


Fig.18 Waveforms showing the input (V_{is}) to output (V_{os}) propagation delays.

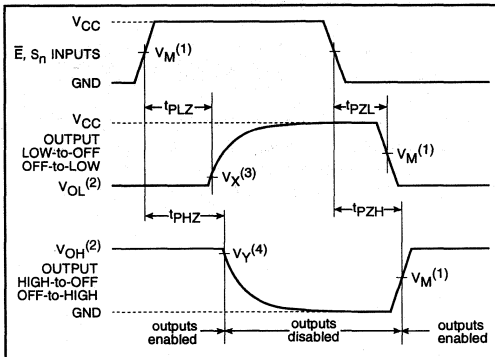


Fig.19 Waveforms showing the turn-on and turn-off times for the inputs (S_n, $\overline{E}$) to the output (V_{os})

Notes:

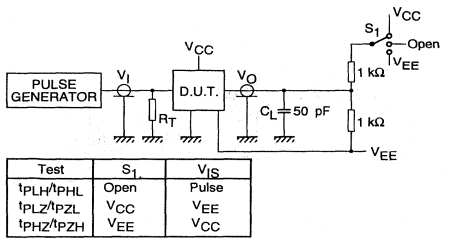
(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

TEST CIRCUIT AND WAVEFORMS



Test	S_1	V_{IS}
t_{PLH}/t_{PHL}	Open	Pulse
t_{PLZ}/t_{PZL}	V_{CC}	V_{EE}
t_{PHZ}/t_{PZH}	V_{EE}	V_{CC}

Fig.20 Test circuit for measuring AC performance.

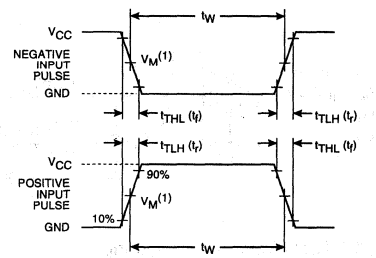


Fig.21 Input (S_n and $\overline{E}$) pulse definitions.

Definitions for figs 20 and 21:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns, when measuring f_{max}, there is no constraint on t_r, t_f with 50% duty factor.

Notes: (1) V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
V_M = 0.5 · V_{CC} at V_{CC} < 2.7 V

Triple 2-channel analog multiplexer/demultiplexer 74LV4053

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 6.0 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Low typ "ON" resistance: 50 Ω at V_{CC} - V_{EE} = 4.5 V 70 Ω at V_{CC} - V_{EE} = 3.0 V 120 Ω at V_{CC} - V_{EE} = 2.0 V**
- **Logic level translation: to enable 3 V logic to communicate with ± 3 V analog signals**
- **Typical "break before make" built in**
- **Output capability: non-standard**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74LV4053 is a low-voltage CMOS device and is pin and function compatible with the 74HC/HCT4053.

The 74LV4053 is a triple 2-channel analog multiplexer/demultiplexer with a common enable input ($\overline{E}$). Each multiplexer/demultiplexer has two independent inputs/outputs (nY_0 to nY_1), a common input/output (nZ) and three digital select inputs (S_1 to S_3).
With $\overline{E}$ LOW, one of the two switches is selected (low impedance ON-state) by S_1 to S_3. With $\overline{E}$ HIGH, all switches are in the high impedance OFF-states, independent of S_1 and S_3.

V_{CC} and GND are the supply voltage pins for the digital control inputs (S_1 to S_3, and $\overline{E}$). The V_{CC} to GND ranges are 1.0 to 6.0 V.
The analog inputs/outputs (nY_0 to nY_1, and nZ) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. V_{CC} - V_{EE} may not exceed 6.0 V.
For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PZH}/t_{PZL}	turn "ON" time $\overline{E}$ to V_{os} S_n to V_{os}	C_L = 15 pF R_L = 1KΩ V_{CC} = 3.3 V	 16 20	ns
t_{PHZ}/t_{PLZ}	turn "OFF" time $\overline{E}$ to V_{os} S_n to V_{os}		 17 16	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per switch	notes 1 and 2	36	pF
C_s	maximum switch capacitance independent (Y) common (Z)		 5 8	 pF pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma ((C_L + C_s) \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; C_s = max. switch capacitance in pF;
   V_{CC} = supply voltage in V;
   $\Sigma ((C_L + C_s) \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV4053N	16	DIL	plastic	DIL16/SOT38Z
74LV4053D	16	SO	plastic	SO16/SOT109A
74LV4053DB	16	SSOP	plastic	SSOP16/SOT338
74LV4053PW	16	TSSOP	plastic	TSSOP16/SOT403

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
2, 1	$2Y_0$, $2Y_1$	independent inputs/outputs
5, 3	$3Y_0$, $3Y_1$	independent inputs/outputs
6	$\overline{E}$	enable input (active LOW)
7	V_{EE}	negative supply voltage
8	GND	ground (0 V)
11, 10, 9	S_1 to S_3	select inputs
12, 13	$1Y_0$, $1Y_1$	independent inputs/outputs
14, 15, 4	1Z to 3Z	common inputs/outputs
16	V_{CC}	positive supply voltage

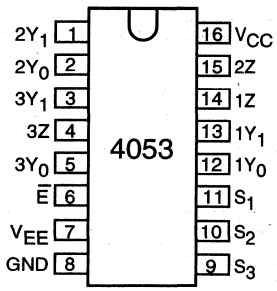


Fig.1 Pin configuration.

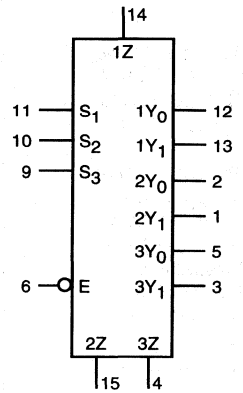


Fig.2 Logic symbol.

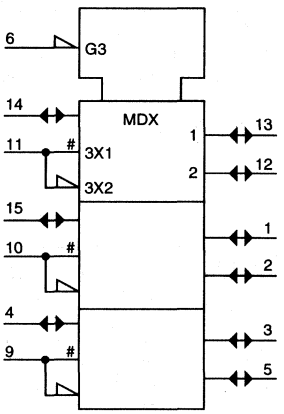


Fig.3 IEC Logic symbol.

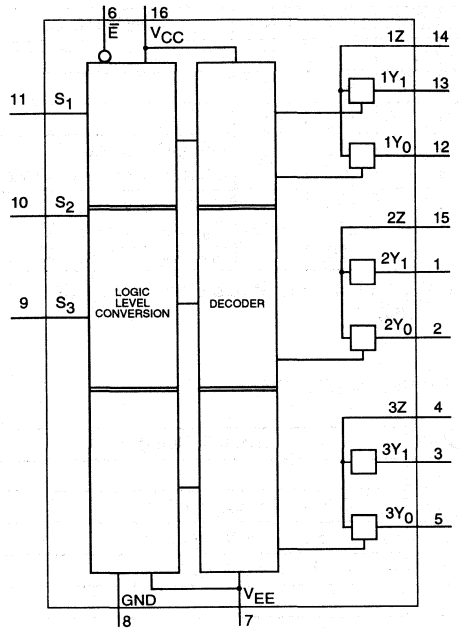


Fig.4 Functional diagram.

FUNCTION TABLE

INPUTS		CHANNEL ON
$\overline{E}$	S_2	
L	L	$nY_0 - nZ$
L	H	$nY_1 - nZ$
H	X	none

H = HIGH voltage level
L = LOW voltage level
X = don't care

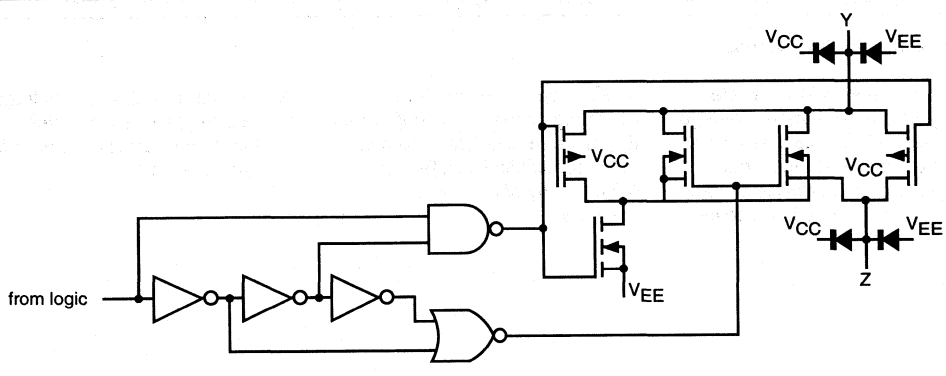


Fig.5 Schematic diagram (one switch).

RECOMMENDED OPERATING CONDITIONS FOR THE LV4053

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	1.0	3.3	6.0	V	Fig.10 and note 1
V_I	input voltage	0	–	V_{CC}	V	
V_O	output voltage	0	–	V_{CC}	V	
T_{amb}	operating ambient temperature range in free air	–40 –40	– –	+85 +125	°C	see DC and AC characteristics per device
t_r, t_f	input rise and fall times except for Schmitt-trigger inputs	– – –	– – –	500 200 100	ns/V	V_{CC} = 1.0 V to 2.0 V V_{CC} = 2.0 V to 2.7 V V_{CC} = 2.7 V to 6.0 V

Notes: 1. The LV-HCMOS is guaranteed to function down to V_{CC} = 1.0 V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2 V to V_{CC} = 6.0 V.

ABSOLUTE MAXIMUM RATINGS FOR THE LV4053

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	–0.5	+7.0	V	
$\pm I_{IK}$	DC input diode current	–	20	mA	$V_I < -0.5$ or $V_I > V_{CC}$ +0.5 V
$\pm I_{SK}$	DC switch diode current	–	20	mA	$V_S < -0.5$ or $V_S > V_{CC}$ +0.5 V
$\pm I_S$	DC switch current	–	25	mA	$-0.5\ V < V_S < V_{CC}$ +0.5 V
T_{stg}	storage temperature range	–65	+150	°C	
P_{tot}	power dissipation per package - plastic DIL - plastic mini-pack (SO) - plastic medium-shrink SO (SSOP)	 – – –	 750 500 500	 mW	for temperature range: –40 to +125 °C above + 70 °C derate linearly with 12 mW/K above + 70 °C derate linearly with 8 mW/K above + 60 °C derate linearly with 8 mW/K

Notes to the limiting values

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operating of the device at these or any other conditions beyond those under 'recommended operating conditions' is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS FOR 74LV4053

Over recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS		
		−40 to +85			−40 to +125			V_{CC}	V_I	OTHER
		MIN.	TYP.	MAX.	MIN.	MAX.		V		
V_{IH}	HIGH level input voltage	0.90	–	–	0.90	–	V	1.2	–	
		1.40	–	–	1.40	–		2.0	–	
		2.00	–	–	2.00	–		2.7 to 3.6	–	
		3.15	–	–	3.15	–		4.5	–	
		4.20	–	–	4.20	–		6.0	–	
V_{IL}	LOW level input voltage	–	–	0.30	–	0.30	V	1.2	–	
		–	–	0.60	–	0.60		2.0	–	
		–	–	0.80	–	0.80		2.7 to 3.6	–	
		–	–	1.35	–	1.35		4.5	–	
		–	–	1.80	–	1.80		6.0	–	
$\pm I_I$	input leakage current	–	–	1.0	–	1.0	µA	3.6	V_{CC} or GND	
		–	–	2.0	–	2.0		6.0		
$\pm I_S$	analog switch OFF-state current per channel	–	–	1.0	–	1.0	µA	3.6	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - GND$ Fig.7
		–	–	2.0	–	2.0		6.0		
$\pm I_S$	analog switch ON-state current	–	–	1.0	–	1.0	µA	3.6	V_{IH} or V_{IL}	$\lvert V_S \rvert = V_{CC} - GND$ Fig.8
		–	–	2.0	–	2.0		6.0		
I_{CC}	quiescent supply current	–	–	20	–	40	µA	3.6	V_{CC} or GND	V_{is} = GND or V_{CC}; V_{os} = V_{CC} or GND
		–	–	40	–	80		6.0		
ΔI_{CC}	additional quiescent supply current per input	–	–	500	–	850	µA	2.7 to 3.6	$V_I = V_{CC} - 0.6$ V	

DC CHARACTERISTICS FOR 74LV4053 *(Continued)*

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS			
		−40 to +85			−40 to +125			V_{CC}	I_S	V_{is}	V_I
		MIN.	TYP.	MAX.	MIN.	MAX.		V	µA		
R_{ON}	ON-resistance (peak)	–	–	–	–	–	Ω	1.2	100	V_{CC} to GND	V_{IH} or V_{IL}
		–	240	480	–	580		2.0	1000		
		–	150	300	–	360		2.7 to 3.6	1000		
		–	100	200	–	240		4.5	1000		
R_{ON}	ON-resistance (rail)	–	325	–	–	–	Ω	1.2	100	GND	V_{IH} or V_{IL}
		–	160	325	–	385		2.0	1000		
		–	100	205	–	240		2.7 to 3.6	1000		
		–	65	135	–	160		4.5	1000		
R_{ON}	ON-resistance (rail)	–	425	–	–	–	Ω	1.2	100	V_{CC}	V_{IH} or V_{IL}
		–	205	420	–	505		2.0	1000		
		–	130	265	–	315		2.7 to 3.6	1000		
		–	85	175	–	210		4.5	1000		
ΔR_{ON}	maximum variation of ON-resistance between any two channels	–	–	–	–	–	Ω	1.2	–	V_{CC} to GND	V_{IH} or V_{IL}
		–	5	–	–	–		2.0	–		
		–	4	–	–	–		2.7 to 3.6	–		
		–	3	–	–	–		4.5	–		

Notes: (1) All typical values are measured at T_{amb} = 25 °C.

(2) At supply voltages approaching 1.2 V, the analog switch ON-resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.

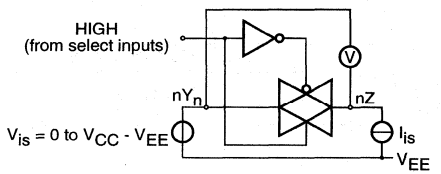


Fig.6 Test circuit for measuring ON-resistance (R_{ON}).

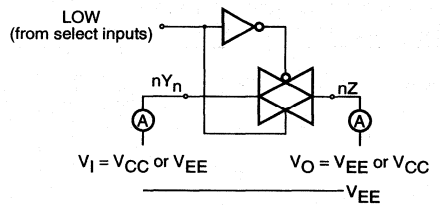


Fig.7 Test circuit for measuring OFF-state current.

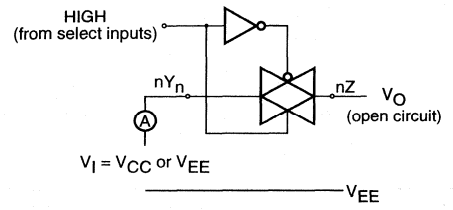


Fig.8 Test circuit for measuring ON-state current.

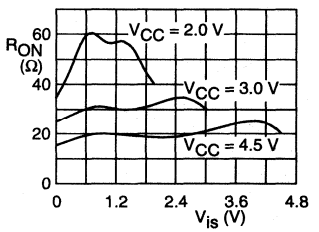


Fig.9 Typical ON-resistance (R_{ON}) as a function of input voltage (V_{is}) for V_{is} = 0 to V_{CC}–V_{EE}.

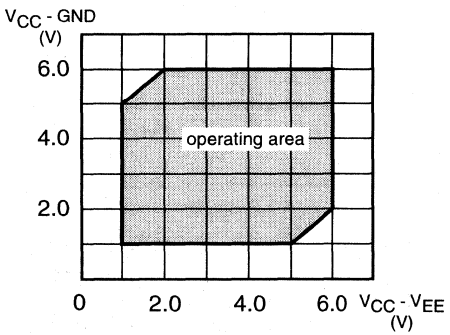


Fig.10 Guaranteed operating area as a function of the supply voltages

AC CHARACTERISTICS FOR 74LV4053

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	OTHER
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay V_{is} to V_{os}	–	25	–	–	–	ns	1.2	$R_L = \infty$; $C_L = 50$ pF Fig.18
		–	9	17	–	20		2.0	
		–	5*	10	–	12		2.7 to 3.6	
		–	4	9	–	10		4.5	
		–	3	8	–	8		6.0	
t_{PZH}/t_{PZL}	turn-on time $\overline{E}$ to V_{os}	–	100	–	–	–	ns	1.2	$R_L = 1$ kΩ; $C_L = 50$ pF Figs19, 20 and 21
		–	34	65	–	77		2.0	
		–	19*	38	–	45		2.7 to 3.6	
		–	17	32	–	38		4.5	
		–	13	25	–	29		6.0	
t_{PZH}/t_{PZL}	turn-on time S_n to V_{os}	–	125	–	–	–	ns	1.2	$R_L = 1$ kΩ; $C_L = 50$ pF Figs19, 20 and 21
		–	43	82	–	97		2.0	
		–	24*	48	–	57		2.7 to 3.6	
		–	21	41	–	48		4.5	
		–	16	31	–	37		6.0	
t_{PHZ}/t_{PLZ}	turn-off time $\overline{E}$ to V_{os}	–	95	–	–	–	ns	1.2	$R_L = 1$ kΩ; $C_L = 50$ pF Figs19, 20 and 21
		–	34	61	–	73		2.0	
		–	20*	37	–	44		2.7 to 3.6	
		–	18	32	–	38		4.5	
		–	15	25	–	30		6.0	
t_{PHZ}/t_{PLZ}	turn-off time S_n to V_{os}	–	90	–	–	–	ns	1.2	$R_L = 1$ kΩ; $C_L = 50$ pF Figs19, 20 and 21
		–	32	59	–	70		2.0	
		–	19*	36	–	42		2.7 to 3.6	
		–	17	31	–	36		4.5	
		–	14	24	–	28		6.0	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

ADDITIONAL AC CHARACTERISTICS FOR THE 74LV4053

Recommended conditions and typical values

GND = 0 V; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	TYP.	UNIT	V_{CC} (V)	$V_{is(p-p)}$ (V)	CONDITIONS
	sine-wave distortion f = 1 kHz	0.80 0.40	%	3.0 6.0	2.75 5.50	R_L = 10 kΩ; C_L = 50 pF Figs15 and 16
	sine-wave distortion f = 10 kHz	2.40 1.20	%	3.0 6.0	2.75 5.50	R_L = 10 kΩ; C_L = 50 pF Figs15 and 16
	switch 'OFF' signal feed through	−50 −50	dB	3.0 6.0	note 1	R_L = 600 Ω; C_L = 50 pF; f = 1 MHz Figs 11 and 17
	crosstalk between any two switches/multiplexers	−60 −60	dB	3.0 6.0	note 1	R_L = 600 Ω; C_L = 50 pF; f = 1 MHz Fig.13
$V_{(p-p)}$	crosstalk voltage between enable or address input to any switch (peak-to-peak value)	110 220	mV	3.0 6.0		R_L = 600 Ω; C_L = 50 pF; f = 1 MHz (S_n or $\overline{E}$, square wave between V_{CC} and GND, $t_r = t_f$ = 6 ns) Fig.14
f_{max}	minimum frequency response (−3 dB)	180 200	MHz	3.0 6.0	note 2	R_L = 50 Ω; C_L = 50 pF Figs 12, 15 and 14
C_S	maximum switch capacitance	5	pF			

Notes to the AC characteristics

General note

V_{is} is the input voltage at nY_n or nZ terminal, whichever is assigned as an input.

V_{os} is the output voltage at nY_n or nZ terminal, whichever is assigned as an output.

Notes

1. Adjust input voltage V_{is} is 0 dBm level (0 dBm = 1 mW into 600 Ω).
2. Adjust input voltage V_{is} is 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).

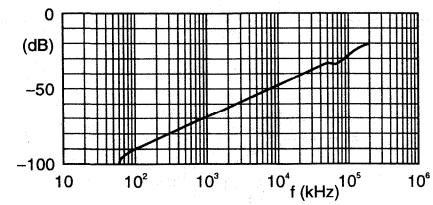


Fig.11 Typical switch 'OFF' signal feed-through as a function of frequency.

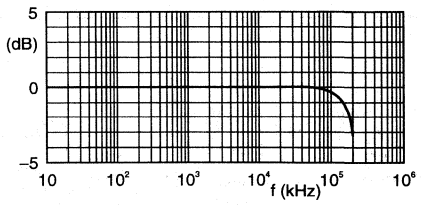


Fig.12 Typical frequency response.

Note to figs 11 and 12

Test conditions: V_{CC} = 3.0 V; GND = 0 V; V_{EE} = −3.0V; R_L = 50 Ω; R_{source} = 1 kΩ.

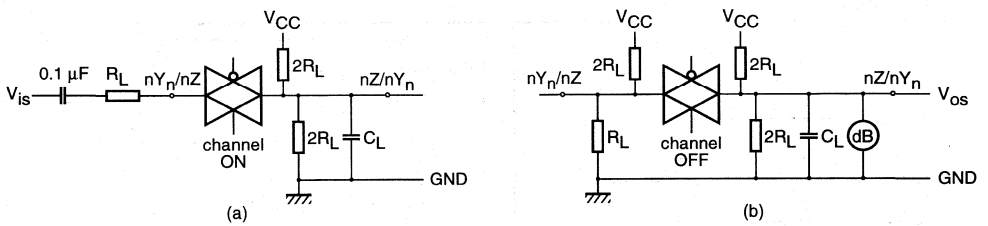


Fig.13 Test circuit for measuring crosstalk between any two switches.
(a) channel ON condition; (b) channel OFF condition.

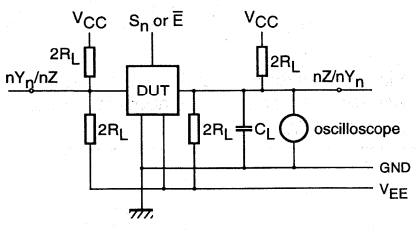
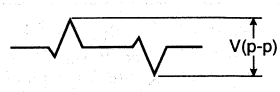


Fig.14 Test circuit for measuring crosstalk between control and any switch.

Note to fig.14

The crosstalk is defined as follows (oscilloscope output):



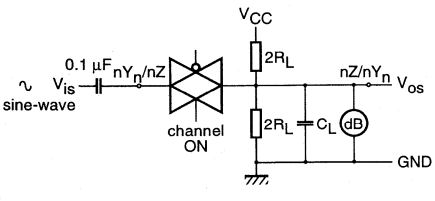


Fig.15 Test circuit for measuring minimum frequency response.

Note to fig.15

Adjust input voltage to obtain 0 dBm at V_{os} when f_{in} = 1 MHz. After set-up frequency of f_{in} is increased to obtain a reading of −3 dB at V_{os}.

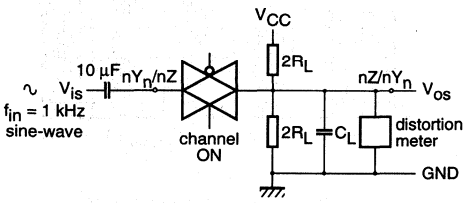


Fig.16 Test circuit for measuring sine-wave distortion.

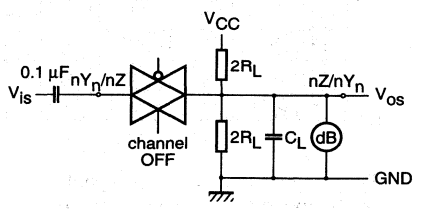


Fig.17 Test circuit for measuring switch 'OFF' signal feed-through.

AC WAVEFORMS

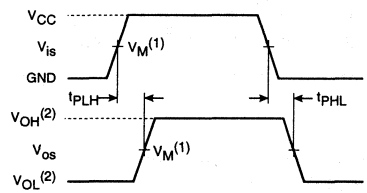


Fig.18 Waveforms showing the input (V_{is}) to output (V_{os}) propagation delays.

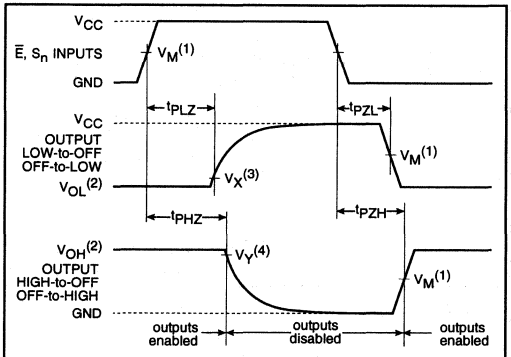


Fig.19 Waveforms showing the turn-on and turn-off times for the inputs (S_n, $\overline{E}$) to the output (V_{os})

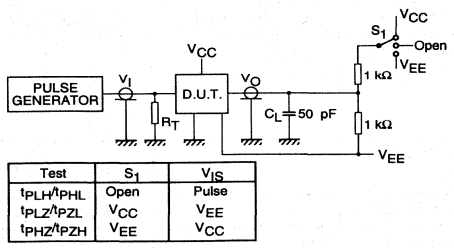
Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

TEST CIRCUIT AND WAVEFORMS



Test	S_1	V_{IS}
t_{PLH}/t_{PHL}	Open	Pulse
t_{PLZ}/t_{PZL}	V_{CC}	V_{EE}
t_{PHZ}/t_{PZH}	V_{EE}	V_{CC}

Fig.20 Test circuit for measuring AC performance.

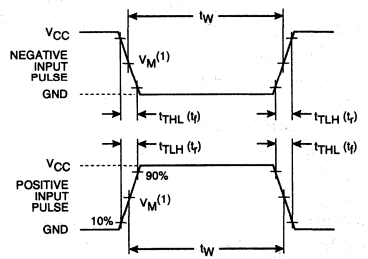


Fig.21 Input (S_n and $\overline{E}$) pulse definitions.

Definitions for figs 20 and 21:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns, when measuring f_{max}, there is no constraint on t_r, t_f with 50% duty factor.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

14-stage binary ripple counter with oscillator | 74LV4060

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **All active components on chip**
- **RC or crystal oscillator configuration**
- **Output capability: standard (except for R_{TC} and C_{TC})**
- **I_{CC} category: MSI**

APPLICATIONS

- **Control counters**
- **Timers**
- **Frequency dividers**
- **Time-delay circuits**

DESCRIPTION

The 74LV4060 is a low-voltage Si-gate CMOS device and is pin and function compatible with the 74HC/HCT4060.

The 74LV4060 is a 14-stage ripple-carry counter/divider and oscillator with three oscillator terminals (RS, R_{TC} and C_{TC}), ten buffered outputs (Q_3 to Q_9 and Q_{11} to Q_{13}) and an overriding asynchronous master reset (MR). The oscillator configuration allows design of either RC or crystal oscillator circuits. The oscillator may be replaced by an external clock signal at input RS. In this case keep the oscillator pins (R_{TC} and C_{TC}) floating.

The counter advances on the negative-going transition of RS. A HIGH level on MR resets the counter (Q_3 to Q_9 and Q_{11} to Q_{13} = LOW), independent of the other input conditions.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH} t_{PHL}	propagation delay RS to Q_3 Q_n to Q_{n+1} MR to Q_n	C_L = 15 pF V_{CC} = 3.3 V	 29 6 16	ns
f_{max}	maximum clock frequency		99	MHz
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1, 2 and 3	40	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}
3. For formula on dynamic power dissipation see following pages.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV4060N	16	DIL	plastic	DIL16/SOT38Z
74LV4060D	16	SO	plastic	SO16/SOT109A
74LV4060DB	16	SSOP	plastic	SSOP16/SOT338
74LV4060PW	16	TSSOP	plastic	TSSOP16/SOT403

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	Q_{11} to Q_{13}	counter outputs
7, 5, 4, 6, 14, 13, 15	Q_3 to Q_9	counter outputs
8	GND	ground (0 V)
9	C_{TC}	external capacitor connection
10	R_{TC}	external resistor connection
11	RS	clock input/oscillator pin
12	MR	master reset
16	V_{CC}	positive supply voltage

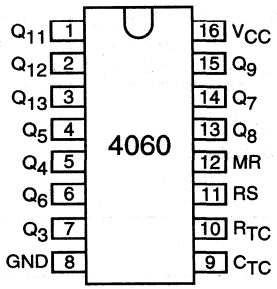


Fig.1 Pin configuration.

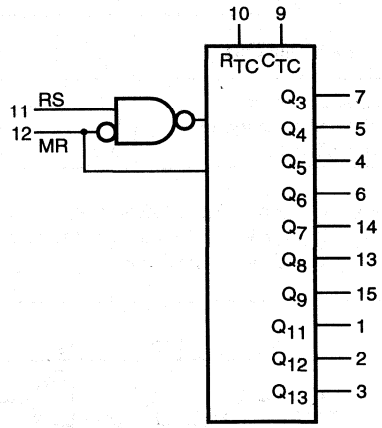
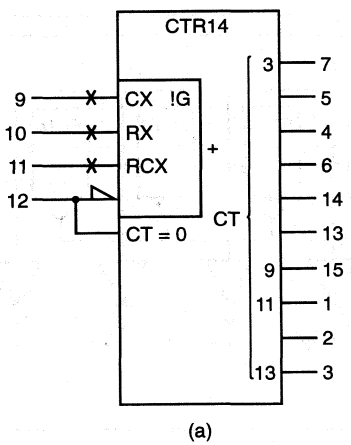


Fig.2 Logic symbol.



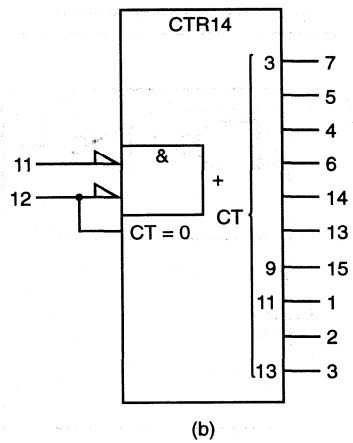


Fig.3 IEC Logic symbol.

DYNAMIC POWER DISSIPATION

GND = 0 V; T_{amb} = 25 °C

PARAMETER	V_{CC} (V)	TYPICAL FORMULA FOR P_D (μW) (note 1)
total dynamic power dissipation when using the on-chip oscillator (P_D)	1.2	$C_{PD} \times f_{osc} \times V_{CC}^2 + \Sigma (C_L \times V_{CC}^2 \times f_o) + 2C_t \times V_{CC}^2 \times f_{osc} + 60 \times V_{CC}$
	2.0	$C_{PD} \times f_{osc} \times V_{CC}^2 + \Sigma (C_L \times V_{CC}^2 \times f_o) + 2C_t \times V_{CC}^2 \times f_{osc} + 1\,750 \times V_{CC}$
	3.0	$C_{PD} \times f_{osc} \times V_{CC}^2 + \Sigma (C_L \times V_{CC}^2 \times f_o) + 2C_t \times V_{CC}^2 \times f_{osc} + 3\,800 \times V_{CC}$

Notes

1. Where: f_o = output frequency in MHz; f_{osc} = oscillator frequency in MHz;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs; C_L = output load capacitance in pF;
   C_t = timing capacitance in pF; V_{CC} = supply voltage in V.

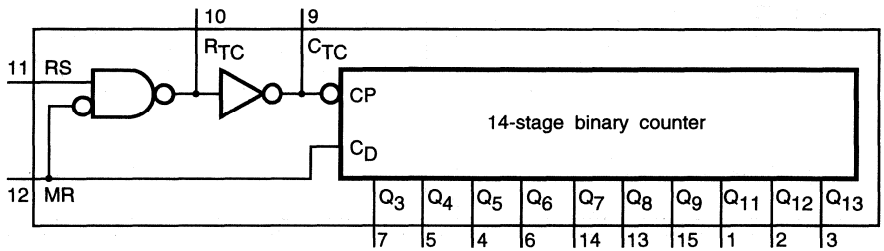


Fig.4 Functional diagram.

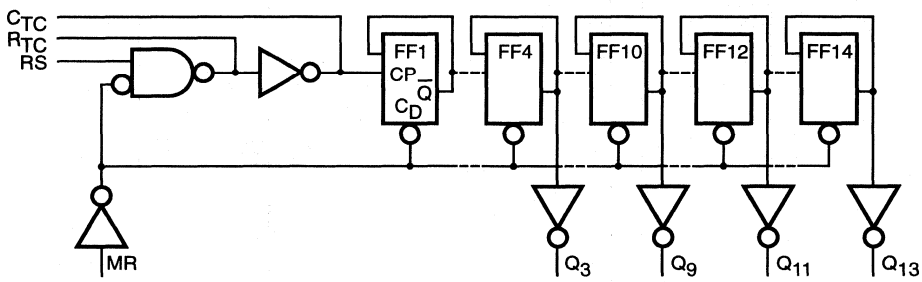


Fig.5 Logic diagram.

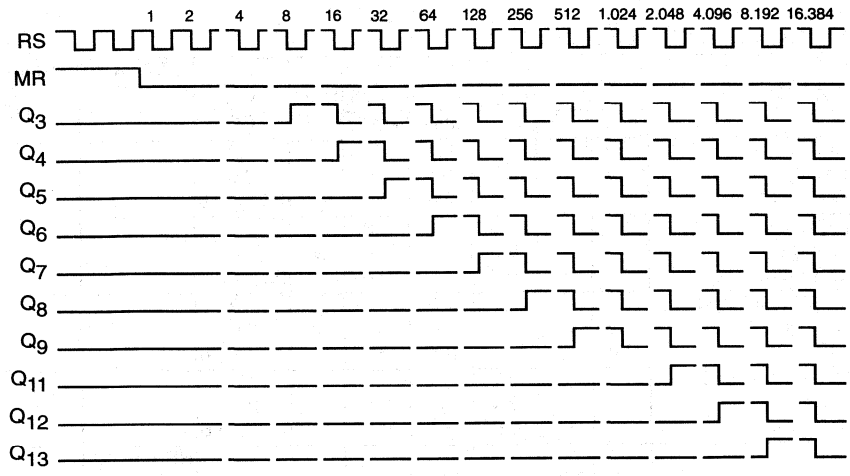


Fig.6 Timing diagram.

DC CHARACTERISTICS FOR THE LV4060

Output capability: standard (except for R_{TC} and C_{TC})

I_{CC} category: MSI

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS		
		−40 to +85			−40 to +125			V_{CC} (V)	V_I	OTHER
		MIN.	TYP.	MAX.	MIN.	MAX.				
V_{IH}	HIGH level input voltage MR input	0.9 1.4 2.0	– – –	– – –	0.9 1.4 2.0	– – –	V	1.2 2.0 2.7 to 3.6		
V_{IL}	LOW level input voltage MR input	– – –	– – –	0.3 0.6 0.8	– – –	0.3 0.6 0.8	V	1.2 2.0 2.7 to 3.6		
V_{IH}	HIGH level input voltage RS input	1.0 1.6 2.4	– – –	– – –	1.0 1.6 2.4	– – –	V	1.2 2.0 2.7 to 3.6		
V_{IL}	LOW level input voltage RS input	– – –	– – –	0.2 0.4 0.5	– – –	0.2 0.4 0.5	V	1.2 2.0 2.7 to 3.6		
V_{OH}	HIGH level output voltage R_{TC} output	2.40	2.82	–	2.20	–	V	3.0	RS = GND and MR = GND	$-I_O$ = 3.4 mA
		2.40	2.82	–	2.20	–	V	3.0	RS = V_{CC} and MR = V_{CC}	$-I_O$ = 0.8 mA
		1.0 1.8 2.8	1.2 2.0 3.0	– – –	1.0 1.8 2.8	– – –	V	1.2 2.0 3.0	RS = GND and MR = GND	$-I_O$ = 100 µA
		1.0 1.8 2.8	1.2 2.0 3.0	– – –	1.0 1.8 2.8	– – –	V	1.2 2.0 3.0	RS = V_{CC} and MR = V_{CC}	$-I_O$ = 100 µA
V_{OH}	HIGH level output voltage C_{TC} output	2.40	2.82	–	2.20	–	V	3.0	RS = V_{IH} and MR = V_{IL}	$-I_O$ = 3.8 mA
V_{OH}	HIGH level output voltage except R_{TC} output	1.0 1.8 2.8	1.2 2.0 3.0	– – –	1.0 1.8 2.8	– – –	V	1.2 2.0 3.0	V_{IH} or V_{IL}	$-I_O$ = 100 µA
V_{OH}	HIGH level output voltage except R_{TC} and C_{TC} outputs	2.40	2.82	–	2.20	–	V	3.0	V_{IH} or V_{IL}	$-I_O$ = 6 mA
V_{OL}	LOW level output voltage R_{TC} output	–	0.25	0.40	–	0.50	V	3.0	RS = V_{CC} and MR = GND	I_O = 3.4 mA
		– – –	0 0 0	0.2 0.2 0.2	– – –	0.2 0.2 0.2	V	1.2 2.0 3.0	RS = V_{CC} and MR = GND	I_O = 100 µA
V_{OL}	LOW level output voltage C_{TC} output	–	0.25	0.40	–	0.50	V	3.0	RS = V_{IH} and MR = V_{IL}	I_O = 3.8 mA

Note: All typical values are measured at T_{amb} = 25 °C.

DC CHARACTERISTICS FOR THE LV4060 *(Continued)*

Output capability: standard (except for R_{TC} and C_{TC})

I_{CC} category: MSI

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS		
		−40 to +85			−40 to +125			V_{CC} (V)	V_I	OTHER
		MIN.	TYP.	MAX.	MIN.	MAX.				
V_{OL}	LOW level output voltage except R_{TC} output	– – –	0 0 0	0.2 0.2 0.2	– – –	0.2 0.2 0.2	V	1.2 2.0 3.0	V_{IH} or V_{IL}	I_O = 100 µA
V_{OL}	LOW level output voltage except R_{TC} and C_{TC} outputs	–	0.25	0.40	–	0.50	V	3.0	V_{IH} or V_{IL}	I_O = 6 mA
$\pm I_I$	input leakage current	–	–	1.0	–	1.0	µA	3.6	V_{CC} or GND	
I_{CC}	quiescent supply current	–	–	20	–	160	µA	3.6	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current per input pin	–	–	500	–	850	µA	2.7 to 3.6	V_{CC} − 0.6 V	I_O = 0

Note: All typical values are measured at T_{amb} = 25 °C.

AC CHARACTERISTICS FOR LV4060

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PHL}	propagation delay RS to Q_3	–	180	–	–	–	ns	1.2	Fig.12
		–	61	116	–	138		2.0	
		–	45	85	–	101		2.7	
		–	34*	68	–	81		3.0 to 3.6	
t_{PHL}/t_{PHL}	propagation delay Q_n to Q_{n+1}	–	40	–	–	–	ns	1.2	Fig.14
		–	14	26	–	31		2.0	
		–	10	19	–	23		2.7	
		–	8*	15	–	18		3.0 to 3.6	
t_{PHL}	propagation delay MR to Q_n	–	100	–	–	–	ns	1.2	Fig.13
		–	34	65	–	77		2.0	
		–	25	48	–	56		2.7	
		–	19*	38	–	45		3.0 to 3.6	
t_W	clock pulse width RS; HIGH or LOW	34	9	–	38	–	ns	2.0	Fig.12
		25	6	–	30	–		2.7	
		20	5*	–	24	–		3.0 to 3.6	
t_W	master reset pulse width MR; HIGH	34	10	–	38	–	ns	2.0	Fig.13
		25	8	–	30	–		2.7	
		20	6*	–	24	–		3.0 to 3.6	
t_{rem}	removal time MR to RS	–	30	–	–	–	ns	1.2	Fig.13
		19	10	–	24	–		2.0	
		14	8	–	18	–		2.7	
		11	6*	–	14	–		3.0 to 3.6	
f_{max}	maximum clock pulse frequency	14	40	–	9	–	MHz	2.0	Fig.12
		19	70	–	12	–		2.7	
		24	90*	–	15	–		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

APPLICATION INFORMATION

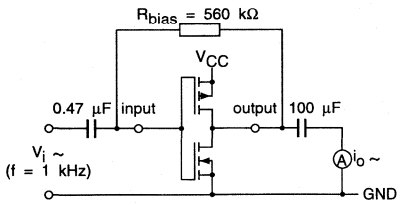


Fig.7 Test set-up for measuring forward transconductance $g_{fs} = di_o/dv_i$ at v_o is constant (see also graph Fig.8); MR = LOW.

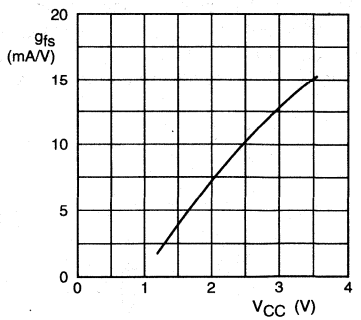


Fig.8 Typical forward transconductance g_{fs} as a function of the supply voltage V_{CC} at T_{amb} = 25 °C.

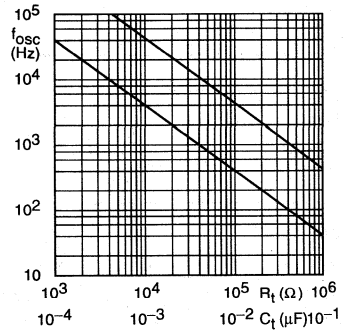


Fig.9 RC oscillator frequency as a function of R_t and C_t at V_{CC} = 1.2 to 3.6 V; T_{amb} = 25 °C. C_t curve at R_t = 100 kΩ; R2 = 200 kΩ. R_t curve at C_t = 1 nF; R2 = 2 x R_t.

RC OSCILLATOR

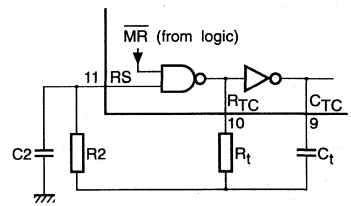


Fig.10 Example of an RC oscillator.
Typical formula for oscillator frequency:

$$F_{osc} = \frac{1}{2.5 \times R_t \times C_t}$$

TIMING COMPONENTS LIMITATIONS

The oscillator frequency is mainly determined by $R_t \cdot C_t$, provided $R2 \approx 2R_t$ and $R2 \cdot C2 \ll R_t \cdot C_t$. The function of R2 is to minimize the influence of the forward voltage across the input protection diodes on the frequency. The stray capacitance C2 should be kept as small as possible. In consideration of accuracy, C_t must be larger than the inherent stray capacitance. R_t must be larger than the 'ON' resistance in series with it, which typically is 280 Ω at V_{CC} = 1.2 V, 130 Ω at V_{CC} = 2.0 V and 100 Ω at V_{CC} = 3.0 V. The recommended values for these components to maintain agreement with the typical oscillation formula are: C_t > 50 pF, up to any practical value, 10 kΩ < R_t < 1 MΩ. In order to avoid start-up problems, $R_t \geq$ 1 kΩ.

TYPICAL CRYSTAL OSCILLATOR

In Fig.11, R2 is the power limiting resistor. For starting and maintaining oscillation a minimum transconductance is necessary, so R2 should not be too large. A practical value for R2 is 2.2 kΩ.

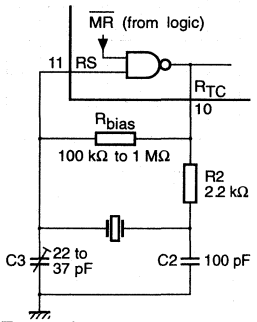


Fig.11 External components connection for a crystal oscillator.

AC WAVEFORMS

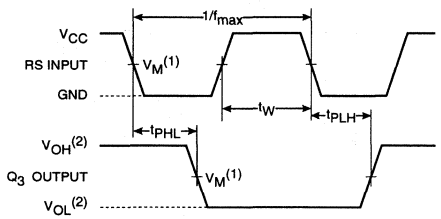


Fig.12 Waveforms showing the clock (RS) to output (Q_3) propagation delays, the clock pulse width and the maximum clock frequency.

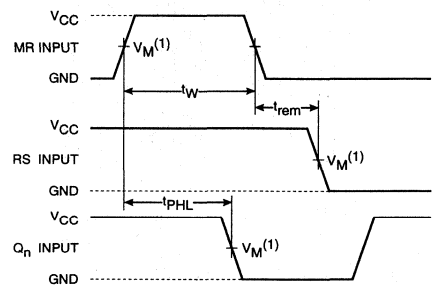


Fig.13 Waveforms showing the master reset (MR) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock (RS) removal time.

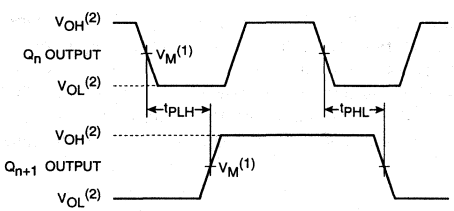


Fig.14 Waveforms showing the output Q_n to output Q_{n+1} propagation delays.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Very low 'ON' resistance: 25 Ω (typ.) at V_{CC} = 4.5 V 35 Ω (typ.) at V_{CC} = 3.0 V 60 Ω (typ.) at V_{CC} = 2.0 V**
- **Output capability: non-standard**
- **I_{CC} category: SSI**

DESCRIPTION

The 74LV4066 is a low-voltage Si-gate CMOS device and is pin and function compatible with the 74HC/HCT4066.

The 74LV4066 has four independent analog switches. Each switch has two input/output terminals (nY, nZ) and an active HIGH enable input (nE). When nE is LOW the corresponding analog switch is turned off.

The 74LV4066 has an on resistance which is dramatically reduced in comparison with 74HC/HCT4066.

FUNCTION TABLE

INPUTS nE	SWITCH
L	off
H	on

H = HIGH voltage level
L = LOW voltage level

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PZH}/t_{PZL}	turn-on time nE to V_{os}	C_L = 15 pF, R_L = 1 kΩ, V_{CC} = 3 V	10	ns
t_{PHZ}/t_{PLZ}	turn-off time nE to V_{os}		13	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per switch	notes 1 and 2	11	pF
C_S	maximum switch capacitances		8	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma \{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; C_S = max. switch capacitance in pF;
   $\Sigma \{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ = sum of the outputs;
   V_{CC} = supply voltage in V.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV4066N	14	DIL	plastic	DIL14/SOT27
74LV4066D	14	SO	plastic	SO14/SOT108A
74LV4066DB	14	SSOP	plastic	SSOP14/SOT337
74LV4066PW	14	TSSOP	plastic	TSSOP14/SOT402

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 8, 11	1Y to 4Y	independent inputs/outputs
2, 3, 9, 10	1Z to 4Z	independent inputs/outputs
13, 5, 6, 12	1E to 4E	enable inputs (active HIGH)
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

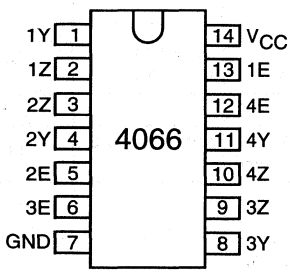


Fig.1 Pin configuration.

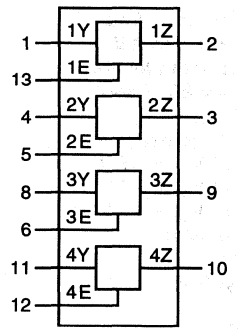


Fig.2 Functional diagram.

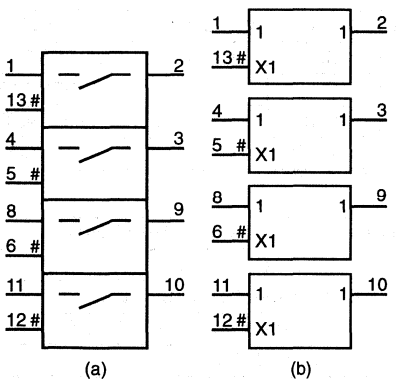


Fig.3 IEC Logic symbol.

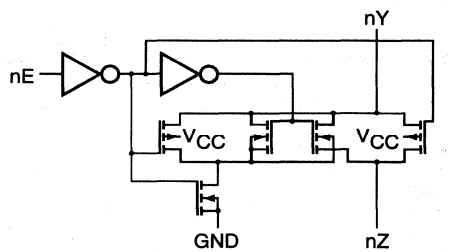


Fig.4 Schematic diagram (one switch).

RECOMMENDED OPERATING CONDITIONS FOR THE LV4066

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	1.0	3.3	6.0	V	see note 1
V_I	input voltage	0	–	V_{CC}	V	
V_O	output voltage	0	–	V_{CC}	V	
T_{amb}	operating ambient temperature range in free air	–40 –40	– –	+85 +125	°C	see DC and AC characteristics per device
t_r, t_f	input rise and fall times except for Schmitt-trigger inputs	– – –	– – –	500 200 100	ns/V	V_{CC} = 1.0 V to 2.0 V V_{CC} = 2.0 V to 2.7 V V_{CC} = 2.7 V to 6.0 V

Notes: 1. The LV-HCMOS is guaranteed to function down to V_{CC} = 1.0 V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2 V to V_{CC} = 6.0 V.

ABSOLUTE MAXIMUM RATINGS FOR THE LV4066

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	–0.5	+7.0	V	
$\pm I_{IK}$	DC input diode current	–	20	mA	$V_I < -0.5$ or $V_I > V_{CC}$ +0.5 V
$\pm I_{SK}$	DC switch diode current	–	20	mA	$V_S < -0.5$ or $V_S > V_{CC}$ +0.5 V
$\pm I_S$	DC switch current	–	25	mA	–0.5 V < V_S < V_{CC} +0.5 V
T_{stg}	storage temperature range	–65	+150	°C	
P_{tot}	power dissipation per package				for temperature range: –40 to +125 °C
	- plastic DIL	–	750	mW	above + 70 °C derate linearly with 12 mW/K
	- plastic mini-pack (SO)	–	500		above + 70 °C derate linearly with 8 mW/K
	- plastic medium-shrink SO (SSOP)	–	500		above + 60 °C derate linearly with 8 mW/K

Notes to the limiting values

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operating of the device at these or any other conditions beyond those under 'recommended operating conditions' is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS FOR 74LV4066

Over recommended operating conditions
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS		
		−40 to +85			−40 to +125			V_{CC} V	V_I	OTHER
		MIN.	TYP.	MAX.	MIN.	MAX.				
V_{IH}	HIGH level input voltage	0.90	–	–	0.90	–	V	1.2	–	
		1.40	–	–	1.40	–		2.0	–	
		2.00	–	–	2.00	–		2.7 to 3.6	–	
		3.15	–	–	3.15	–		4.5	–	
		4.20	–	–	4.20	–		6.0	–	
V_{IL}	LOW level input voltage	–	–	0.30	–	0.30	V	1.2	–	
		–	–	0.60	–	0.60		2.0	–	
		–	–	0.80	–	0.80		2.7 to 3.6	–	
		–	–	1.35	–	1.35		4.5	–	
		–	–	1.80	–	1.80		6.0	–	
$\pm I_I$	input leakage current	–	–	1.0	–	1.0	µA	3.6	V_{CC} or GND	
		–	–	2.0	–	2.0		6.0		
$\pm I_S$	analog switch OFF-state current per channel	–	–	1.0	–	1.0	µA	3.6	V_{IH} or V_{IL}	$\|V_S\| = V_{CC} - GND$ Fig.7
		–	–	2.0	–	2.0		6.0		
$\pm I_S$	analog switch ON-state current	–	–	1.0	–	1.0	µA	3.6	V_{IH} or V_{IL}	$\|V_S\| = V_{CC} - GND$ Fig.8
		–	–	2.0	–	2.0		6.0		
I_{CC}	quiescent supply current	–	–	20	–	40	µA	3.6	V_{CC} or GND	$V_{is} = GND$ or V_{CC}; $V_{os} = V_{CC}$ or GND
		–	–	40	–	80		6.0		
ΔI_{CC}	additional quiescent supply current per input	–	–	500	–	850	µA	2.7 to 3.6	$V_I = V_{CC} - 0.6$ V	

DC CHARACTERISTICS FOR 74LV4066 *(Continued)*

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS			
		−40 to +85			−40 to +125			V_{CC} V	I_S µA	V_{is}	V_I
		MIN.	TYP.	MAX.	MIN.	MAX.					
R_{ON}	ON-resistance (peak)	–	300	–	–	–	Ω	1.2	100	V_{CC} to GND	V_{IH} or V_{IL}
		–	60	125	–	150		2.0	1000		
		–	37	79	–	95		2.7 to 3.6	1000		
		–	25	53	–	63		4.5	1000		
R_{ON}	ON-resistance (rail)	–	75	–	–	–	Ω	1.2	100	GND	V_{IH} or V_{IL}
		–	35	85	–	103		2.0	1000		
		–	24	51	–	62		2.7 to 3.6	1000		
		–	15	36	–	43		4.5	1000		
R_{ON}	ON-resistance (rail)	–	75	–	–	–	Ω	1.2	100	V_{CC}	V_{IH} or V_{IL}
		–	40	107	–	128		2.0	1000		
		–	30	64	–	77		2.7 to 3.6	1000		
		–	22	45	–	54		4.5	1000		
ΔR_{ON}	maximum variation of ON-resistance between any two channels	–	–	–	–	–	Ω	1.2	–	V_{CC} to GND	V_{IH} or V_{IL}
		–	5	–	–	–		2.0	–		
		–	4	–	–	–		2.7 to 3.6	–		
		–	3	–	–	–		4.5	–		

Notes: (1) All typical values are measured at $T_{amb} = 25$ °C.
(2) At supply voltages approaching 1.2 V, the analog switch ON-resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.

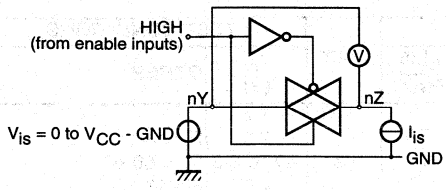


Fig.6 Test circuit for measuring ON-resistance (R_{ON}).

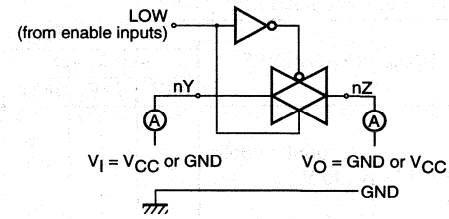


Fig.7 Test circuit for measuring OFF-state current.

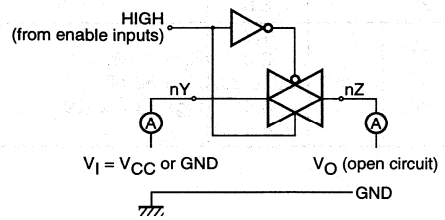


Fig.8 Test circuit for measuring ON-state current.

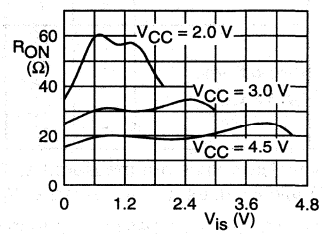


Fig.9 Typical ON-resistance (R_{ON}) as a function of input voltage (V_{is}) for V_{is} = 0 to V_{CC}.

AC CHARACTERISTICS FOR 74LV4066

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	OTHER
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay V_{is} to V_{os}	–	8	–	–	–	ns	1.2	$R_L = \infty$; C_L = 50 pF Fig.17
		–	5	26	–	31		2.0	
		–	3*	15	–	18		2.7 to 3.6	
		–	2	13	–	15		4.5	
		–	2	10	–	12		6.0	
t_{PZH}/t_{PZL}	turn-on time nE to V_{os}	–	40	–	–	–	ns	1.2	R_L = 1 kΩ; C_L = 50 pF Figs 18 and 19
		–	22	43	–	51		2.0	
		–	12*	25	–	30		2.7 to 3.6	
		–	10	21	–	26		4.5	
		–	8	16	–	20		6.0	
t_{PHZ}/t_{PLZ}	turn-off time nE to V_{os}	–	50	–	–	–	ns	1.2	R_L = 1 kΩ; C_L = 50 pF Figs 18 and 19
		–	27	65	–	81		2.0	
		–	15*	38	–	47		2.7 to 3.6	
		–	13	32	–	40		4.5	
		–	12	28	–	34		6.0	

Notes: All typical values are measured at T_{amb} = 25 °C.
* Typical values are measured at V_{CC} = 3.3 V.

ADDITIONAL AC CHARACTERISTICS FOR THE 74LV4066

Recommended conditions and typical values
GND = 0 V; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	TYP.	UNIT	V_{CC} (V)	$V_{is(p-p)}$ (V)	CONDITIONS
	sine-wave distortion f = 1 kHz	0.04	%	3.0	2.75	R_L = 10 kΩ; C_L = 50 pF Fig.15
		0.02		6.0	5.50	
	sine-wave distortion f = 10 kHz	0.12	%	3.0	2.75	R_L = 10 kΩ; C_L = 50 pF Fig.15
		0.06		6.0	5.50	
	switch 'OFF' signal feed through	−50	dB	3.0	note 1	R_L = 600 Ω; C_L = 50 pF; f = 1 MHz Figs 10 and 16
		−50		6.0		
	crosstalk between any two switches	−60	dB	3.0	note 1	R_L = 600 Ω; C_L = 50 pF; f = 1 MHz Fig.12
		−60		6.0		
$V_{(p-p)}$	crosstalk voltage between enable or address input to any switch (peak-to-peak value)	110	mV	3.0		R_L = 600 Ω; C_L = 50 pF; f = 1 MHz (nE, square wave between V_{CC} and GND, $t_r = t_f$ = 6 ns) Fig.13
		220		6.0		
f_{max}	minimum frequency response (−3 dB)	180	MHz	3.0	note 2	R_L = 50 Ω; C_L = 50 pF Figs 11 and 14
		200		6.0		
C_S	maximum switch capacitance	8	pF			

Notes to the AC characteristics

General note

V_{is} is the input voltage at nY or nZ terminal, whichever is assigned as an input.
V_{os} is the output voltage at nY or nZ terminal, whichever is assigned as an output.

Notes

1. Adjust input voltage V_{is} is 0 dBm level (0 dBm = 1 mW into 600 Ω).
2. Adjust input voltage V_{is} is 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).

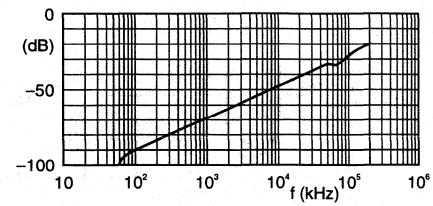


Fig.10 Typical switch 'OFF' signal feed-through as a function of frequency.

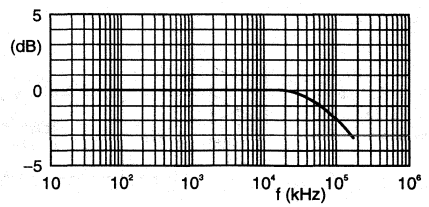


Fig.11 Typical frequency response.

Note to figs 10 and 11

Test conditions: V_{CC} = 3.0 V; GND = 0 V; R_L = 50 Ω; R_{source} = 1 kΩ.

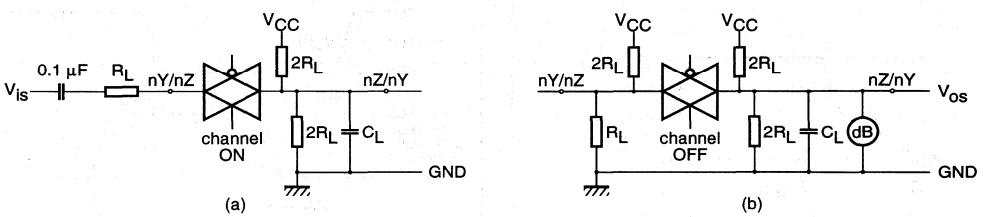


Fig.12 Test circuit for measuring crosstalk between any two switches.
(a) channel ON condition; (b) channel OFF condition.

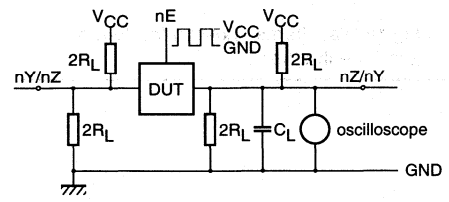
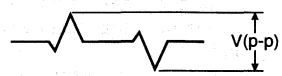


Fig.13 Test circuit for measuring crosstalk between control and any switch.

Note to fig.13

The crosstalk is defined as follows (oscilloscope output):



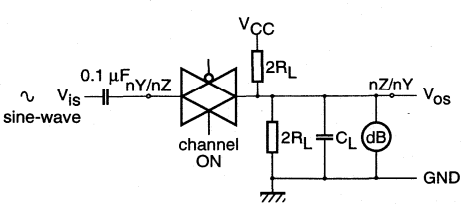


Fig.14 Test circuit for measuring minimum frequency response.

Note to fig.14

Adjust input voltage to obtain 0 dBm at V_{os} when f_{in} = 1 MHz. After set-up, frequency of f_{in} is increased to obtain a reading of −3 dB at V_{os}.

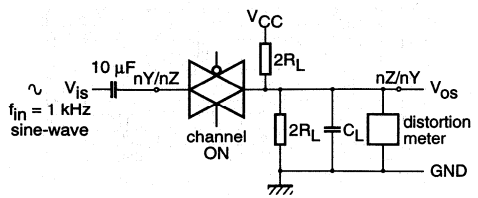


Fig.15 Test circuit for measuring sine-wave distortion.

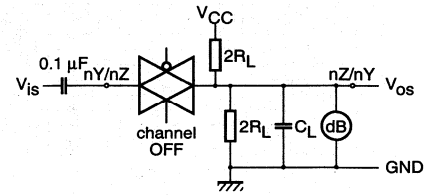


Fig.16 Test circuit for measuring switch 'OFF' signal feed-through.

AC WAVEFORMS

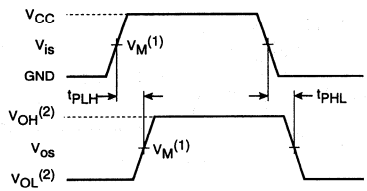


Fig.17 Waveforms showing the input (V_{is}) to output (V_{os}) propagation delays.

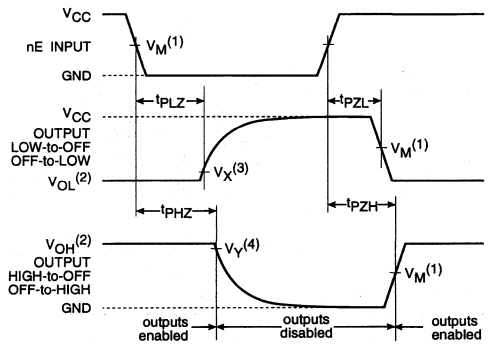


Fig.18 Waveforms showing the turn-on and turn-off times.

Notes:

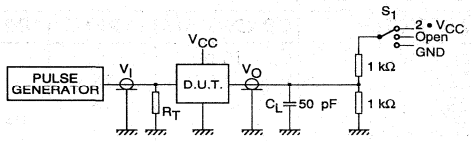
(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

TEST CIRCUIT AND WAVEFORMS



Test	S_1	V_{IS}
t_{PLH}/t_{PHL}	Open	Pulse
t_{PLZ}/t_{PZL}	2 • V_{CC}	GND
t_{PHZ}/t_{PZH}	GND	2 • V_{CC}

Fig.19 Test circuit for measuring AC performance.

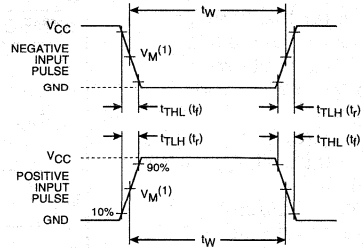


Fig.20 Input pulse definitions.

Definitions for figs 19 and 20:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns, when measuring f_{max}, there is no constraint on t_r, t_f with 50% duty factor.

Notes: (1) V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
V_M = 0.5 · V_{CC} at V_{CC} < 2.7 V

8-stage shift-and-store bus register | 74LV4094

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Output capability: standard**
- **I_{CC} category: MSI**

APPLICATIONS

- **Serial-to-parallel data conversion**
- **Remote control holding register**

DESCRIPTION

The 74LV4094 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT4094.

The 74LV4094 is an 8-stage serial shift register having a storage latch associated with each stage for strobing data from the serial input (D) to the parallel buffered 3-state outputs (QP_0 to QP_7). The parallel outputs may be connected directly to the common bus lines. Data is shifted on the positive-going clock (CP) transitions. The data in each shift register is transferred to the storage register when the strobe input (STR) is HIGH. Data in the storage register appears at the outputs whenever the output enable input (OE) signal is HIGH.
Two serial outputs (QS_1 and QS_2) are available for cascading a number of '4094' devices. Data is available at QS_1 on the positive-going clock edges to allow high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information in available at QS_2 on the next negative going clock edge and is for cascading '4094' devices when the clock rise time is slow.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay CP to QS_1 CP to QS_2 CP to QP_n STR to QP_n	C_L = 15 pF V_{CC} = 3.3 V	 14 13 18 17	ns
f_{MAX}	maximum clock frequency		95	MHz
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per gate	V_{CC} = 3.3 V notes 1 and 2	83	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV4094N	16	DIL	plastic	DIL16/SOT38Z
74LV4094D	16	SO	plastic	SO16/SOT109A
74LV4094DB	16	SSOP	plastic	SSOP16/SOT338
74LV4094PW	16	TSSOP	plastic	TSSOP16/SOT403

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	STR	strobe input
2	D	serial input
3	CP	clock input
4, 5, 6, 7, 14, 13, 12, 11	QP_0 to QP_7	parallel outputs
8	GND	ground (0 V)
9,10	QS_1, QS_2	serial outputs
15	OE	output enable input
16	V_{CC}	positive supply voltage

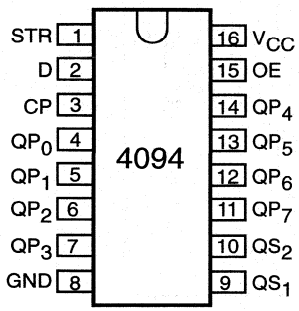


Fig.1 Pin configuration.

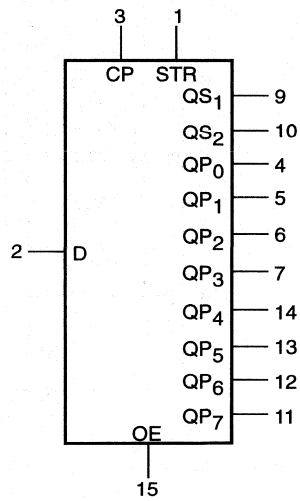


Fig.2 Logic symbol.

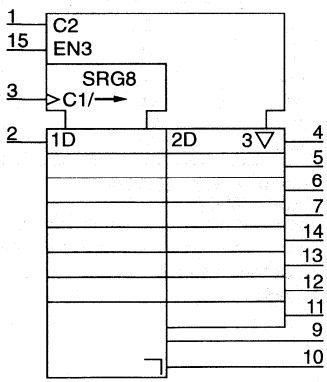


Fig.3 IEC logic symbol.

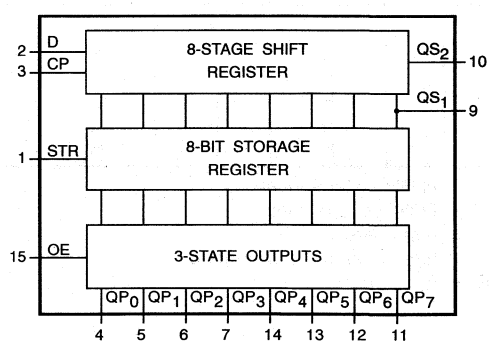


Fig.4 Functional diagram.

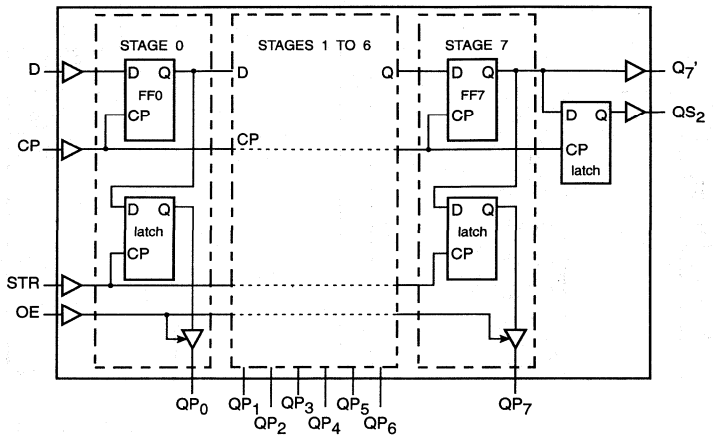


Fig.5 Logic diagram.

FUNCTION TABLE

INPUTS				PARALLEL OUTPUT		SERIAL OUTPUTS	
CP	OE	STR	D	QP_0	QP_n	QS_1	QS_2
↑	L	X	X	Z	Z	Q'_6	NC
↓	L	X	X	Z	Z	NC	QP_7
↑	H	L	X	NC	NC	Q'_6	NC
↑	H	H	L	L	QP_{n-1}	Q'_6	NC
↑	H	H	H	H	QP_{n-1}	Q'_6	NC
↓	H	H	H	NC	NC	NC	QP_7

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state
NC = no change

↑ = LOW-to-HIGH CP transition
↓ = HIGH-to-LOW CP transition
Q'_6 = the information in the seventh register stage is transferred to the 8th register stage and QS_n output at the positive clock edge.

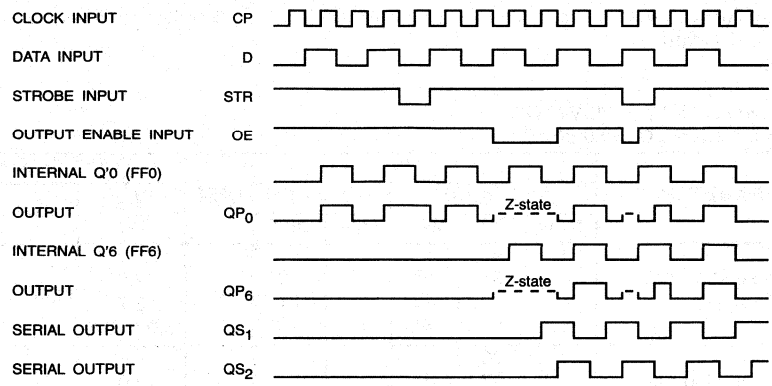


Fig.6 Timing diagram.

DC CHARACTERISTICS FOR 74LV4094

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LV4094

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay CP to QS_1	– – – –	90 31 23 17*	– 58 43 34	– – – –	– 70 51 41	ns	1.2 2.0 2.7 3.0 to 3.6	Fig.7
t_{PHL}/t_{PLH}	propagation delay CP to QS_2	– – – –	80 27 20 14*	– 51 38 30	– – – –	– 61 45 36	ns	1.2 2.0 2.7 3.0 to 3.6	Fig.7
t_{PHL}/t_{PLH}	propagation delay CP to QP_n	– – – –	115 39 29 22*	– 75 55 44	– – – –	– 90 66 53	ns	1.2 2.0 2.7 3.0 to 3.6	Fig.7
t_{PHL}/t_{PLH}	propagation delay STR to QP_n	– – – –	105 36 26 20*	– 68 50 40	– – – –	– 82 60 48	ns	1.2 2.0 2.7 3.0 to 3.6	Fig.8
t_{PZH}/t_{PZL}	3-state output enable time OE to QP_n	– – – –	100 34 25 19*	– 65 48 38	– – – –	– 77 56 45	ns	1.2 2.0 2.7 3.0 to 3.6	Fig.9
t_{PHZ}/t_{PLZ}	3-state output disable time OE to QP_n	– – – –	65 24 18 14*	– 40 32 26	– – – 	– 49 37 30	ns	1.2 2.0 2.7 3.0 to 3.6	Fig.9
t_W	clock pulse width HIGH or LOW	34 25 20	9 6 5*	– – –	41 30 24	– – –	ns	2.0 2.7 3.0 to 3.6	Fig.7
t_W	strobe pulse width; HIGH	34 25 20	9 6 5*	– – –	41 30 24	– – –	ns	2.0 2.7 3.0 to 3.6	Fig.8

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC CHARACTERISTICS FOR 74LV4094 ***(Continued)***

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{su}	set-up time D to CP	– 22 16 13	25 9 6 5*	– – – –	– 26 19 15	– – – –	ns	1.2 2.0 2.7 3.0 to 3.6	Fig.10
t_{su}	set-up time CP to STR	– 43 31 25	50 17 13 10*	– – – –	– 51 38 30	– – – –	ns	1.2 2.0 2.7 3.0 to 3.6	Fig.8
t_h	hold time D to CP	– 5 5 5	−10 −4 −3 −2*	– – – –	– 5 5 5	– – – –	ns	1.2 2.0 2.7 3.0 to 3.6	Fig.10
t_h	hold time CP to STR	– 5 5 5	−25 −9 −6 −5*	– – – –	– 5 5 5	– – – –	ns	1.2 2.0 2.7 3.0 to 3.6	Fig.8
f_{max}	maximum clock pulse frequency	14 19 24	52 70 87*	– – –	12 16 20	– – –	MHz	2.0 2.7 3.0 to 3.6	Fig.7

Notes: All typical values are measured at $T_{amb} = 25$ °C.

* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

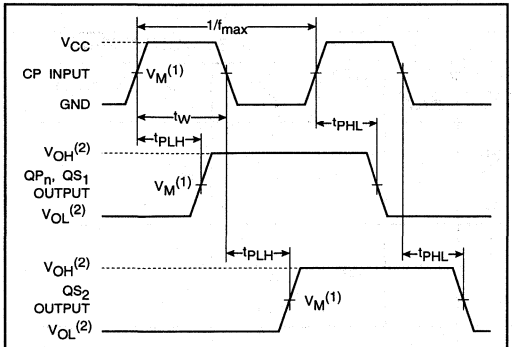


Fig.7 Waveforms showing the clock (CP) to output (QP_n, QS_1, QS_2) propagation delays, the clock pulse width and the maximum clock frequency.

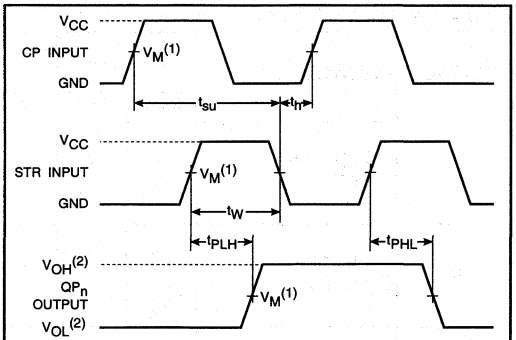


Fig.8 Waveforms showing the strobe (STR) to output (QP_n) propagation delays and the strobe pulse width and the clock set-up and hold times for the strobe input.

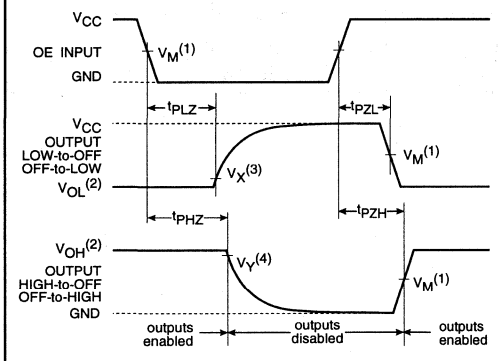


Fig.9 Waveforms showing the 3-state enable and disable times for input OE.

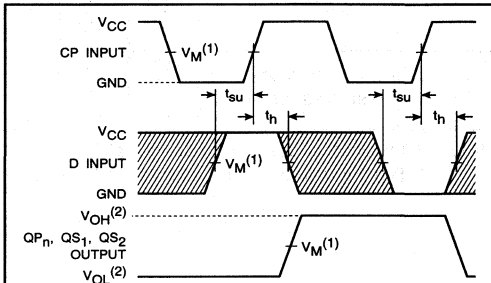
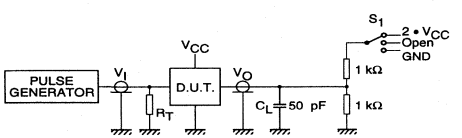


Fig.10 Waveforms showing the data set-up and hold times for the data input (D).

Note to Fig.10
The shaded areas indicate when the input is permitted to change for predictable output performance.



Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.11 Load circuitry for switching times.

Notes:

(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 6.0 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Low typ "ON" resistance: 80 Ω at V_{CC} - V_{EE} = 4.5 V 120 Ω at V_{CC} - V_{EE} = 3.0 V 295 Ω at V_{CC} - V_{EE} = 2.0 V**
- **Logic level translation: to enable 3 V logic to communicate with ± 3 V analog signals**
- **Typical "break before make" built in**
- **Output capability: non-standard**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74LV4316 is a low-voltage CMOS device and is pin and function compatible with the 74HC/HCT4316.

The 74LV4316 has four independent analog switches. Each switch has two input/output terminals (nY, nZ) and an active HIGH select input (nS). When the enable input ($\overline{E}$) is HIGH, all four analog switches are turned off.
Current through a switch will not cause additional V_{CC} current provided the voltage at the terminals of the switch is maintained within the supply voltage range; $V_{CC} > (V_Y, V_Z) > V_{EE}$. Inputs nY and nZ are electrically equivalent terminals.
V_{CC} and GND are the supply voltage pins for the digital control inputs ($\overline{E}$ and nS). The V_{CC} to GND ranges are 1.0 to 6.0V.
The analog inputs/outputs (nY and nZ) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit.
V_{CC} - V_{EE} may not exceed 6.0 V.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PZH}/t_{PZL}	turn "ON" time $\overline{E}$ to V_{os} nS to V_{os}	C_L = 15 pF R_L = 1KΩ V_{CC} = 3.3 V	19	ns
t_{PHZ}/t_{PLZ}	turn "OFF" time $\overline{E}$ to V_{os} nS to V_{os}		20	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per switch	notes 1 and 2	13	pF
C_s	maximum switch capacitance		5	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma ((C_L + C_s) \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; C_s = max. switch capacitance in pF;
   V_{CC} = supply voltage in V;
   $\Sigma ((C_L + C_s) \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV4316N	16	DIL	plastic	DIL16/SOT38Z
74LV4316D	16	SO	plastic	SO16/SOT109A
74LV4316DB	16	SSOP	plastic	SSOP16/SOT338
74LV4316PW	16	TSSOP	plastic	TSSOP16/SOT403

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	1Z to 4Z	independent inputs/outputs
2, 3, 11, 12	1Y to 4Y	independent inputs/outputs
7	$\overline{E}$	enable input (active LOW)
8	GND	ground (0 V)
9	V_{EE}	negative supply voltage
15, 5, 6, 14	1S to 4S	select inputs (active HIGH)
16	V_{CC}	positive supply voltage

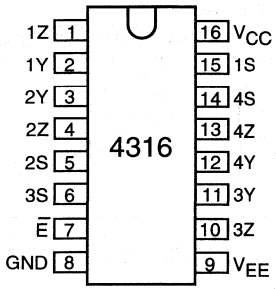


Fig.1 Pin configuration.

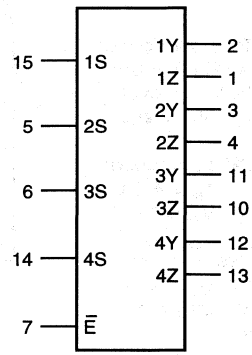


Fig.2 Logic symbol.

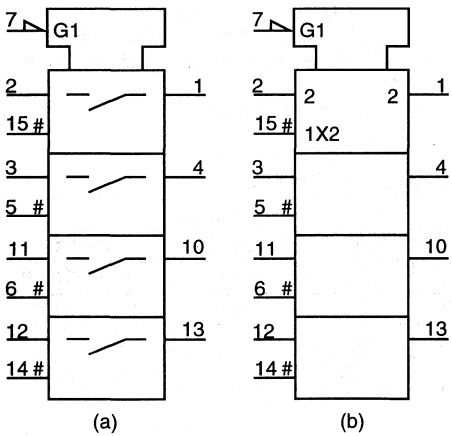


Fig.3 IEC Logic symbol.

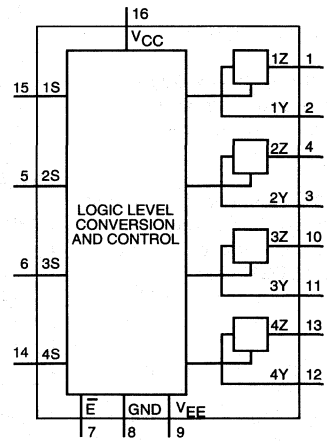


Fig.4 Functional diagram.

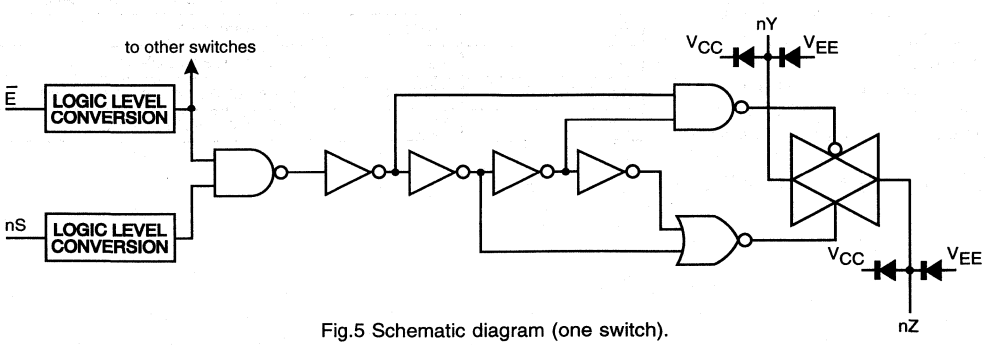


Fig.5 Schematic diagram (one switch).

RECOMMENDED OPERATING CONDITIONS FOR THE LV4316

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	1.0	3.3	6.0	V	see note 1
V_I	input voltage	0	–	V_{CC}	V	
V_O	output voltage	0	–	V_{CC}	V	
T_{amb}	operating ambient temperature range in free air	–40 –40	– –	+85 +125	°C	see DC and AC characteristics per device
t_r, t_f	input rise and fall times except for Schmitt-trigger inputs	– – –	– – –	500 200 100	ns/V	V_{CC} = 1.0 V to 2.0 V V_{CC} = 2.0 V to 2.7 V V_{CC} = 2.7 V to 6.0 V

Notes: 1. The LV-HCMOS is guaranteed to function down to V_{CC} = 1.0 V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2 V to V_{CC} = 6.0 V.

ABSOLUTE MAXIMUM RATINGS FOR THE LV4316

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	–0.5	+7.0	V	
$\pm I_{IK}$	DC input diode current	–	20	mA	$V_I < -0.5$ or $V_I > V_{CC}$ +0.5 V
$\pm I_{SK}$	DC switch diode current	–	20	mA	$V_S < -0.5$ or $V_S > V_{CC}$ +0.5 V
$\pm I_S$	DC switch current	–	25	mA	–0.5 V < V_S < V_{CC} +0.5 V
T_{stg}	storage temperature range	–65	+150	°C	
P_{tot}	power dissipation per package - plastic DIL - plastic mini-pack (SO) - plastic medium-shrink SO (SSOP)	 – – –	 750 500 500	 mW	for temperature range: –40 to +125 °C above + 70 °C derate linearly with 12 mW/K above + 70 °C derate linearly with 8 mW/K above + 60 °C derate linearly with 8 mW/K

Notes to the limiting values

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operating of the device at these or any other conditions beyond those under 'recommended operating conditions' is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS FOR 74LV4316
Over recommended operating conditions
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS		
		−40 to +85			−40 to +125			V_{CC} V	V_I	OTHER
		MIN.	TYP.	MAX.	MIN.	MAX.				
V_{IH}	HIGH level input voltage	0.90	–	–	0.90	–	V	1.2	–	
		1.40	–	–	1.40	–		2.0	–	
		2.00	–	–	2.00	–		2.7 to 3.6	–	
		3.15	–	–	3.15	–		4.5	–	
		4.20	–	–	4.20	–		6.0	–	
V_{IL}	LOW level input voltage	–	–	0.30	–	0.30	V	1.2	–	
		–	–	0.60	–	0.60		2.0	–	
		–	–	0.80	–	0.80		2.7 to 3.6	–	
		–	–	1.35	–	1.35		4.5	–	
		–	–	1.80	–	1.80		6.0	–	
$\pm I_I$	input leakage current	–	–	1.0	–	1.0	µA	3.6	V_{CC} or GND	
		–	–	2.0	–	2.0		6.0		
$\pm I_S$	analog switch OFF-state current per channel	–	–	1.0	–	1.0	µA	3.6	V_{IH} or V_{IL}	$\|V_S\| = V_{CC} - GND$ Fig.7
		–	–	2.0	–	2.0		6.0		
$\pm I_S$	analog switch ON-state current	–	–	1.0	–	1.0	µA	3.6	V_{IH} or V_{IL}	$\|V_S\| = V_{CC} - GND$ Fig.8
		–	–	2.0	–	2.0		6.0		
I_{CC}	quiescent supply current	–	–	20	–	40	µA	3.6	V_{CC} or GND	$V_{is} = GND$ or V_{CC}; $V_{os} = V_{CC}$ or GND
		–	–	40	–	80		6.0		
ΔI_{CC}	additional quiescent supply current per input	–	–	500	–	850	µA	2.7 to 3.6	$V_I = V_{CC} - 0.6$ V	

DC CHARACTERISTICS FOR 74LV4316 ***(Continued)***

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS			
		−40 to +85			−40 to +125			V_{CC} V	I_S µA	V_{is}	V_I
		MIN.	TYP.	MAX.	MIN.	MAX.					
R_{ON}	ON-resistance (peak)	–	–	–	–	–	Ω	1.2	100	V_{CC} to GND	V_{IH} or V_{IL}
		–	295	860	–	990		2.0	1000		
		–	120	300	–	360		2.7 to 3.6	1000		
		–	80	200	–	240		4.5	1000		
R_{ON}	ON-resistance (rail)	–	225	–	–	–	Ω	1.2	100	GND	V_{IH} or V_{IL}
		–	110	240	–	290		2.0	1000		
		–	85	150	–	180		2.7 to 3.6	1000		
		–	40	100	–	120		4.5	1000		
R_{ON}	ON-resistance (rail)	–	250	–	–	–	Ω	1.2	100	V_{CC}	V_{IH} or V_{IL}
		–	120	270	–	325		2.0	1000		
		–	75	170	–	205		2.7 to 3.6	1000		
		–	45	115	–	135		4.5	1000		
ΔR_{ON}	maximum variation of ON-resistance between any two channels	–	–	–	–	–	Ω	1.2	–	V_{CC} to GND	V_{IH} or V_{IL}
		–	5	–	–	–		2.0	–		
		–	4	–	–	–		2.7 to 3.6	–		
		–	3	–	–	–		4.5	–		

Notes: (1) All typical values are measured at T_{amb} = 25 °C.
(2) At supply voltages approaching 1.2 V, the analog switch ON-resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.

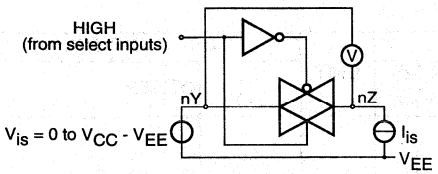


Fig.6 Test circuit for measuring ON-resistance (R_{ON}).

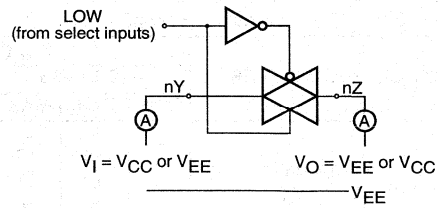


Fig.7 Test circuit for measuring OFF-state current.

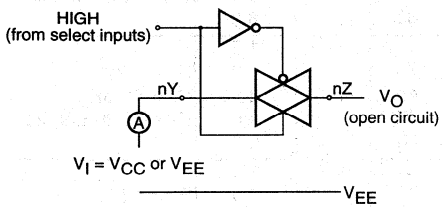


Fig.8 Test circuit for measuring ON-state current.

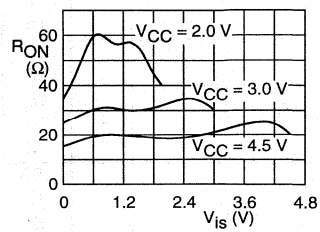


Fig.9 Typical ON-resistance (R_{ON}) as a function of input voltage (V_{is}) for V_{is} = 0 to V_{CC}–V_{EE}.

AC CHARACTERISTICS FOR 74LV4316

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 to +85			−40 to +125			V_{CC} (V)	OTHER
		MIN.	TYP.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay V_{is} to V_{os}	–	30	–	–	–	ns	1.2	$R_L = \infty$; $C_L = 50$ pF Fig.17
		–	10	19	–	24		2.0	
		–	6*	11	–	14		2.7 to 3.6	
		–	5	9	–	12		4.5	
		–	4	7	–	9		6.0	
t_{PZH}/t_{PZL}	turn-on time $\overline{E}$ to V_{os}	–	110	–	–	–	ns	1.2	$R_L = 1$ kΩ; $C_L = 50$ pF Figs19, 20 and 21
		–	37	70	–	85		2.0	
		–	21*	41	–	50		2.7 to 3.6	
		–	19	35	–	43		4.5	
		–	15	27	–	33		6.0	
t_{PZH}/t_{PZL}	turn-on time nS to V_{os}	–	95	–	–	–	ns	1.2	$R_L = 1$ kΩ; $C_L = 50$ pF Figs18, 20 and 21
		–	32	61	–	75		2.0	
		–	18*	36	–	44		2.7 to 3.6	
		–	16	31	–	37		4.5	
		–	12	23	–	29		6.0	
t_{PHZ}/t_{PLZ}	turn-off time $\overline{E}$ to V_{os}	–	105	–	–	–	ns	1.2	$R_L = 1$ kΩ; $C_L = 50$ pF Figs19, 20 and 21
		–	37	68	–	80		2.0	
		–	22*	41	–	48		2.7 to 3.6	
		–	20	35	–	41		4.5	
		–	16	28	–	32		6.0	
t_{PHZ}/t_{PLZ}	turn-off time nS to V_{os}	–	90	–	–	–	ns	1.2	$R_L = 1$ kΩ; $C_L = 50$ pF Figs18, 20 and 21
		–	32	59	–	70		2.0	
		–	19*	36	–	42		2.7 to 3.6	
		–	17	31	–	36		4.5	
		–	14	24	–	28		6.0	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

ADDITIONAL AC CHARACTERISTICS FOR THE 74LV4316

Recommended conditions and typical values

GND = 0 V; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	TYP.	UNIT	V_{CC} (V)	$V_{is(p-p)}$ (V)	CONDITIONS
	sine-wave distortion f = 1 kHz	0.80 0.40	%	3.0 6.0	2.75 5.50	R_L = 10 kΩ; C_L = 50 pF Fig.15
	sine-wave distortion f = 10 kHz	2.40 1.20	%	3.0 6.0	2.75 5.50	R_L = 10 kΩ; C_L = 50 pF Fig.15
	switch 'OFF' signal feed through	−50 −50	dB	3.0 6.0	note 1	R_L = 600 Ω; C_L = 50 pF; f = 1 MHz Figs 10 and 16
	crosstalk between any two switches	−60 −60	dB	3.0 6.0	note 1	R_L = 600 Ω; C_L = 50 pF; f = 1 MHz Fig.12
$V_{(p-p)}$	crosstalk voltage between enable or address input to any switch (peak-to-peak value)	110 220	mV	3.0 6.0		R_L = 600 Ω; C_L = 50 pF; f = 1 MHz (nS or $\overline{E}$, square wave between V_{CC} and GND, $t_r = t_f$ = 6 ns) Fig.13
f_{max}	minimum frequency response (−3 dB)	180 200	MHz	3.0 6.0	note 2	R_L = 50 Ω; C_L = 50 pF Figs 11 and 14
C_S	maximum switch capacitance	5	pF			

Notes to the AC characteristics

General note

V_{is} is the input voltage at nY or nZ terminal, whichever is assigned as an input.

V_{os} is the output voltage at nY or nZ terminal, whichever is assigned as an output.

Notes

1. Adjust input voltage V_{is} is 0 dBm level (0 dBm = 1 mW into 600 Ω).
2. Adjust input voltage V_{is} is 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).

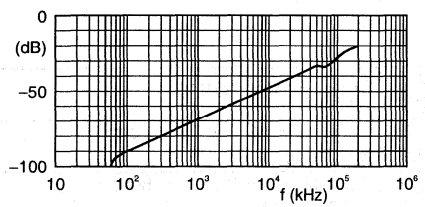


Fig.10 Typical switch 'OFF' signal feed-through as a function of frequency.

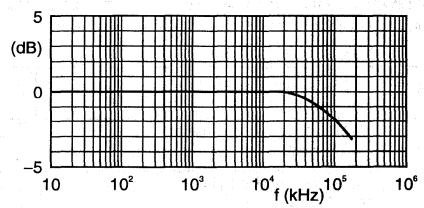


Fig.11 Typical frequency response.

Note to figs 10 and 11

Test conditions: V_{CC} = 3.0 V; GND = 0 V; V_{EE} = −3.0V; R_L = 50 Ω; R_{source} = 1 kΩ.

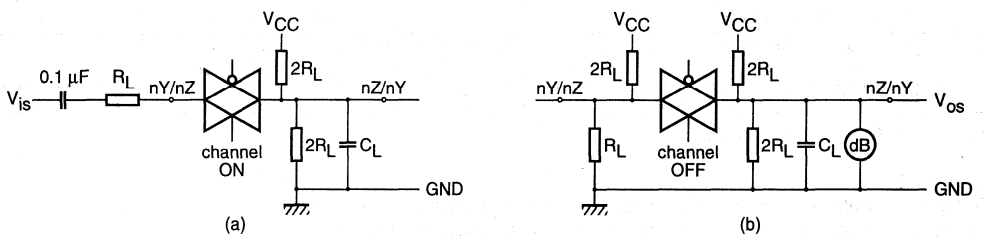


Fig.12 Test circuit for measuring crosstalk between any two switches.
(a) channel ON condition; (b) channel OFF condition.

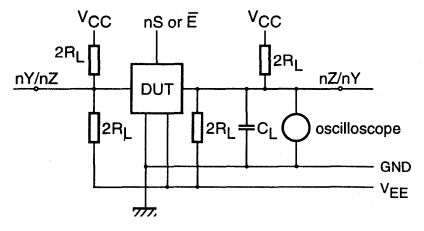
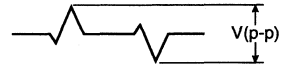


Fig.13 Test circuit for measuring crosstalk between control and any switch.

Note to fig.13

The crosstalk is defined as follows (oscilloscope output):



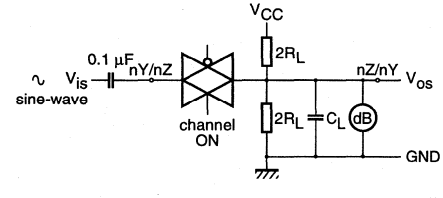


Fig.14 Test circuit for measuring minimum frequency response.

Note to fig.14

Adjust input voltage to obtain 0 dBm at V_{os} when f_{in} = 1 MHz. After set-up frequency of f_{in} is increased to obtain a reading of −3 dB at V_{os}.

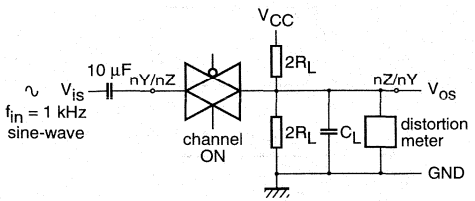


Fig.15 Test circuit for measuring sine-wave distortion.

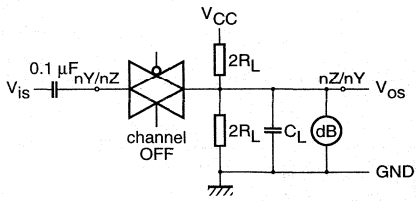


Fig.16 Test circuit for measuring switch 'OFF' signal feed-through.

AC WAVEFORMS

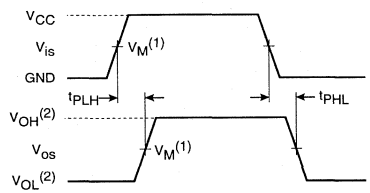


Fig.17 Waveforms showing the input (V_{is}) to output (V_{os}) propagation delays.

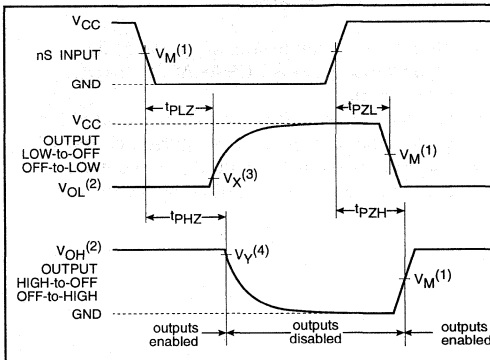


Fig.18 Waveforms showing the turn-on and turn-off times for the select input (nS) to the output (V_{os})

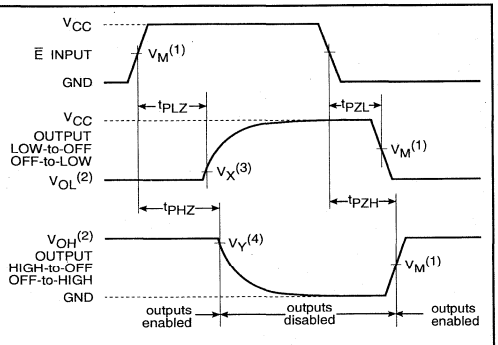


Fig.19 Waveforms showing the turn-on and turn-off times for the enable input ($\overline{E}$) to the output (V_{os}).

Notes:

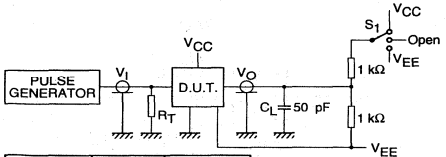
(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

TEST CIRCUIT AND WAVEFORMS



Test	S_1	V_{IS}
t_{PLH}/t_{PHL}	Open	Pulse
t_{PLZ}/t_{PZL}	V_{CC}	V_{EE}
t_{PHZ}/t_{PZH}	V_{EE}	V_{CC}

Fig.20 Test circuit for measuring AC performance.

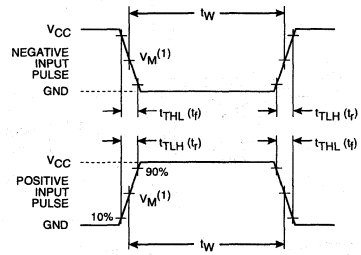


Fig.21 Input (nS and $\overline{E}$) pulse definitions.

Definitions for figs 20 and 21:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = t_f = 6 ns, when measuring f_{max}, there is no constraint on t_r, t_f with 50% duty factor.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

Timer for NiCd and NiMH chargers | 74LV4799

FEATURES

- Wide supply voltage range of 0.9 V to 6 V allows 1 to 4-cell applications
- 10 V allowed on special inputs
- Supports virtually all battery chargers, including switched-mode power supplies
- On-chip timer calculates the actual capacity of the battery by measuring the charge time, discharge time and self-discharge time
- Automatic switch-over to trickle charge after completion of the charge time
- Can be adjusted for use with different types of batteries:
  - Charge time: 4 to 16 hours
  - Discharge time: 15 minutes to 4.7 hours
  - Self-discharge time: 50 to 100 days
- Battery status indication included:
  - $\overline{\text{LED}}$ output for charging/full indication
  - $\overline{\text{MOLLI}}$ output for battery-low indication
- LED mode select allows two different methods of indication
- Automatic power-ON reset
- Low power consumption
- Requires only a few peripheral components
- Very accurate on-chip oscillator
- Scan test facilities included
- I_{CC} category: non-standard.

APPLICATIONS

- Time-controlled NiCd and NiMH low-current chargers
- Domestic appliances such as rechargeable battery shavers, electric toothbrushes etc.
- Portable equipment such as notebook PCs, laptop PCs, camera flash units etc.
- Personal communications like cordless telephones, personal mobile radios, pagers etc.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	DC supply voltage		0.9	–	6.0	V
I_{CC}	operating supply current	V_{CC} = 3.3 V; self-discharge mode; R_S = 100 kΩ; C_1 = 220 nF	–	36	–	µA
Δf	oscillator frequency tolerance	V_{CC} = 1 to 6 V	–	–	7	%

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV4799N	16	DIL	plastic	DIL16/SOT38Z
74LV4799D	16	SO	plastic	SO16/SOT109A
74LV4799DB	16	SSOP	plastic	SSOP16/SOT338
74LV4799PW	16	TSSOP	plastic	TSSOP16/SOT403

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{\text{LED}}$	LED driver output pin (active LOW)
2	EN	enable output (active HIGH)
3	$\overline{\text{EN}}$	enable output (active LOW)
4	V_{in}	external supply input
5	PWRS	power sense input
6	$\overline{\text{MOLLI}}$/SCO	more-or-less-low-indication output (active LOW)/scan test output
7	SEL	LED mode select input
8	GND	ground (0 V)
9	$\overline{\text{DIS}}$	discharge input (active LOW)
10	R_C	external resistor pin 3-state oscillator output (charge)
11	R_D	external resistor pin 3-state oscillator output (discharge)
12	R_S	external resistor pin 3-state oscillator output (self-discharge)
13	I_{OSC}	oscillator input
14	SCAN	scan test mode select input (active HIGH)
15	SCI	scan test input
16	V_{CC}	positive supply voltage

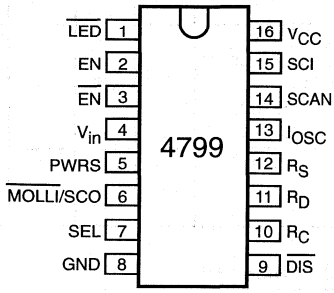


Fig.1 Pin configuration.

GENERAL DESCRIPTION

The 74LV4799 is a low-voltage Si-gate CMOS control IC for battery management. It consists of:

- 17-stage divider
- 10-stage up/down counter
- Control logic
- Integrated precision oscillator (using external timing components)
- Automatic power-ON reset
- Scan test facilities
- Battery charging/full indication output ($\overline{LED}$)
- Battery-low indication output ($\overline{MOLLI}$)
- Open-drain-N outputs for driving the load transistor.

Battery management with the 74LV4799 is based on the principle of time measurement. It measures the charge time, discharge time and self-discharge time by means of a very accurate on-chip oscillator, a divider and an up/down counter.

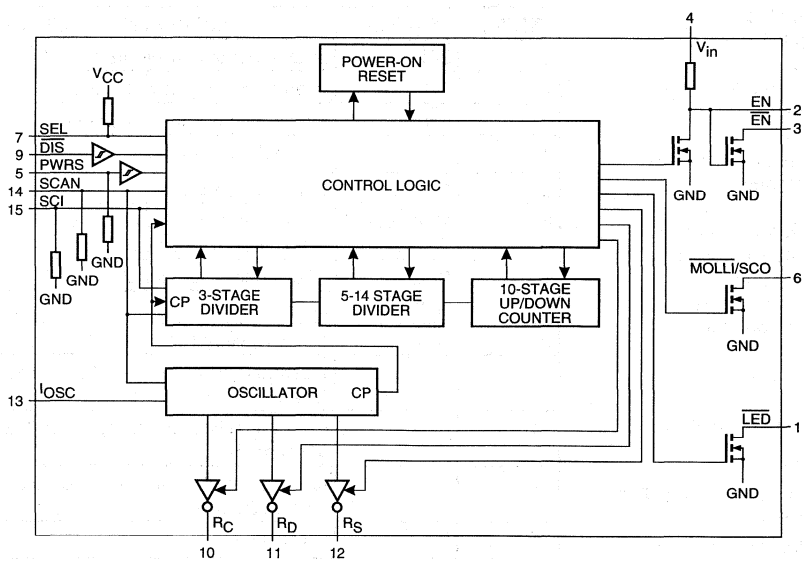


Fig.2 Functional diagram.

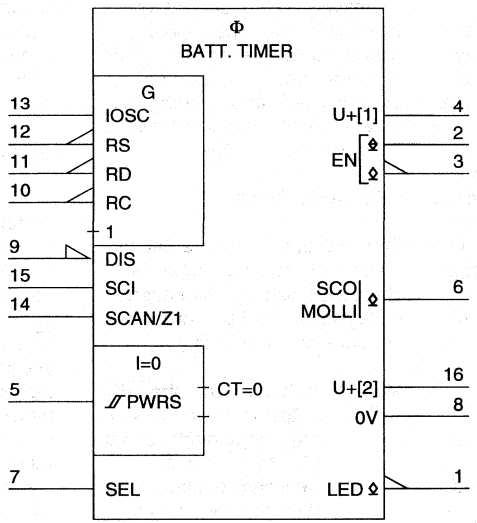


Fig.3 IEC Logic symbol.

Power On Reset.

An automatic Power On Reset initiates the IC when the battery is discharged and power is connected to the circuit. The initial condition is the charge mode in which the counter is reset and counts from zero up to maximum. At start up, the battery therefore always receives a full charge cycle. When a partially charged battery is inserted, it may be over-charged during the first cycle. To guard against this, simply replace the resistor at the R_C pin with an NTC type which is in good thermal contact with the battery. If the temperature of the battery increases, the frequency of the oscillator also increases to quickly reach a counter full indication and switch-over to trickle charge. With a battery that is almost completely discharged, the POR input can also be activated during discharge or self-discharge. The counter will then be reset to zero. This is a correct action while returning to the initial condition.

Power-on sensing.

Because this IC supports virtually all battery chargers, the PWRS input has a broad input frequency spectrum (active HIGH to 100 kHz). A pull-down circuit at the PWRS input allows detection of the open state which corresponds to an inactive charger. A HIGH level on the PWRS input, or an AC signal up to 100 kHz, enables the charge mode.

Start-up with low battery voltage.

Good start-up, even with an un-charged battery, is assured by using the V_{IN} input. The voltage on the V_{IN} input biases the external bipolar transistors at the EN or $\overline{EN}$ output, even if the IC is not yet functioning. After the battery has received sufficient charge, the internal control logic takes over control of the EN and $\overline{EN}$ outputs.

Charge mode.

This mode is selected when PWRS is active (HIGH or pulsed) and the discharge input $\overline{DIS}$ is HIGH. The EN output is HIGH, and the $\overline{EN}$ output is LOW initiating continuous charge of the battery. The counter then counts from the zero state up to the maximum value. The clock frequency is determined by the external capacitor and resistor connected to the R_C output. The counter stops when it reaches its maximum value and the EN and $\overline{EN}$ outputs switch over from the continuous charge to the trickle charge mode.

Trickle charge mode.

At the maximum counter value, it is assumed that the battery is fully charged. The counter stops and remains on this maximum value.

The EN and $\overline{EN}$ outputs switch-over from the continuous charge to the trickle charge mode. In the trickle charge mode, the average charge current is reduced to only compensate the self-discharge of the battery by using dedicated duty cycle control. The control is dedicated because it adjusts the duty cycle in inverse proportion to the load current, resulting in a fixed charger current irrespective of the kind of charger (e.g. 4-hour or 16-hour charger). In the trickle charge mode, the oscillator circuitry alternately generates 4 periods of the R_C-C1 time-constant, and 3 periods of the R_S-C1 time-constant. See Fig.4.

Discharge mode.

The discharge input ($\overline{DIS}$) is used to detect the discharge of the battery. If $\overline{DIS}$ is LOW, the counter counts down. The clock frequency is determined by the external capacitor and resistor at the R_D output. If PWRS is inactive (LOW or open), the EN output is LOW, and the $\overline{EN}$ output is in the high impedance OFF-state (no charge of the battery). This is called the discharge mode. If PWRS is active, the circuit is in the charge/discharge mode.

Charge/Discharge mode.

If $\overline{DIS}$ is LOW and PWRS is active (HIGH or pulsed), the circuit is in the charge/discharge mode. The counter counts down. The clock frequency is determined by the external capacitor and resistor tied at the R_D output. The EN output is HIGH, and the $\overline{EN}$ output is LOW initiating continuous charge of the battery. The battery is therefore charged and discharged at the same instant, thereby maintaining a better load condition of the battery.

Self-discharge mode.

If $\overline{DIS}$ is HIGH and PWRS is inactive (LOW or open), the battery is being neither charged nor discharged. The circuit is in the self-discharge mode. This mode represents the battery leakage (self-discharge). The counter counts down. The clock frequency is determined by the external capacitor and resistor at the R_S output. When the counter reaches the zero state, it stops.

LED mode select.

The $\overline{LED}$ output drives a battery status LED which indicates the charge/full status of the battery. For optimum flexibility, two modes of operation are built-in.

Mode 1: If SEL is LOW, the $\overline{LED}$ output is active LOW in the charge mode, and the LED blinks with a frequency of about 1 Hz during trickle charge.

Mode 2: If SEL is HIGH or open, the $\overline{LED}$ output blinks with a frequency of about 0.25 Hz in the charge mode, and is active LOW during trickle charge. In the discharge or self-discharge mode, the $\overline{LED}$ output is open except when PWRS is active (HIGH or pulsed). Then, the battery is charging and discharging simultaneously. Although the discharge mode is dominant, the $\overline{LED}$ output is active when PWRS is also active.

Note: The blink frequency depends on the oscillator frequency. (See application information)

Low indication.

As part of the user interface, the $\overline{MOLLI}$ output shows when the battery needs to be charged. $\overline{MOLLI}$ stands for More Or Less Low Indication (active LOW). The function is as follows: In the discharge mode, ($\overline{DIS}$ is active LOW), the counter counts down and, when it reaches the zero state, it stops. If $\overline{DIS}$ is switched HIGH, the $\overline{MOLLI}$ output gives an output signal of four periods of about one second, with a 50% duty cycle. This can be used to activate a buzzer. The $\overline{MOLLI}$ output signal of four periods will be interrupted as soon as PWRS is activated.

Alarm indication

If an almost completely discharged battery is connected to the charger, it may not be noticed by the user if the load switch is still on. To prevent damaging the battery, an alarm signal on the $\overline{LED}$ output will alert the user to switch off the load. The alarm signal is easily recognised, because the $\overline{LED}$ output will blink at a higher frequency than normal (about 5 Hz instead of 1 Hz). This alarm indication is only active if the SEL input is HIGH or open. If the SEL input is LOW, no alarm indication is present, because in many applications simultaneous charging and discharging is quite acceptable (See charge/discharge mode).

Scan test mode.

If the SCAN input (pin 14) is made active HIGH, the circuit is in the test mode. The tester clock is connected to the I_{OSC} pin (pin 13). In the scan mode, the on-chip oscillator is bypassed to allow rapid testing of the divider/counter. The scan test patterns are available on request. The scan test data is entered serially through the SCI input (pin 15). The scan out data is present on the $\overline{MOLLI}$/SCO output (pin 6), which then acts as a scan output.

Remaining energy indication.

The scan test facility can be used as a remaining energy indication because the value of the counter can be read out at the scan output ($\overline{MOLLI}$/SCO). This is done by briefly interrupting the normal mode of operation, putting the circuit in the scan mode, and reading out the counter value. The

circuit then reverts to the normal mode. This only works correctly with the $\overline{\text{MOLLI}}$/SCO output and SCI input linked (round coupled loop) and with exactly 49 clock pulses applied to the I_{OSC} input.

The serial scan-out data is available on the $\overline{\text{MOLLI}}$/SCO output. The value of the counter can be decoded by reading the correct bits. Details are given in the Chapter "Application information".

Output drivers EN and $\overline{\text{EN}}$.

In one-cell battery (low-voltage) applications, the drive from the ENABLE output ($\overline{\text{EN}}$) is insufficient to provide the base current directly for the external bipolar PNP regulator transistor. The inverse signal has therefore been made available at the ENABLE output (EN) to drive an extra bipolar NPN transistor that can provide the base current for the bipolar PNP regulator transistor as shown in Fig.5.

FUNCTION TABLE 1

OPERATING MODES	INPUTS			OUTPUTS					DIVIDER/COUNTER	
	PWRS	V_{IN}	$\overline{\text{DIS}}$	EN	$\overline{\text{EN}}$	R_C	R_D	R_S	MODE	VALUE
charge	H or ⎍⎍	H	H	H	L	⎍⎍	Z	Z	count up 22 sections	< max
trickle charge	H or ⎍⎍	H	H	⎍⎍	⎓⎓	⎍⎍	Z	⎍⎍	stop	max
charge/discharge	H or ⎍⎍	H	L	H	L	Z	⎍⎍	Z	count down 18 sections	≥ min
discharge	L or open	X	L	L	Z	Z	⎍⎍	Z	count down 18 sections	≥ min
self-discharge	L or open	X	H	L	Z	Z	Z	⎍⎍	count down 27 sections	≥ min

FUNCTION TABLE 2

STATUS INDICATION	INPUTS			OUTPUTS		COUNTER	
	PWRS	$\overline{\text{DIS}}$	SEL[1]	$\overline{\text{LED}}$	$\overline{\text{MOLLI}}$	MODE	VALUE
charge	H or ⎍⎍ H or ⎍⎍	H H	L H or open	L ⎓⎓	Z Z	count up count up	< max < max
charge/discharge	H or ⎍⎍	L	L	L	Z	count down	≥ min
trickle charge	H or ⎍⎍ H or	H H	L H or open	⎓⎓ L	Z Z	stop stop	max max
discharge	L or open	L	X	Z	Z	count down	> min
self-discharge	L or open	H	X	Z	Z	count down	> min
low	L or open	↑	X	Z	⎓	stop	min
low	↑	↑	X	Z	Z[2]	count up	≥ min
alarm	H or	L	H or open	⎓⎓	Z	count down	≥ min

Notes

1. Don't change SEL during operation.
2. The $\overline{\text{MOLLI}}$ function will be interrupted as soon as PWRS is activated.

H = HIGH voltage level
L = LOW voltage level
Z = high impedance OFF-state
X = don't care
⎍⎍ = pulsed (H/L)
⎓⎓ = pulsed (Z/L)
⎓ = 4 periods of about one second (Z/L)
↑ = LOW-to-HIGH level transition

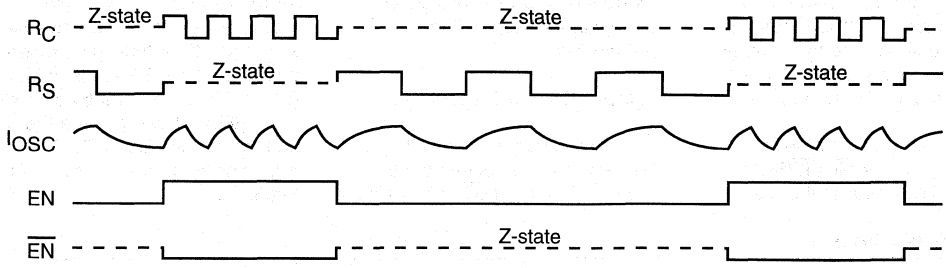


Fig.4 Operation in the trickle charge mode. The duration of the R_C cycle determines the duty cycle of the enable outputs (EN and $\overline{EN}$), allowing a dedicated control. The average trickle charge current will compensate for the self-discharge, independent of the charge current.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	0.9	1.2	6.0	V	
V_I	input voltage pins 4, 5 and 9	0	–	10	V	see note 1
	input voltage pins 7, 13, 14 and 15	0	–	V_{CC}	V	
V_O	output voltage pins 10, 11 and 12	0	–	V_{CC}	V	
	output voltage pins 1, 2, 3 and 6	0	–	10	V	
T_{amb}	operating ambient temperature range in free air	0	–	+70	°C	
t_r, t_f	input rise and fall times pin 5	–	–	10	ms	
	input rise and fall times pins 7, 14 and 15	–	–	4000	ns	V_{CC} = 1.0 V; V_I = 1.0 V
		–	–	1000	ns	V_{CC} = 2.0 V; V_I = 2.0 V
		–	–	500	ns	V_{CC} = 3.0 V; V_I = 4.5 V
		–	–	400	ns	V_{CC} = 6.0 V; V_I = 6.0 V
	input rise and fall times pin 9	–	–	2	µs	

Note

1. Single sided input protection applied on pins 4, 5 and 9

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7.0	V	
I_{IK}	DC input diode current pins 4, 5 and 9	–	±20	mA	$V_I < -0.5$ or $V_I > 12$ V
	DC input diode current pins 7, 13, 14 and 15	–	±20	mA	$V_I < -0.5$ or $V_I > V_{CC}$ +0.5 V
I_{IK}	NON repetitive peak DC input diode current pin 9	–	10	mA	$V_I > 10$ V and $t < 10$ µs; see note 1
V_I	DC input voltage range pins 4,5 and 9	−0.5	+12	V	
	DC input voltage range pins 7, 13, 14 and 15	−0.5	V_{CC} + 0.5	V	
I_{OK}	DC output diode current pins 1, 2, 3 and 6	–	−20	mA	$V_O < -0.5$ V
I_O	DC output sink current pins 1, 2, 3 and 6	–	−25	mA	$V_O > 0$ V
I_{OK}	DC output diode current pins 10, 11 and 12	–	±20	mA	$V_O < -0.5$ V or $V_O > V_{CC}$ + 0.5 V
I_O	DC output sink or source current pins 10, 11 and 12	–	±25	mA	-0.5 V $< V_O < V_{CC}$ + 0.5 V
I_{GND}, I_{CC}	DC GND or V_{CC} current	–	±50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for temperature range: −40 to +125 °C
	plastic DIL	–	750	mW	above + 70 °C derate linearly with 12 mW/K
	plastic mini-pack (SO)	–	500	mW	above + 70 °C derate linearly with 8 mW/K

Notes

1. In applications where a motor is present, the input voltage may exceed the maximum V_I level of 10 V at the DIS input for a very short period when the motor is switched off.
2. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those under 'recommended operating conditions' is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS

Over recommended operating conditions.
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS		
		+25			0 to +70			V_{CC} (V)	V_I	OTHER
		MIN.	TYP.	MAX.	MIN.	MAX.				
V_{IH}	HIGH level input voltage	0.8	0.5	–	0.8	–	V	1.0		
		3.6	2.4	–	3.6	–	V	4.5		
		4.8	3.2	–	4.8	–	V	6.0		
V_{IL}	LOW level input voltage	–	0.5	0.2	–	0.2	V	1.0		
		–	2.1	0.9	–	0.9	V	4.5		
		–	2.8	1.2	–	1.2	V	6.0		
V_{OH}	HIGH level output voltage; R_C, R_D outputs	0.90	0.96	–	0.89	–	V	1.0	V_{IH} or V_{IL}	I_O = –190 µA
		5.73	5.84	–	5.66	–	V	6.0		I_O = –6.1 mA
V_{OH}	HIGH level output voltage; R_S output	0.90	0.96	–	0.89	–	V	1.0	V_{IH} or V_{IL}	I_O = –24 µA
		5.73	5.84	–	5.66	–	V	6.0		I_O = –760 µA
V_{OL}	LOW level output voltage; R_C, R_D outputs	–	0.04	0.10	–	0.11	V	1.0	V_{IH} or V_{IL}	I_O = 190 µA
		–	0.16	0.26	–	0.33	V	6.0		I_O = 6.1 mA
V_{OL}	LOW level output voltage; R_S output	–	0.04	0.10	–	0.11	V	1.0	V_{IH} or V_{IL}	I_O = 24 µA
		–	0.16	0.26	–	0.33	V	6.0		I_O = 760 µA
V_{OL}	LOW level output voltage; $\overline{MOLLI}$, $\overline{LED}$ outputs	–	0.04	0.10	–	0.11	V	1.0	V_{IH} or V_{IL}	I_O = 220 µA
		–	0.17	0.26	–	0.33	V	6.0		I_O = 7.4 mA
V_{OL}	LOW level output voltage; EN output	–	0.04	0.10	–	0.11	V	1.0	V_{IH} or V_{IL}	I_O = 360 µA; pin 4 open
		–	0.17	0.26	–	0.33	V	6.0		I_O = 13.0 mA; pin 4 open
V_{OL}	LOW level output voltage; EN output	–	0.12	0.35	–	0.40	V V	1.3	V_{IH} or V_{IL}	pin 4 = 10 V; see note 1
V_{OL}	LOW level output voltage; $\overline{EN}$ output	–	0.04	0.10	–	0.11	V	1.0	V_{IH} or V_{IL}	I_O = 140 µA; pin 4 HIGH
		–	0.17	0.26	–	0.33	V	6.0		I_O = 5.0 mA; pin 4 HIGH
V_{CC}	POR level	0.25	–	0.65	–	–	V			
	active inactive	–	–	0.9	–	–	V			

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS		
		+25			0 to +70			V_{CC} (V)	V_I	OTHER
		MIN.	TYP.	MAX.	MIN.	MAX.				
I_{CC}	quiescent supply current	–	34	50	–	400	µA	6.0	V_{CC} or GND	pins 5, 14 and 15 at GND; pins 7 and 9 at V_{CC}; see note 2
I_I	input leakage current pins 4 and 9	–	–	500	–	–	nA	1.0	10 V	
I_I	input leakage current pins 14 and 15	–	–	100	–	–	nA	6.0	V_{CC} or GND	
I_I	pull-up current pin 7	–0.5 –0.5	–2.4 –2.4	–10 –10	– –	– –	µA µA	1.0 6.0	GND	
I_I	pull-down current pin 5	0.5 0.5	2.4 2.4	10 10	– –	– –	µA µA	1.0 6.0	V_{CC}	
I_{OZH}	OFF-state current pins 1, 3 and 6	–	–	500	–	–	nA	6.0	V_{IH} or V_{IL}	V_o = 10V
I_{OZH}	OFF-state current pin 2	–	–	100	–	–	nA	6.0		V_o = 6V V_{in} = open
I_{OZH}	OFF-state current pin 3	–	–	100	–	–	nA	6.0	V_{IH} or V_{IL}	V_o = 6V
I_{OZ}	OFF-state current pins 10, 11 and 12	–	–	±100	–	–	nA	6.0	V_{IH} or V_{IL}	V_o = V_{CC} or GND

Notes to the DC characteristics

1. This item guarantees that an external bipolar NPN-transistor can be switched off by the EN output.
2. Oscillator disabled. This can be done by I_{OSC} = HIGH or LOW.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		+25			0 to +70			V_{CC} (V)	OTHER
		MIN.	TYP.	MAX.	MIN.	MAX.			
Δf	oscillator frequency spread	−11 −9	−4 −2	+3 +5	– –	– –	% %	1.0 6.0	any resistor or capacitor according to the application information; see note 1
δ_{LED}	duty factor at pin 1	– –	50 50	– –	– –	– –	% %	1.0 6.0	see note 2
δ_{MOLLI}	duty factor at pin 6	– –	50 50	– –	– –	– –	% %	1.0 6.0	see note 3
t_{deb}	debounce suppression at pin 9	– –	67 65	– –	– –	– –	ms ms	1.0 6.0	
$f_{i(max)}$	maximum frequency at power sense input	100 100	– –	– –	– –	– –	kHz kHz	1.0 6.0	
$f_{i(min)}$	minimum frequency at power sense input	– –	– –	50 50	– –	– –	Hz Hz	1.0 6.0	

Notes

1. The oscillator frequency can be calculated by: $f = \frac{0.36}{R \times C1}$
2. During blinking.
3. An output signal of four periods will appear in case of discharged batteries and $\overline{DIS}$ is switched HIGH.

APPLICATION INFORMATION

Oscillator.

The frequency will be determined by the external components R_C, R_D, R_S and C1. The frequencies can be calculated by the following expressions: $f_C = \frac{0.36}{R_C \times C1}$; $f_D = \frac{0.36}{R_D \times C1}$; $f_S = \frac{0.36}{R_S \times C1}$.

R_C and C1 determine the charge time.
R_D and C1 determine the discharge time.
R_S and C1 determine the self-discharge time.

The charge, discharge and self-discharge times can be calculated as follows:

Charge time = $\frac{2^{22}}{f_C}$; Discharge time = $\frac{2^{18}}{f_D}$; Self-discharge time = $\frac{2^{27}}{f_S}$.

In the trickle charge mode the average charge current will be reduced by a factor: $\frac{1}{1 + \frac{3 \times R_S}{4 \times R_C}}$.

External components range

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS		
		+25				V_{CC} (V)	V_I	OTHER
		MIN.	TYP.	MAX.				
R_C/R_D	resistor range	5.360	–	100	kΩ	1.0	–	C1 = 0.22 µF
		1.150	–	100	kΩ	2.0	–	
		0.562	–	100	kΩ	4.5	–	
		0.511	–	100	kΩ	6.0	–	
R_S	resistor range	42.20	–	825	kΩ	1.0	–	C1 = 0.22 µF
		9.09	–	825	kΩ	2.0	–	
		4.22	–	825	kΩ	4.5	–	
		3.32	–	825	kΩ	6.0	–	
C1	capacitor range	–	–	no limit	pF	1.0	–	
		–	–	no limit	pF	2.0	–	
		–	–	no limit	pF	4.5	–	
		–	–	no limit	pF	6.0	–	

Charge-discharge times

PARAMETER	TIME RANGE	CONDITIONS
Charge time	4 hours to 16 hours	Components ranges are within the values given in Section "External components range"
Discharge time	15 minutes to 4.7 hours	
Self-discharge time	50 days to 100 days	

LED frequency

The frequency of the $\overline{LED}$ output (pin 1) is determined by the oscillator frequency.
Three modes of operation, each with its own frequency, are possible.

Mode	SEL	$\overline{LED}$ frequency
charge	H or open	$\frac{f_C}{256}$
trickle charge	L	$\frac{1}{\frac{8}{f_C} + \frac{6}{f_S}}$
alarm	H	$\frac{f_D}{32}$

$\overline{\text{MOLLI}}$ pulse duration

The $\overline{\text{MOLLI}}$ output gives an output signal of four periods with a 50% duty cycle.
The duration of one period is determined by: $16/f_s$

Timing accuracy.

The timing accuracy depends on the accuracy of the on-chip oscillator and on the external R and C components. The inaccuracy of the on-chip oscillator is specified as maximum ±7%. In most cases the actual inaccuracy will be significantly lower. This depends on the supply voltage as well as the value of the external components.

Influence of Resistor value.

Low resistor values cause some spread because the RC combination is biased by a 3-state push-pull output. The spread of the R_{on} of the push-pull stage will contribute to the frequency spread. When high-value resistors are used, any possible output leakage of the not-selected 3-state outputs will cause a frequency deviation. For these reasons, the resistor values must be within the specified ranges.

Influence of supply voltage

The trip levels of the oscillator are fixed at 20% and 80% of V_{CC}. At higher supply voltages the spread of the trip levels decreases in greater proportion because the offset voltage remains constant, and the propagation delay decreases. Furthermore, the R_{ON} values of the push-pull driving stage decrease at higher voltages.

Spread-causing factors

SYMBOL	PARAMETER	T_{amb} = 25 °C			UNIT	V_{CC} (V)
		MIN.	TYP.	MAX.		
V_{off}	offset voltage	–	7	–	mV	1.0
		–	7	–	mV	6.0
t_P	propagation delay	–	22	–	µs	1.0
		–	5.5	–	µs	6.0
R_{ON}	P-channel resistance R_C, R_D outputs	–	170	–	Ω	1.0
		–	25	–	Ω	6.0
R_{ON}	N-channel resistance R_C, R_D outputs	–	250	–	Ω	1.0
		–	35	–	Ω	6.0
R_{ON}	P-channel resistance R_S output	–	1300	–	Ω	1.0
		–	180	–	Ω	6.0
R_{ON}	N-channel resistance R_S output	–	1300	–	Ω	1.0
		–	180	–	Ω	6.0

Error free operation, even under extreme conditions.

Several measures are taken in the circuit design to ensure error-free operation, even with very low supply voltages. Moreover, the circuit has been made very insensitive to the effects of external fields. The measures taken during the design are:

- Use of synchronous logic
- Bistable POR instead of monostable POR
- Data retention assured below a supply voltage of 0.9 V.
- Debounce circuitry on $\overline{\text{DIS}}$ input (maximum expected debounce time = 10 ms)
- Schmitt trigger on PWRS (power sense) input and on $\overline{\text{DIS}}$ input
- Special oscillator security to prevent any malfunction.

Synchronous logic and bistable POR.

Use of synchronous logic results in much lower sensitivity to spikes on input pins. The POR is adapted to fit well into a synchronous environment. An increasing supply voltage sets the POR. The POR output signal is routed to the control logic and divider/counter. It is synchronized with the on-chip clock. After all flip-flops are reset, a reset acknowledge signal is generated which resets the POR. This method ensures that the POR signal is acknowledged in all cases, even at very low voltages.

Data retention.

The circuit may be used in an application where an electric motor is present. When the motor is switched on, it will disturb the supply voltage for a short period. The POR level is set at such a level that, even with very low supply voltages, the POR will not respond during motor switch on. The flip-flops will retain their data during the supply voltage disturbance because of the inherent data retention of any CMOS gate. However, when the battery is almost completely discharged and the motor switch is activated, the dip on the supply voltage line can be too large. The retention of the POR is therefore made deliberately worse than that of the internal flip-flops. The POR will therefore respond long before the flip-flops will loose their data. This results in a proper start condition for a new charge cycle.

Debounce circuitry on $\overline{DIS}$ input.

A discharge cycle is activated by a switch. To protect the circuit from any bounce of the switch contacts, de-bounce circuitry is provided at the $\overline{DIS}$ input. The circuitry allows a switch de-bounce time of max. 10 ms.

Schmitt trigger on PWRS (power sense) input.

The PWRS input can be corrupted by high transients due to disturbances on the mains supply. To suppress any false triggering, the PWRS input is provided with a Schmitt-trigger. However, for some applications, it is advisable to connect a low-value capacitor (150 pF min.) between the PWRS input and GND.

Special oscillator security to prevent any malfunction.

The excellent performance of the oscillator is achieved by using linear op-amp techniques. The oscillator consists of an internal reference, two comparators and a latch. Care was taken to design a very reliable oscillator even with a supply voltage below 0.9 V. If one of the comparators ceases to operate with a supply voltage below 0.9 V, the latch will not be corrupted. Priority was given to stop the oscillator rather than allow uncontrolled oscillation.

All these measures result in reliable 1-cell to 4-cell battery charge management.

Remaining energy indication:

The scan test facility can be used as a remaining energy indication because the value of the counter can be read-out at the scan output ($\overline{MOLLI}$/SCO). This is achieved by briefly interrupting the normal mode of operation, putting the circuit in the scan mode (pin 14 = HIGH), and reading-out of the counter value. The circuit is then returned to the normal mode (pin 14 = LOW or open).

Read-out procedure: The contents of the counter flip-flops can be read-out in the scan mode. To ensure that there is no disturbance of the circuit function, it is essential to either create a round coupled loop by linking the $\overline{MOLLI}$/SCO output (pin 6) directly to the SCI input (pin 15), or to shift-in the serial data of the scan line at the SCI input after completion of the read out cycle. 49 clock pulses are needed on the I_{OSC} input (pin 13) to shift-out the contents of the whole scan line. The most-significant bit of the counter will appear at the $\overline{MOLLI}$/SCO output after the last clock pulse. The least-significant bit after the penultimate clock pulse, etc. Selecting the last three or four bits will yield sufficiently high accuracy to obtain the counter value which represents the remaining energy of the battery.

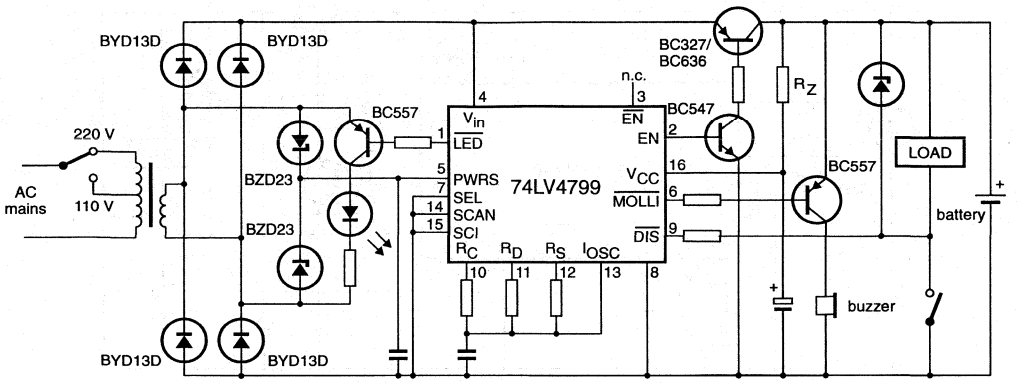


Fig.5 Typical application of the low-voltage 74LV4799.

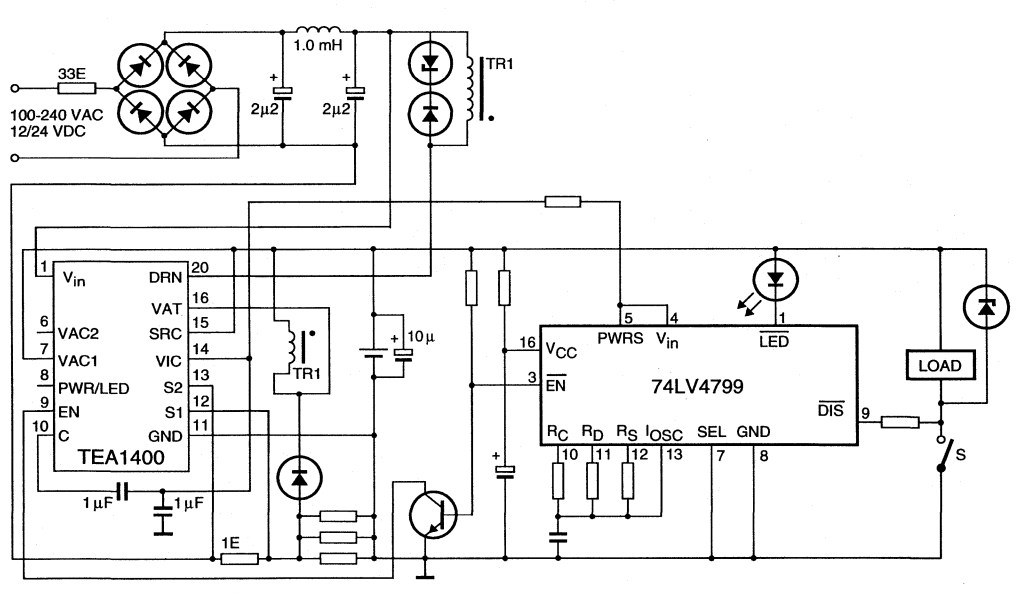
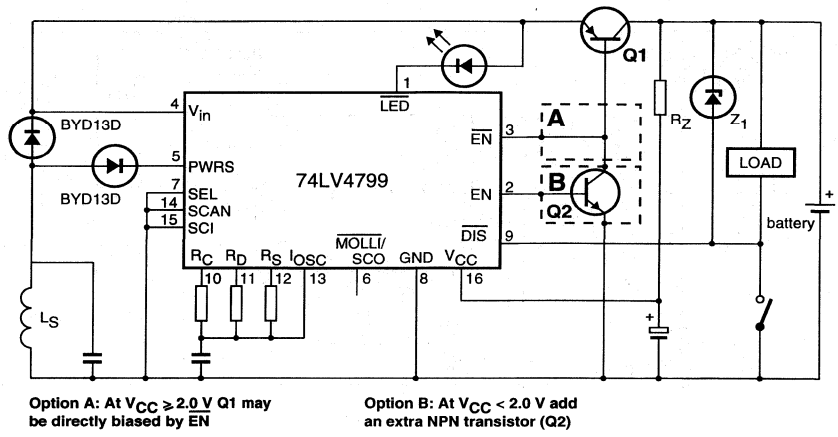


Fig.6 Application diagram of the 74LV4799 in combination with the high-voltage IC TEA1400.



Option A: At $V_{CC} \geq 2.0$ V Q1 may be directly biased by $\overline{EN}$

Option B: At $V_{CC} < 2.0$ V add an extra NPN transistor (Q2)

Fig.7 Inductive loader, showing the two options A and B.

DEVICE DATA

LVC

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **Inputs accept voltages upto 5.5 V**
- **CMOS low power consumption**
- **Direct interface with TTL levels**

DESCRIPTION

The 74LVC00 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment.

The 74LVC00 provides the 2-input NAND function.

FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	C_L = 50 pF V_{CC} = 3.3 V	3.3	ns
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	50	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC00D	14	SO	plastic	SO14/SOT108A
74LVC00DB	14	SSOP	plastic	SSOP14/SOT337
74LVC00PW	14	TSSOP	plastic	TSSOP14/SOT402

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

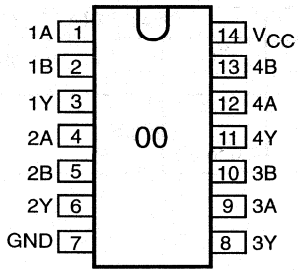


Fig.1 Pin configuration.

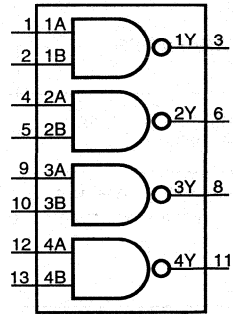


Fig.2 Logic symbol.

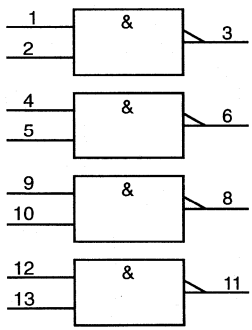


Fig.3 IEC Logic symbol.

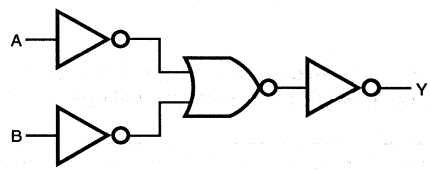


Fig.4 Logic diagram (one gate).

DC CHARACTERISTICS FOR 74LVC00

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74LVC00

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C) −40 to +85			UNIT	TEST CONDITIONS	
		MIN.	TYP.	MAX.		V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	–	20	–	ns	1.2	Fig.5
		1.5	4.0	6.5		2.7	
		1.5	3.5*	6.0		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

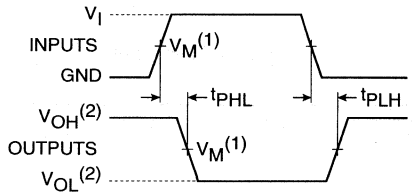
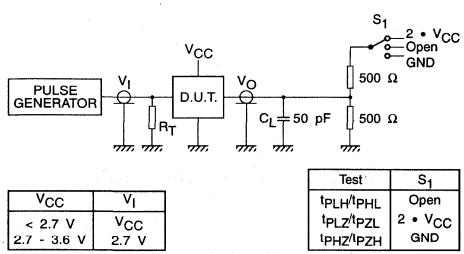


Fig. 5 Waveforms showing the input (nA, nB) to output (nY) propagation delays.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.6 Load circuitry for switching times.

Quad 2-input NOR gate | 74LVC02

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **Inputs accept voltages upto 5.5 V**
- **CMOS low power consumption**
- **Direct interface with TTL levels**

DESCRIPTION

The 74LVC02 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment.

The 74LVC02 provides the 2-input NOR function.

FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	H
L	H	L
H	L	L
H	H	L

H = HIGH voltage level
L = LOW voltage level

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	C_L = 50 pF V_{CC} = 3.3 V	3.3	ns
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	60	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC02D	14	SO	plastic	SO14/SOT108A
74LVC02DB	14	SSOP	plastic	SSOP14/SOT337
74LVC02PW	14	TSSOP	plastic	TSSOP14/SOT402

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	1Y to 4Y	data outputs
2, 5, 8, 11	1A to 4A	data inputs
3, 6, 9, 12	1B to 4B	data inputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

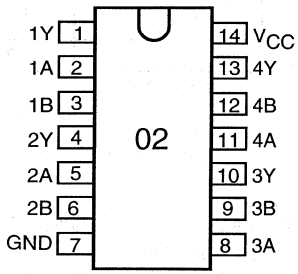


Fig.1 Pin configuration.

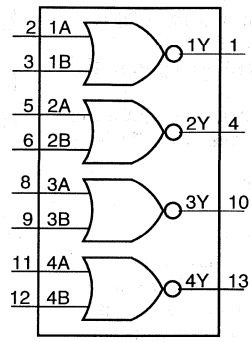


Fig.2 Logic symbol.

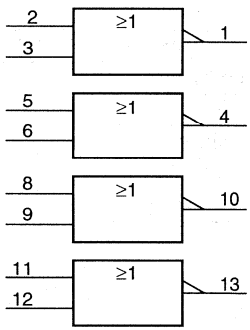


Fig.3 IEC Logic symbol.

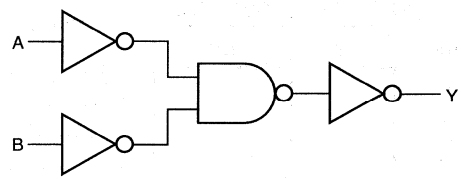


Fig.4 Logic diagram (one gate).

DC CHARACTERISTICS FOR 74LVC02

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74LVC02

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C) −40 to +85			UNIT	TEST CONDITIONS	
		MIN.	TYP.	MAX.		V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	–	20	–	ns	1.2	Fig.5
		1.5	4.0	6.5		2.7	
		1.5	3.5*	6.0		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

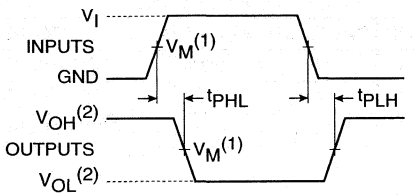
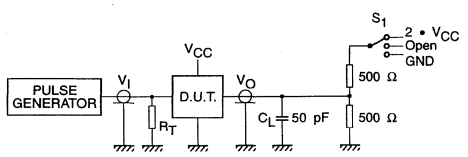


Fig. 5 Waveforms showing the input (nA, nB) to output (nY) propagation delays.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.6 Load circuitry for switching times.

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **Inputs accept voltages upto 5.5 V**
- **CMOS low power consumption**
- **Direct interface with TTL levels**

DESCRIPTION

The 74LVC04 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment.

The 74LVC04 provides six inverting buffers.

FUNCTION TABLE

INPUT	OUTPUT
nA	nY
L	H
H	L

H = HIGH voltage level
L = LOW voltage level

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 50 pF V_{CC} = 3.3 V	3.3	ns
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	45	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC04D	14	SO	plastic	SO14/SOT108A
74LVC04DB	14	SSOP	plastic	SSOP14/SOT337
74LVC04PW	14	TSSOP	plastic	TSSOP14/SOT402

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A to 6A	data inputs
2, 4, 6, 8, 10, 12	1Y to 6Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

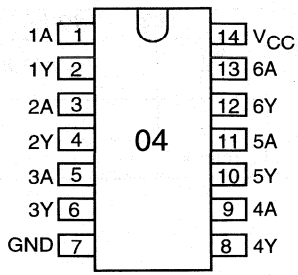


Fig.1 Pin configuration.

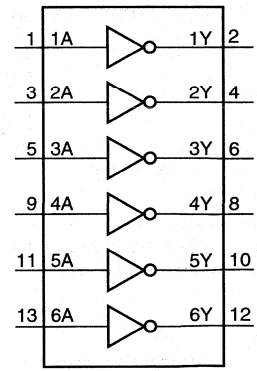


Fig.2 Logic symbol.

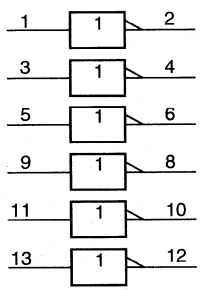


Fig.3 IEC Logic symbol.

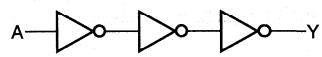


Fig.4 Logic diagram (one inverter).

DC CHARACTERISTICS FOR 74LVC04

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74LVC04

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		−40 to +85				V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t_{PHL}/t_{PLH}	propagation delay nA to nY	–	20	–	ns	1.2	Fig.5
		1.5	4.0	6.5		2.7	
		1.5	3.5*	6.0		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

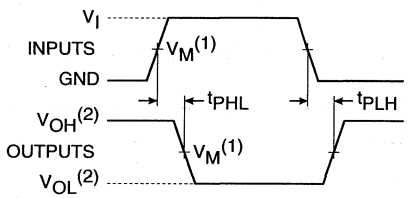
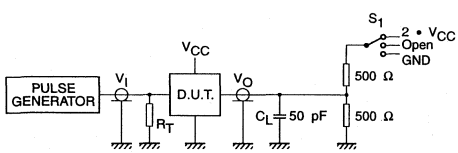


Fig. 5 Waveforms showing the input (nA) to output (nY) propagation delays.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.6 Load circuitry for switching times.

Quad 2-input AND gate | 74LVC08

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **Inputs accept voltages upto 5.5 V**
- **CMOS low power consumption**
- **Direct interface with TTL levels**

DESCRIPTION

The 74LVC08 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment.

The 74LVC08 provides the 2-input AND function.

FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	L
L	H	L
H	L	L
H	H	H

H = HIGH voltage level
L = LOW voltage level

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	C_L = 50 pF; V_{CC} = 3.3 V	3.3	ns
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	50	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC08D	14	SO	plastic	SO14/SOT108A
74LVC08DB	14	SSOP	plastic	SSOP14/SOT337
74LVC08PW	14	TSSOP	plastic	TSSOP14/SOT402

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

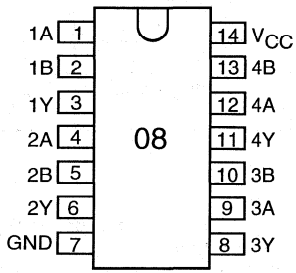


Fig.1 Pin configuration.

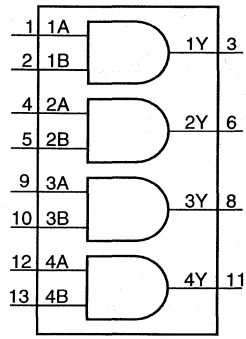


Fig.2 Logic symbol.

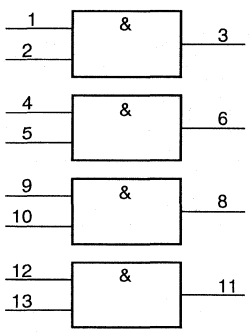


Fig.3 IEC Logic symbol.

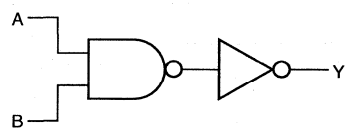


Fig.4 Logic diagram (one gate).

DC CHARACTERISTICS FOR 74LVC08

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74LVC08

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C) −40 to +85			UNIT	TEST CONDITIONS	
		MIN.	TYP.	MAX.		V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	–	20	–	ns	1.2	Fig.5
		1.5	4.0	6.5		2.7	
		1.5	3.5*	6.0		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

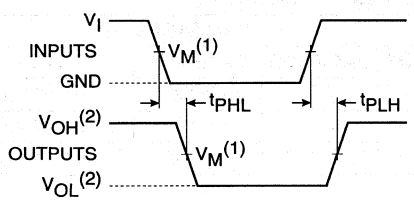
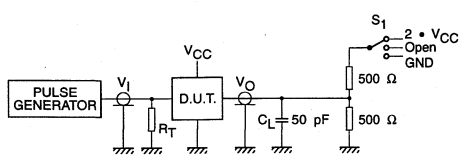


Fig.5 Waveforms showing the input (nA, nB) to output (nY) propagation delays.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.6 Load circuitry for switching times.

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **Inputs accept voltages upto 5.5 V**
- **CMOS low power consumption**
- **Direct interface with TTL levels**

DESCRIPTION

The 74LVC00 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment.

The 74LVC32 provides the 2-input OR function.

FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	H

H = HIGH voltage level
L = LOW voltage level

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	C_L = 50 pF; V_{CC} = 3.3 V	3.3	ns
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	50	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC32D	14	SO	plastic	SO14/SOT108A
74LVC32DB	14	SSOP	plastic	SSOP14/SOT337
74LVC32PW	14	TSSOP	plastic	TSSOP14/SOT402

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

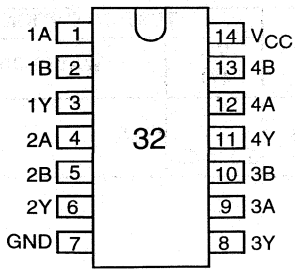


Fig.1 Pin configuration.

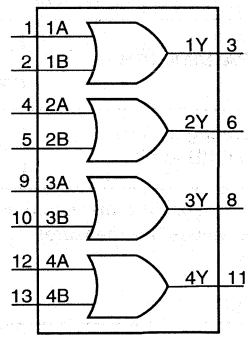


Fig.2 Logic symbol.

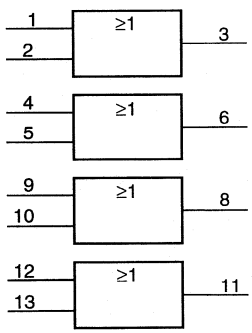


Fig.3 IEC Logic symbol.

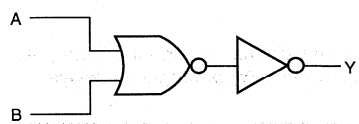


Fig.4 Logic diagram (one gate).

DC CHARACTERISTICS FOR 74LVC32

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74LVC32

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		−40 to +85				V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	–	20	–	ns	1.2	Fig.5
		1.5	4.0	6.5		2.7	
		1.5	3.5*	6.0		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

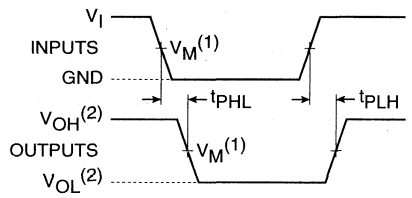
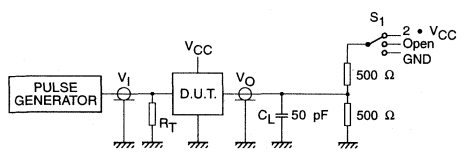


Fig. 5 Waveforms showing the input (nA, nB) to output (nY) propagation delays.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.6 Load circuitry for switching times.

Quad 2-input NAND buffer (open drain) 74LVC38

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **Inputs accept voltages upto 5.5 V**
- **Open drain outputs**
- **CMOS low power consumption**
- **Direct interface with TTL levels**

DESCRIPTION

The 74LVC38 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment.

The 74LVC38 provides the 2-input NAND function.

FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	Z
L	H	Z
H	L	Z
H	H	L

H = HIGH voltage level
L = LOW voltage level
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PZL}	propagation delay nA, nB to nY	C_L = 50 pF V_{CC} = 3.3 V	2.7	ns
t_{PLZ}	propagation delay nA, nB to nY	C_L = 50 pF V_{CC} = 3.3 V	5.0	ns
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	20	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o) +$
   $\Sigma (V_O^2/R_L) \times$ duty factor LOW, where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   V_O = output voltage in V; R_L = pull-up resistor in MΩ;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}
3. The given value of C_{PD} is obtained with: C_L = 0 pF and $R_L = \infty$

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC38D	14	SO	plastic	SO14/SOT108A
74LVC38DB	14	SSOP	plastic	SSOP14/SOT337
74LVC38PW	14	TSSOP	plastic	TSSOP14/SOT402

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

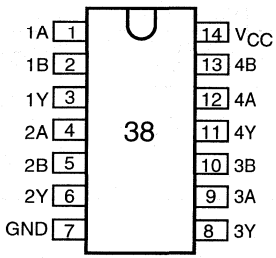


Fig.1 Pin configuration.

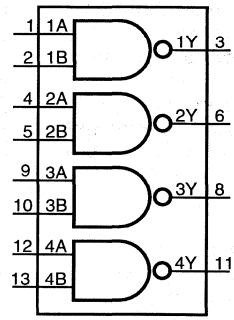


Fig.2 Logic symbol.

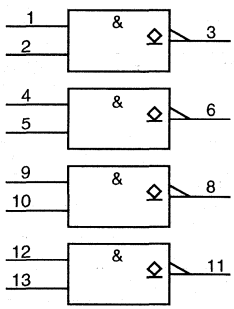


Fig.3 IEC Logic symbol.

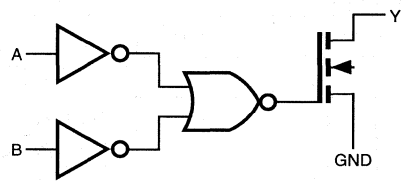


Fig.4 Logic diagram (one gate).

DC CHARACTERISTICS FOR THE 74LVC38

Over recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C) −40 to +85			UNIT	TEST CONDITIONS		
		MIN.	TYP.	MAX.		V_{CC} (V)	V_I	OTHER
V_{IH}	HIGH level input voltage	0.9 2.0	– –	– –	V	1.2 2.7 to 3.6		
V_{IL}	LOW level input voltage	– –	– –	0.3 0.8	V	1.2 2.7 to 3.6		
V_{OL}	LOW level output voltage	– – –	– – –	0.40 0.20 0.55	V	2.7 3.0 3.0	V_{IH} or V_{IL}	I_O = 12 mA I_O = 100 µA I_O = 24 mA
I_I	input leakage current	–	±0.1	±5	µA	3.6	5.5 V or GND	not for I/O pins
I_{OZ}	3-state output OFF-state current	–	0.1	±10	µA	3.6	V_{IH} or V_{IL}	V_O = V_{CC} or GND
I_{CC}	quiescent supply current	–	0.1	20	µA	3.6	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current given per input pin	–	5	500	µA	2.7 to 3.6	V_{CC} − 0.6 V	I_O = 0

Note: All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

AC CHARACTERISTICS FOR 74LVC38

GND = 0 V; $t_r = t_f \leq 2.5$ ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C) −40 to +85			UNIT	TEST CONDITIONS	
		MIN.	TYP.	MAX.		V_{CC} (V)	WAVEFORMS
t_{PZL}	propagation delay nA, nB to nY	– 1.5 1.5	20 3.5 2.7*	– 6.0 5.0	ns	1.2 2.7 3.0 to 3.6	Fig.5
t_{PLZ}	propagation delay nA, nB to nY	– 1.5 1.5	20 6.2 5.0*	– 7.5 6.5	ns	1.2 2.7 3.0 to 3.6	Fig.5, 6

Notes: All typical values are measured at T_{amb} = 25 °C.

* Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

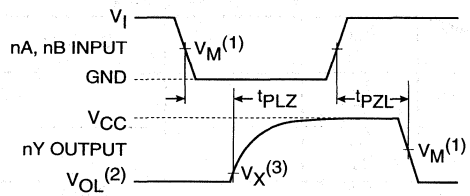


Fig. 5 Waveforms showing the input (nA, nB) to output (nY) propagation delays.

Notes:

(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

TEST CIRCUIT

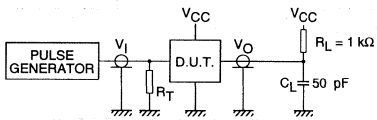


Fig.6 Test circuit (open drain).

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

$t_r = t_f \leq 2.5$ ns; when measuring f_{max}, there is no constraint on t_r, t_f with 50% duty factor.

Dual D-type flip-flop with set and reset; positive-edge trigger

74LVC74

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **Inputs accept voltages upto 5.5 V**
- **CMOS low power consumption**
- **Direct interface with TTL levels**
- **Output drive capability 50 Ω transmission lines @ 85 °C**

GENERAL DESCRIPTION

The 74LVC74 is a high-performance low-voltage Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74LVC74 is a dual positive edge triggered, D-type flip-flop with individual data (D) inputs, clock (CP) inputs, set ($\overline{S_D}$) and ($\overline{R_D}$) inputs; also complementary Q and $\overline{Q}$ outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition, for predictable operation.

Schmitt-trigger action in all data inputs makes the circuit highly tolerant to slower clock rise and fall times.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f$ =2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nCP to nQ, n$\overline{Q}$ n$\overline{S}_D$ to nQ, n$\overline{Q}$ n$\overline{R}_D$ to nQ, n$\overline{Q}$	C_L = 50pF V_{CC} = 3.3 V	 3.8 4.8 4.8	ns
f_{max}	maximum clock frequency		250	MHz
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	15	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC74D	14	SO	plastic	SO14/SOT108A
74LVC74DB	14	SSOP	plastic	SSOP14/SOT337
74LVC74PW	14	TSSOP	plastic	TSSOP14/SOT402

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 13	1$\overline{R}_D$, 2$\overline{R}_D$	asynchronous reset-direct input (active LOW)
2, 12	1D, 2D	data inputs
3, 11	1CP, 2CP	clock input (LOW-to-HIGH, edge-triggered)
4, 10	1$\overline{S}_D$, 2$\overline{S}_D$	asynchronous set-direct input (active LOW)
5, 9	1Q, 2Q	true flip-flop outputs
6, 8	1$\overline{Q}$, 2$\overline{Q}$	complement flip-flop outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

Dual D-type flip-flop with set and reset; positive-edge trigger

74LVC74

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{S}_D$	$\overline{R}_D$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH CP transition
Q_{n+1} = state after the next LOW-to-HIGH CP transition

INPUTS				OUTPUTS	
$\overline{S}_D$	$\overline{R}_D$	CP	D	Q_{n+1}	$\overline{Q}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

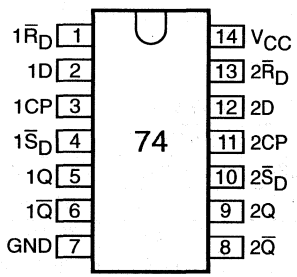


Fig.1 Pin configuration.

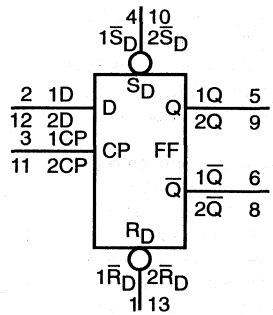


Fig.2 Logic symbol.

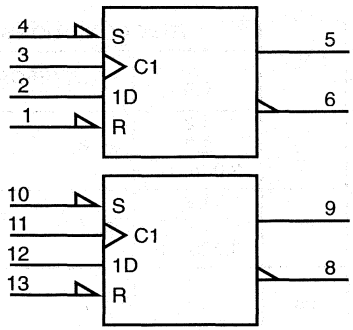


Fig.3 IEC Logic symbol.

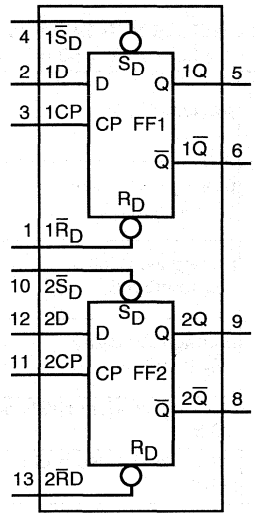


Fig.4 Functional diagram.

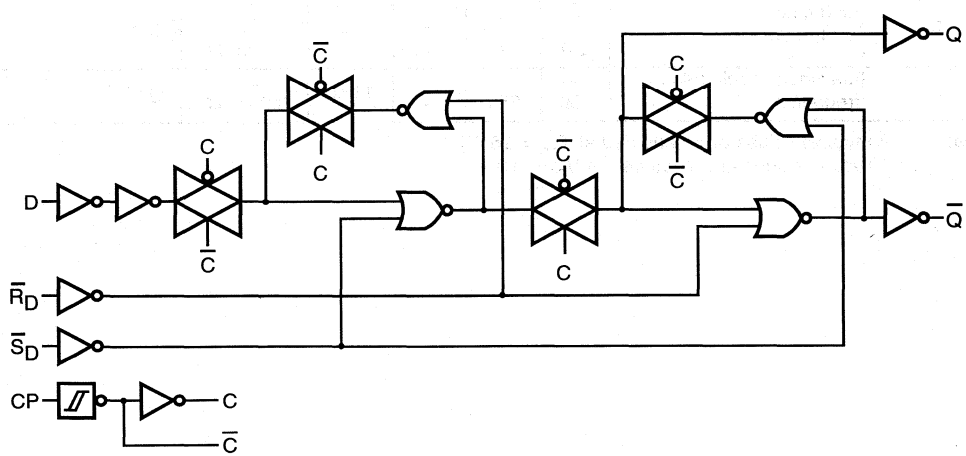


Fig.5 Logic diagram (one flip-flop).

DC CHARACTERISTICS FOR 74LVC74

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74LVC74

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		−40 to +85				V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t_{PHL}/t_{PLH}	propagation delay nCP to nQ, n$\overline{Q}$	– – –	– – 3.8*	– 7.0 6.0	ns	1.2 2.7 3.0 to 3.6	Fig. 6
t_{PHL}/t_{PLH}	propagation delay n$\overline{S}_D$ to nQ, n$\overline{Q}$	– – –	– – 4.8*	– 8.5 7.5	ns	1.2 2.7 3.0 to 3.6	Fig. 7
t_{PHL}/t_{PLH}	propagation delay n$\overline{R}_D$ to nQ, n$\overline{Q}$	– – –	– – 4.8*	– 8.5 7.5	ns	1.2 2.7 3.0 to 3.6	Fig. 7
t_W	clock pulse width HIGH or LOW	– 3.3	– 2.0	– –	ns	2.7 3.0 to 3.6	Fig. 6
t_W	set or reset pulse width LOW	– 2.0	– –	– –	ns	2.7 3.0 to 3.6	Fig. 7
t_{rem}	removal time set or reset	– – 2.0	– – –	– – –	ns	1.2 2.7 3.0 to 3.6	Fig. 7
t_{su}	set–up time nD to nCP	– – 2.0	– – –	– – –	ns	1.2 2.7 3.0 to 3.6	Fig. 6
t_h	hold time nD to nCP	– – 2.0	– – –	– – –	ns	1.2 2.7 3.0 to 3.6	Fig. 6
f_{max}	maximum clock pulse frequency	– 150	– 250	– –	MHz	2.7 3.0 to 3.6	Fig. 6

Notes: All typical values are measured at T_{amb} = 25 °C.
* Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

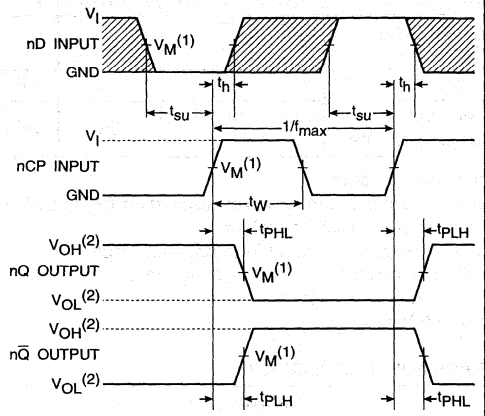


Fig. 6 Waveforms showing the clock (nCP) to output (nQ, nQ̄) propagation delays, the clock pulse width, the nD to nCP set-up times, the nCP to nD hold times and the maximum clock pulse frequency.

Note to Fig.6

The shaded areas indicate when the input is permitted to change for predictable output performance.

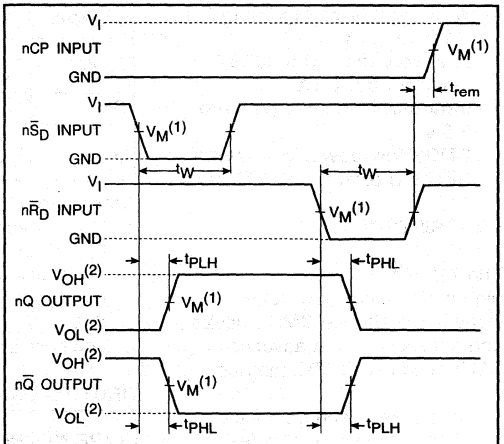
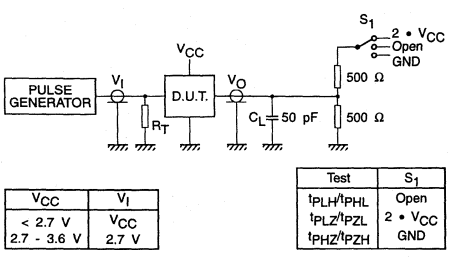


Fig.7 Waveforms showing the set ($n\overline{S}_D$) and reset ($n\overline{R}_D$) input to output (nQ, nQ̄) propagation delays, the set and reset pulse widths and the $n\overline{R}_D$ to nCP removal time.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.8 Load circuitry for switching times.

Notes: (1) V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
V_M = 0.5 · V_{CC} at V_{CC} < 2.7 V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

Quad 2-input EXCLUSIVE-OR gate | 74LVC86

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **Inputs accept voltages upto 5.5 V**
- **CMOS low power consumption**
- **Direct interface with TTL levels**

DESCRIPTION

The 74LVC86 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment.

The 74LV86 provides the 2-input EXCLUSIVE-OR function.

FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF V_{CC} = 3.3 V	3.7	ns
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	55	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC86D	14	SO	plastic	SO14/SOT108A
74LVC86DB	14	SSOP	plastic	SSOP14/SOT337
74LVC86PW	14	TSSOP	plastic	TSSOP14/SOT402

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

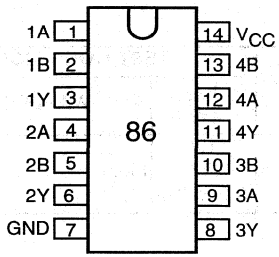


Fig.1 Pin configuration.

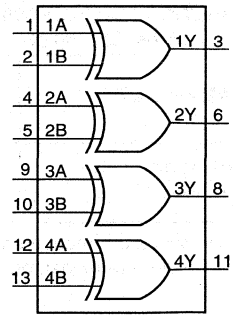


Fig.2 Logic symbol.

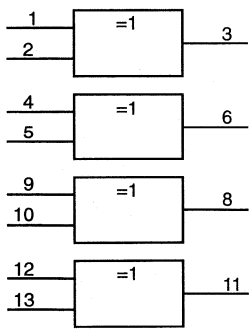


Fig.3 IEC Logic symbol.

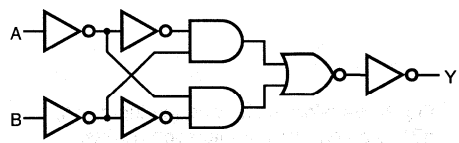


Fig.4 Logic diagram (one gate).

DC CHARACTERISTICS FOR 74LVC86

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LVC86

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C) −40 to +85			UNIT	TEST CONDITIONS	
		MIN.	TYP.	MAX.		V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	–	20	–	ns	1.2	Fig.5
		1.5	4.5	7.0		2.7	
		1.5	4.0*	6.5		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

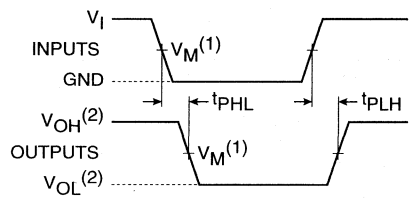
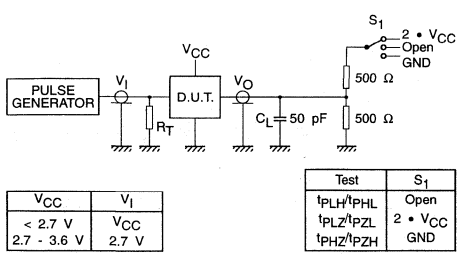


Fig. 5 Waveforms showing the input (nA, nB) to output (nY) propagation delays.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.6 Load circuitry for switching times.

Dual $J\overline{K}$ flip-flop with set and reset; positive-edge trigger 74LVC109

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **Inputs accept voltages upto 5.5 V**
- **CMOS low power consumption**
- **Direct interface with TTL levels**
- **Output capability: standard**
- **I_{CC} category: flip-flops**

DESCRIPTION

The 74LVC109 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT109.

The 74LVC109 is a dual positive-edge triggered JK-type flip-flop featuring individual J, $\overline{K}$ inputs, clock (CP) inputs, set ($\overline{S}_D$) and reset ($\overline{R}_D$) inputs; also complementary Q and $\overline{Q}$ outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input.

The J and $\overline{K}$ inputs control the state changes of the flip-flops as described in the mode select function table.
The J and $\overline{K}$ inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

The $J\overline{K}$ design allows operation as a D-type flip-flop by tying the J and $\overline{K}$ inputs together.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nCP to nQ, n$\overline{Q}$ n$\overline{S}_D$ to nQ, n$\overline{Q}$ n$\overline{R}_D$ to nQ, n$\overline{Q}$	C_L = 15 pF V_{CC} = 3.3 V	 4.0 4.5 4.5	ns
f_{max}	maximum clock frequency		250	MHz
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	15	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC109D	16	SO	plastic	SO16/SOT109A
74LVC109DB	16	SSOP	plastic	SSOP16/SOT338
74LVC109PW	16	TSSOP	plastic	TSSOP16/SOT403

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1, 15	1$\overline{R}_D$, 2$\overline{R}_D$	asynchronous reset input (active LOW)
2, 14, 3, 13	1J, 2J, 1$\overline{K}$, 2$\overline{K}$	synchronous inputs; flip-flops 1 and 2
4, 12	1CP, 2CP	clock input (LOW-to-HIGH, edge-triggered)
5, 11	1$\overline{S}_D$, 2$\overline{S}_D$	asynchronous set inputs (active LOW)
6, 10	1Q, 2Q	true flip-flop outputs
7, 9	1$\overline{Q}$, 2$\overline{Q}$	complement flip-flop outputs
8	GND	ground (0 V)
16	V_{CC}	positive supply voltage

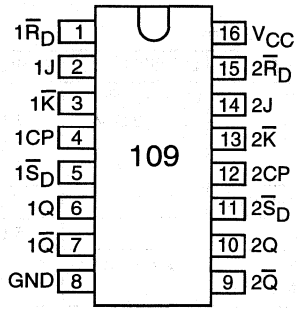


Fig.1 Pin configuration.

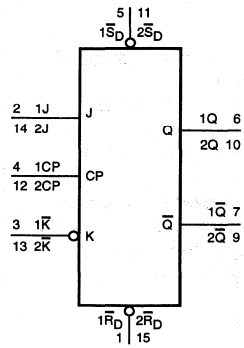


Fig.2 Logic symbol.

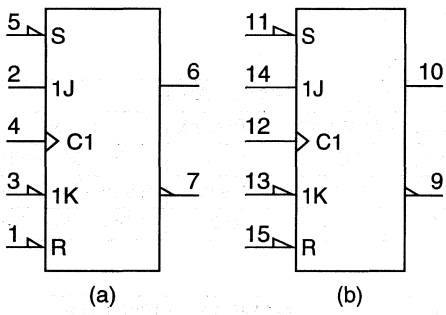


Fig3. IEC logic symbol.

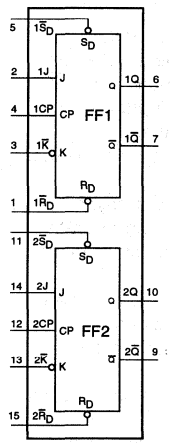


Fig.4 Functional diagram.

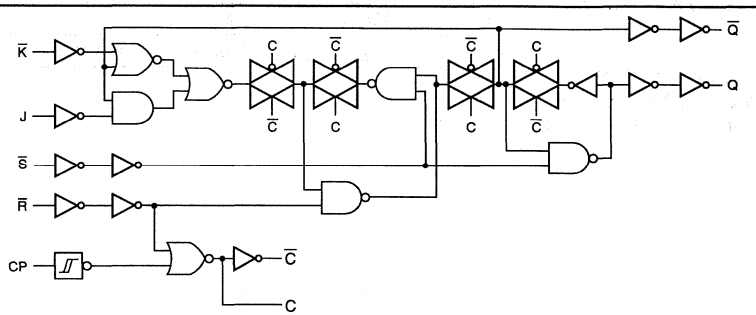


Fig.5 Logic diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS					OUTPUTS	
	$n\overline{S}_D$	$n\overline{R}_D$	nCP	nJ	$n\overline{K}$	nQ	$n\overline{Q}$
asynchronous set	L	H	X	X	X	H	L
asynchronous reset	H	L	X	X	X	L	H
undetermined	L	L	X	X	X	H	H
toggle	H	H	↑	h	l	$\overline{q}$	q
load "0" (reset)	H	H	↑	l	l	L	H
load "1" (set)	H	H	↑	h	h	H	L
hold "no change"	H	H	↑	l	h	q	$\overline{q}$

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition.
X = don't care
↑ = LOW-to-HIGH CP transition

DC CHARACTERISTICS FOR 74LVC109

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: standard
I_{CC} category: flip-flops

AC CHARACTERISTICS FOR 74LVC109

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		−40 to +85				V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t_{PHL}/t_{PLH}	propagation delay nCP to nQ, nQ	–	–	–	ns	1.2	Fig.6
		–	–	7.5		2.7	
		–	4.0*	6.5		3.0 to 3.6	
t_{PLH}	propagation delay nS_D to nQ, nQ	–	–	–	ns	1.2	Fig.7
		–	–	8.0		2.7	
		–	4.5*	7.0		3.0 to 3.6	
t_{PHL}	propagation delay nR_D to nQ, nQ	–	–	–	ns	1.2	Fig.7
		–	–	8.0		2.7	
		–	4.5*	7.0		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC CHARACTERISTICS FOR 74LVC109 *(Continued)*

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		−40 to +85				V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t_w	clock pulse width HIGH or LOW	– 3.3	– 2.0*	– –	ns	2.7 3.0 to 3.6	Fig.6
t_w	set or reset pulse width HIGH or LOW	3.0 2.0	– –	– –	ns	2.7 3.0 to 3.6	Fig.7
t_{rem}	removal time $n\overline{S}_D$, $n\overline{R}_D$ to nCP	– 3.0 2.0	– – –	– – –	ns	1.2 2.7 3.0 to 3.6	Fig.7
t_{su}	set-up time nJ, $n\overline{K}$ to nCP	– 2.5 2.0	– – –	– – –	ns	1.2 2.7 3.0 to 3.6	Fig.6
t_h	hold time nJ, $n\overline{K}$ to nCP	– 2.5 2.0	– – –	– – –	ns	1.2 2.7 3.0 to 3.6	Fig.6
f_{max}	maximum clock pulse frequency	– 150	– 250*	– –	MHz	2.7 3.0 to 3.6	Fig.6

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

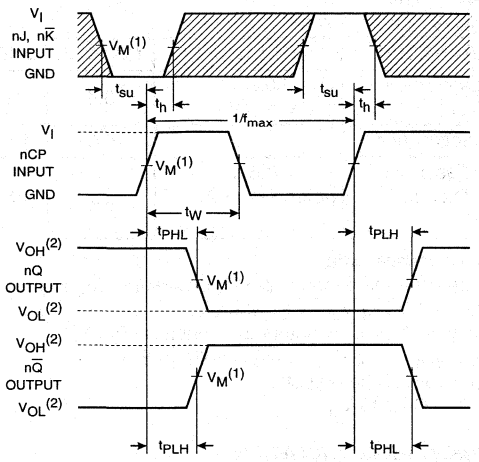


Fig.6 Waveforms showing the clock (nCP) to output (nQ, $n\overline{Q}$) propagation delays, the clock pulse width, the nJ, $n\overline{K}$ to nCP set-up, the nCP to nJ, $n\overline{K}$ hold times and the maximum clock pulse frequency.

Note to Fig.6: The shaded areas indicate when the input is permitted to change for predictable output performance.

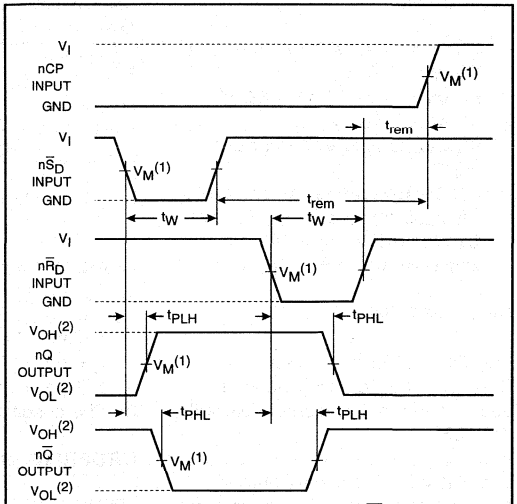
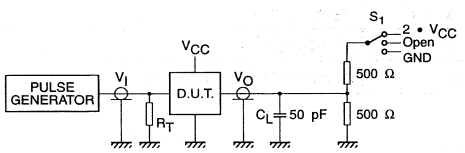


Fig.7 Waveforms showing the set ($n\overline{S}_D$) and reset ($n\overline{R}_D$) input to output (nQ, $n\overline{Q}$) propagation delays, the set and reset pulse widths and the $n\overline{R}_D$, $n\overline{S}_D$ to nCP removal time.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.8 Load circuitry for switching times.

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **Inputs accept voltages upto 5.5 V**
- **CMOS low power consumption**
- **Direct interface with TTL levels**
- **Output drive capability 50 Ω transmission lines @ 85 °C**

DESCRIPTION

The 74LVC125 is a low-voltage Si-gate CMOS device and is pin, speed and function compatible with 74F125.

The 74LVC125 consists of four non-inverting buffers/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable input ($n\overline{OE}$). A HIGH at $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state.

FUNCTION TABLE

INPUTS		OUTPUT
$n\overline{OE}$	nA	nY
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f$ = 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 50 pF V_{CC} = 3.3 V	3.4	ns
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per buffer	V_{CC} = 3.3 V notes 1 and 2	20	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC125D	14	SO	plastic	SO14/SOT108A
74LVC125DB	14	SSOP	plastic	SSOP14/SOT337
74LVC125PW	14	TSSOP	plastic	TSSOP14/SOT402

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	$1\overline{OE}$ to $4\overline{OE}$	output enable inputs (active LOW)
2, 5, 9, 12	1A to 4A	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

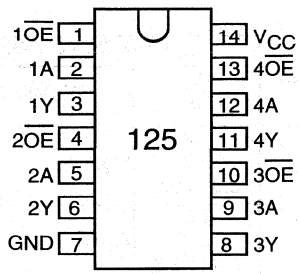


Fig.1 Pin configuration.

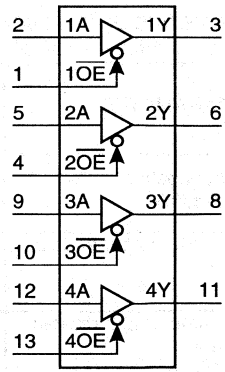


Fig.2 Logic symbol.

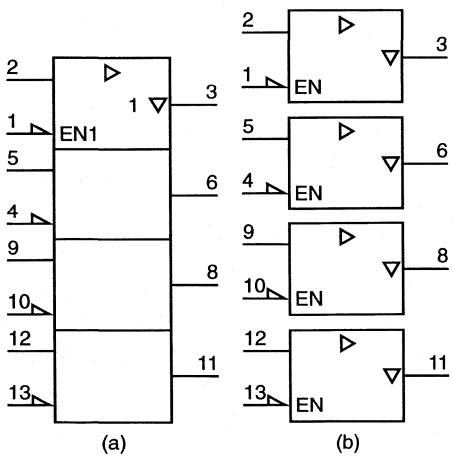


Fig.3 IEC Logic symbol.

DC CHARACTERISTICS FOR 74LVC125

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LVC125

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		−40 to +85				V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t_{PHL}/t_{PLH}	propagation delay nA to nY	–	–	–	ns	1.2	Fig.4
		–	3.8	6.0		2.7	
		–	3.4*	5.5		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time $n\overline{OE}$ to nY	–	–	–	ns	1.2	Fig.5
		–	4.4	7.0		2.7	
		–	3.5*	6.0		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time $n\overline{OE}$ to nY	–	–	–	ns	1.2	Fig.5
		–	4.0	5.5		2.7	
		–	3.3*	4.5		3.0 to 3.6	

Notes: All typical values are measured at T_{amb} = 25 °C.
* Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

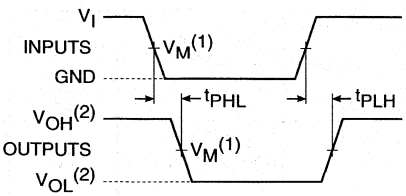


Fig.4 Waveforms showing the input (nA) to output (nY) propagation delays.

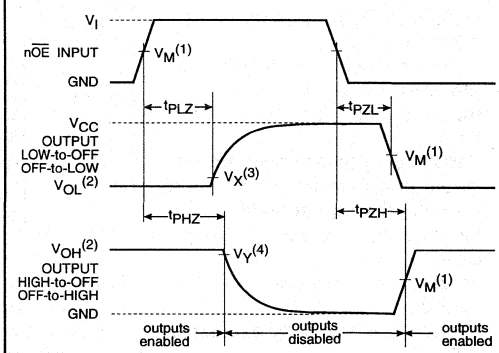
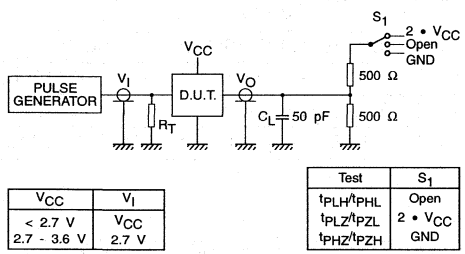


Fig.5 Waveforms showing the 3-state enable and disable times.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.6 Load circuitry for switching times.

Notes:

(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **Inputs accept voltages up to 5.5 V**
- **CMOS low power consumption**
- **Direct interface with TTL levels**
- **Demultiplexing capability**
- **Multiple input enable for easy expansion**
- **Ideal for memory chip select decoding**
- **Active LOW mutually exclusive outputs**
- **Output drive capability 50 Ω transmission lines @ 85 °C**

DESCRIPTION

The 74LVC138 is a low-voltage, low-power, high-performance Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74LVC138 accepts three binary weighted address inputs (A_0, A_1, A_2) and when enabled, provide 8 mutually exclusive active LOW outputs ($\overline{Y}_0$ to $\overline{Y}_7$).
The '138 features three enable inputs: two active LOW ($\overline{E}_1$ and $\overline{E}_2$ and one active HIGH (E_3). Every output will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH.

This multiple enable function allows easy parallel expansion of the '138' to a 1-of-32 (5 lines to 32 lines) decoder with just four '138' ICs and one inverter. The '138 can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Unused enable inputs must be permanently tied to their appropriate active HIGH or LOW state.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay An to $\overline{Y}n$, E3 to $\overline{Y}n$, $\overline{E}n$ to $\overline{Y}n$	C_L = 15 pF V_{CC} = 3.3 V	4.0 4.4	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per package	V_{CC} = 3.3 V notes 1 and 2	22	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC138D	14	SO	plastic	SO14/SOT108A
74LVC138DB	14	SSOP	plastic	SSOP14/SOT337
74LVC138PW	14	TSSOP	plastic	TSSOP14/SOT402

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	A_0 to A_2	address inputs
4, 5	$\overline{E}_1$, $\overline{E}_2$	enable inputs (active LOW)
6	E_3	enable inputs (active HIGH)
15, 14, 13, 12, 11, 10, 9, 7	$\overline{Y}_0$ to $\overline{Y}_7$	outputs
8	GND	ground (0 V)
16	V_{CC}	positive supply voltage

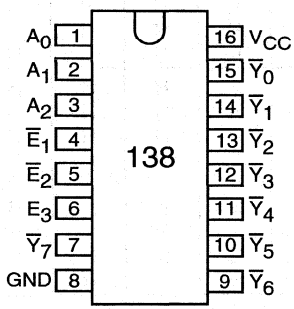


Fig.1 Pin configuration.

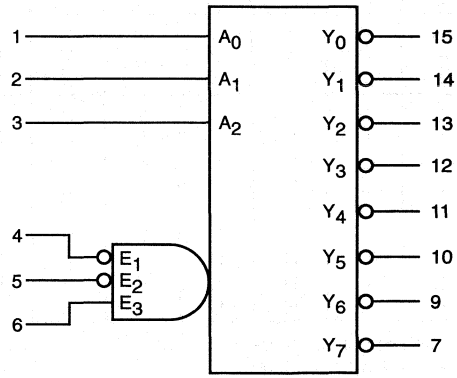


Fig.2 Logic diagram.

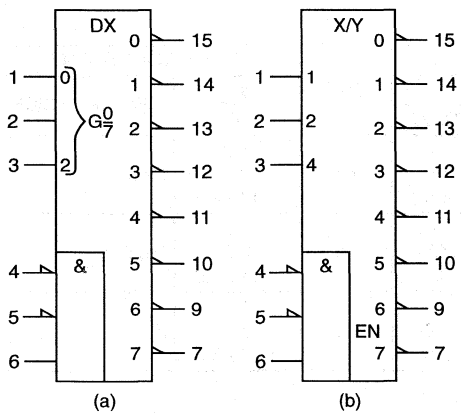


Fig.3 IEC logic symbol.

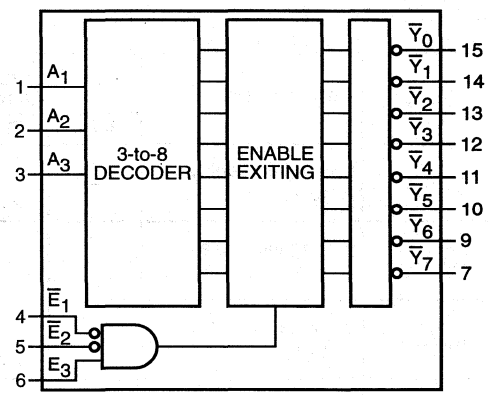


Fig.4 Functional diagram.

FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	$\overline{Y}_4$	$\overline{Y}_5$	$\overline{Y}_6$	$\overline{Y}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care

DC CHARACTERISTICS FOR 74LVC138

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LVC138

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		−40 to +85				V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t_{PHL}/t_{PLH}	propagation delay A_n to $\overline{Y}_n$	– – –	– – 4.0*	– 7.0 6.0	ns	1.2 2.7 3.0 to 3.6	Fig.5
t_{PHL}/t_{PLH}	propagation delay E_3 to $\overline{Y}_n$	– – –	– – 4.5*	– 7.5 6.5	ns	1.2 2.7 3.0 to 3.6	Fig.5
t_{PHL}/t_{PLH}	propagation delay $\overline{E}_n$ to $\overline{Y}_n$	– – –	– – 4.0*	– 7.0 6.0	ns	1.2 2.7 3.0 to 3.6	Fig.6

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

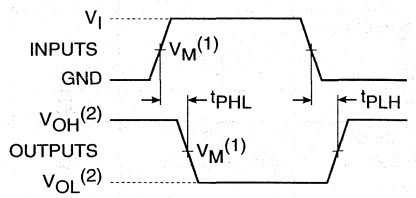


Fig. 5 Waveforms showing the address input (An) and enable input (E_3) to output (Yn) propagation delays.

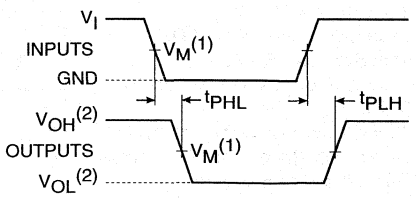
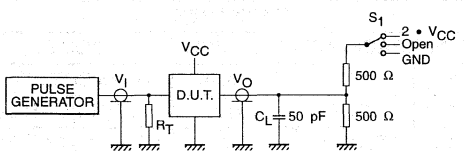


Fig. 6 Waveforms showing the enable input ($\overline{E}_n$) to output (Yn) propagation delays.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.7 Load circuitry for switching times.

Notes: (1) V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
$V_M = 0.5 \cdot V_{CC}$ at V_{CC} < 2.7 V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

Dual 2-to-4 line decoder/demultiplexer — 74LVC139

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **Inputs accept voltages up to 5.5 V**
- **CMOS low power consumption**
- **Direct interface with TTL levels**
- **Demultiplexing capability**
- **Two independent 2-to-4 decoders**
- **Multifunction capability**
- **Active LOW mutually exclusive outputs**
- **Active LOW mutually exclusive outputs**
- **Output drive capability 50 Ω transmission lines @ 85 °C**

DESCRIPTION

The 74LVC138 is a low-voltage, low-power, high-performance Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74LVC139 is a dual 2-to-4 line decoder/demultiplexer. This device has two independent decoders, each accepting two binary weighted inputs (nA_0 and nA_1) and providing four mutually exclusive active LOW outputs ($n\overline{Y}_0$ to $n\overline{Y}_3$). Each decoder has an active LOW enable input ($n\overline{E}$).
When $n\overline{E}$ is HIGH, every output is forced HIGH. The enable can be used as the data input for a 1-to-4 demultiplexer application.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA_n to $n\overline{Y}_n$, $n\overline{E}$ to $n\overline{Y}_n$	C_L = 15 pF V_{CC} = 3.3 V	4.0 4.5	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per multiplexer	V_{CC} = 3.3 V notes 1 and 2	22	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC139D	16	SO	plastic	SO16/SOT109A
74LVC139DB	16	SSOP	plastic	SSOP16/SOT338
74LVC139PW	16	TSSOP	plastic	TSSOP16/SOT403

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$1\overline{E}$, $2\overline{E}$	enable inputs (active LOW)
2, 3	$1A_0$, $1A_1$	address inputs
4, 5, 6, 7	$1\overline{Y}_0$ to $1\overline{Y}_3$	outputs (active LOW)
8	GND	ground (0 V)
12, 11, 10, 9	$2\overline{Y}_0$ to $2\overline{Y}_3$	outputs (active LOW)
14, 13	$2A_0$, $2A_1$	address inputs
16	V_{CC}	positive supply voltage

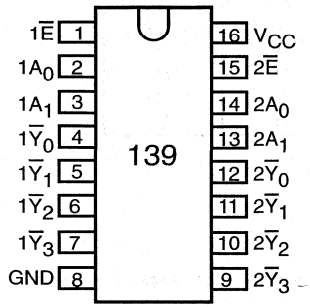


Fig.1 Pin configuration.

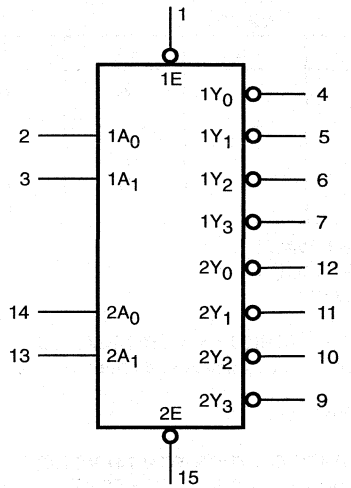


Fig.2 Logic diagram.

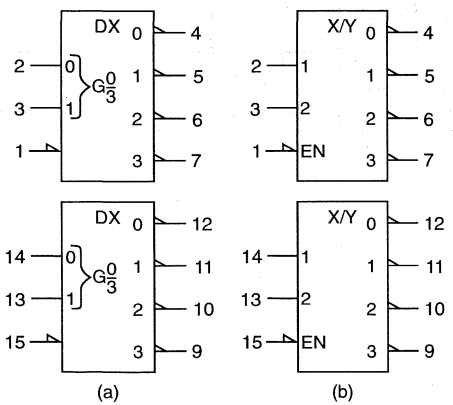


Fig.3 IEC logic symbol.

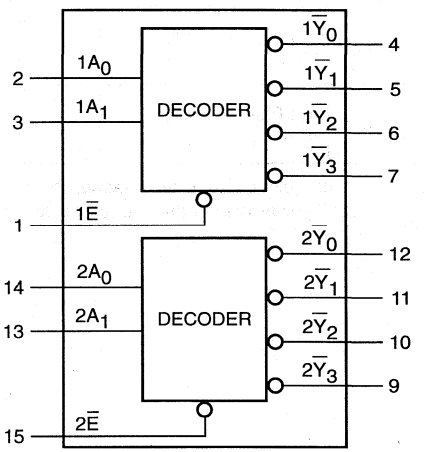


Fig.4 Functional diagram.

FUNCTION TABLE

INPUTS			OUTPUTS			
$n\overline{E}$	nA_0	nA_1	$n\overline{Y}_0$	$n\overline{Y}_1$	$n\overline{Y}_2$	$n\overline{Y}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care

DC CHARACTERISTICS FOR 74LVC139

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LVC139

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		-40 to +85				V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t_{PHL}/t_{PLH}	propagation delay nA_n to Y_n	–	–	–	ns	1.2	Fig.5
		–	–	7.0		2.7	
		–	4.0*	6.0		3.0 to 3.6	
t_{PHL}/t_{PLH}	propagation delay $n\overline{E}$ to Y_n	–	–	–	ns	1.2	Fig.6
		–	–	7.5		2.7	
		–	4.5*	6.5		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

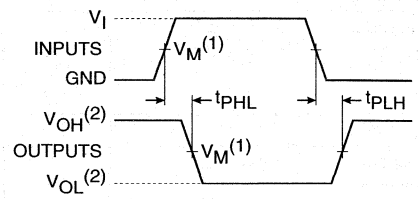


Fig. 5 Waveforms showing the address input (nA_n) to output (nY_n) propagation delays.

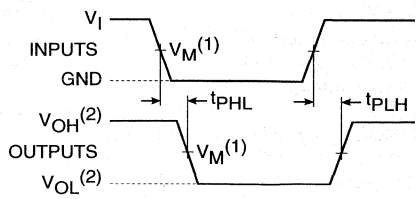
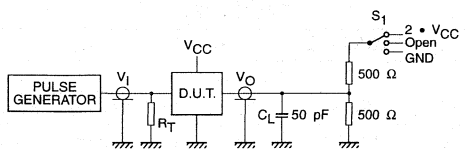


Fig. 6 Waveforms showing the enable input (nE) to output (nY_n) propagation delays.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.7 Load circuitry for switching times.

Notes: (1) V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
$V_M = 0.5 \cdot V_{CC}$ at V_{CC} < 2.7 V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

Quad 2-input multiplexer | 74LVC157

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **Inputs accept voltages upto 5.5 V**
- **CMOS low power consumption**
- **Direct interface with TTL levels**
- **Output drive capability 50 Ω transmission lines @ 85 °C**
- **Non-inverting data path**

DESCRIPTION

The 74LVC157 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74LVC157 is a quad 2-input multiplexer which select 4 bits of data from two sources under the control of a common data select input (S). The four outputs present the selected data in the true (non-inverted) form. The enable input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs (1Y to 4Y) are forced LOW regardless of all other input conditions. Moving the data from two groups of registers to four common output buses is a common use of the "157". The state of the common data select input (S) determines the particular register from which the data comes. It can also be used as function generator.

The device is useful for implementing highly irregular logic by generating any four of the 16 different functions of two variables with one variable common.

The "157" is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S.

The "157" is identical to the "158" but has non-inverting (true) outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nI_0, nI_1 to nY $\overline{E}$ to nY S to nY	C_L = 50 pF V_{CC} = 3.3 V	 4.0 3.8 4.5	ns
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	30	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC157D	16	SO	plastic	SO16/SOT109A
74LVC157DB	16	SSOP	plastic	SSOP16/SOT338M
74LVC157PW	16	TSSOP	plastic	TSSOP16/SOT403

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	S	common data select input
2, 5, 11, 14	$1I_0$ to $4I_0$	data inputs from source 0
3, 6, 10, 13	$1I_1$ to $4I_1$	data inputs from source 1
4, 7, 9, 12	1Y to 4Y	multiplexer outputs
8	GND	ground (0 V)
15	$\overline{E}$	enable input (active LOW)
16	V_{CC}	positive supply voltage

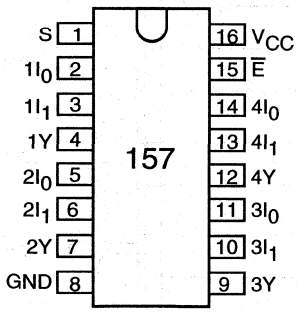


Fig.1 Pin configuration.

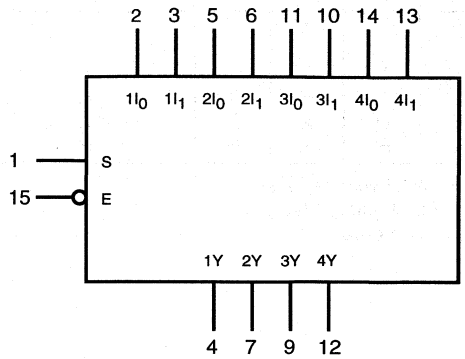


Fig.2 Logic symbol.

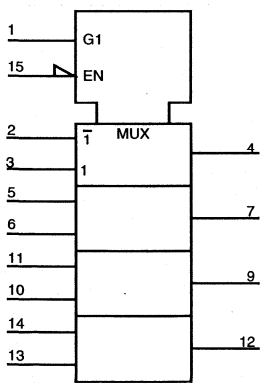


Fig.3 IEC Logic symbol.

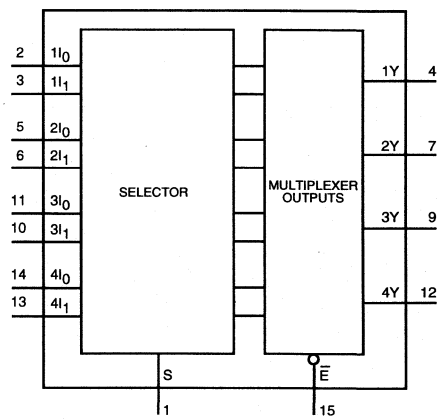


Fig.4 Functional diagram.

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{E}$	S	nI_0	nI_1	nY
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care

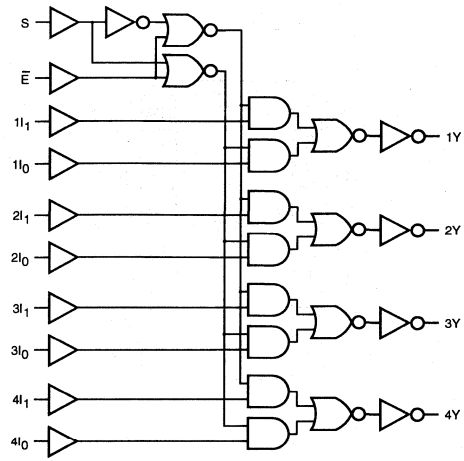


Fig.5 Logic diagram

DC CHARACTERISTICS FOR 74LVC157

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74LVC157

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C) −40 to +85			UNIT	TEST CONDITIONS	
		MIN.	TYP.	MAX.		V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay nI_0 to nY; nI_1 to nY	– – –	– 4.8 4.0*	– 8.0 7.0	ns	1.2 2.7 3.0 to 3.6	Fig.7
t_{PHL}/t_{PLH}	propagation delay $\overline{E}$ to nY	– – –	– 4.5 3.8*	– 8.0 7.0	ns	1.2 2.7 3.0 to 3.6	Fig.6
t_{PHL}/t_{PLH}	propagation delay S to nY	– – –	– 5.2 4.5*	– 9.0 8.0	ns	1.2 2.7 3.0 to 3.6	Fig.7

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

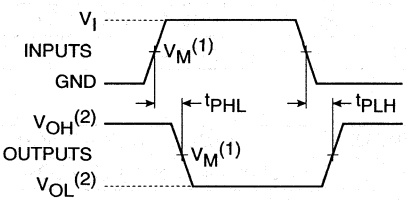


Fig. 6 Waveforms showing the enable input ($\overline{E}$) to output nY propagation delays.

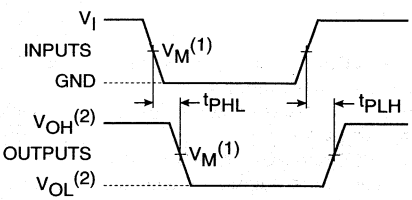


Fig. 7 Waveforms showing the data inputs (nI_0, nI_1) and common data select input (S) to output (nY) propagation delays.

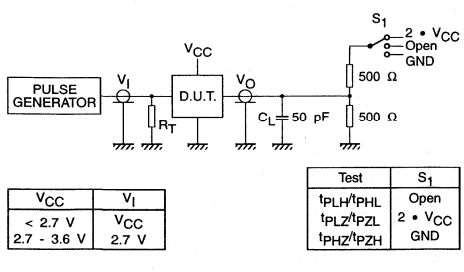


Fig.8 Load circuitry for switching times.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

Octal buffer/line driver; 3-state; inverting — 74LVC240

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **Inputs accept voltages upto 5.5 V**
- **CMOS low power consumption**
- **Direct interface with TTL levels**
- **Output drive capability 50 Ω transmission lines @ 85 °C**

DESCRIPTION

The 74LVC240 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment.

The 74LVC240 is an octal inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state. Schmitt-trigger action at all inputs makes the circuit highly tolerant for slower input rise and fall times. The '240' is identical to the '244' but has inverting outputs.

FUNCTION TABLE

INPUTS		OUTPUT
$n\overline{OE}$	nA_n	nY_n
L	L	H
L	H	L
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	C_L = 50 pF; V_{CC} = 3.3 V	4.6	ns
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	30	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC240D	20	SO	plastic	SO20/SOT163A
74LVC240DB	20	SSOP	plastic	SSOP20/SOT339
74LVC240PW	20	TSSOP	plastic	TSSOP20/SOT360

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	output enable input (active LOW)
2, 4, 6, 8	$1A_0$ to $1A_3$	data inputs
3, 5, 7, 9	$2Y_0$ to $2Y_3$	bus outputs
10	GND	ground (0 V)
17, 15, 13, 11	$2A_0$ to $2A_3$	data inputs
18, 16, 14, 12	$1Y_0$ to $1Y_3$	bus outputs
19	$2\overline{OE}$	output enable input (active LOW)
20	V_{CC}	positive power supply

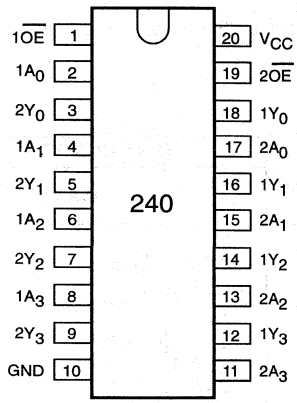


Fig.1 Pin configuration.

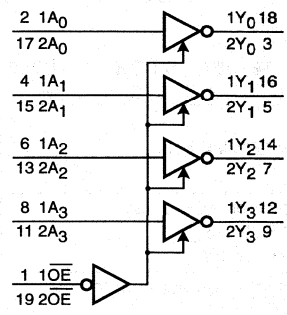


Fig.2 Logic symbol.

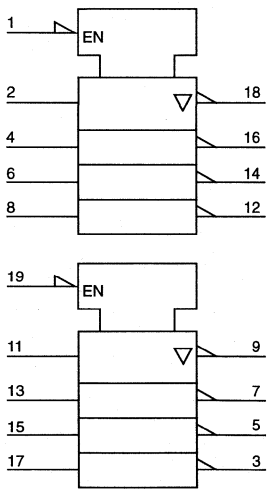


Fig.3 IEC logic symbol.

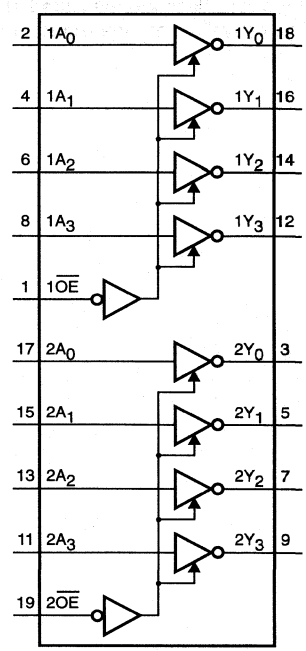


Fig.4 Functional diagram.

DC CHARACTERISTICS FOR 74LVC240

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LVC240

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C) -40 to +85			UNIT	TEST CONDITIONS	
		MIN.	TYP.	MAX.		V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay	–	21	–	ns	1.2	Fig. 5
	$1A_n$ to $1Y_n$;	1.5	4.8	9.0		2.7	
	$2A_n$ to $2Y_n$	1.5	4.6*	8.0		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time	–	42	–	ns	1.2	Figs 6, 7
	$1\overline{OE}$ to $1Y_n$;	1.5	6.3	9.5		2.7	
	$2\overline{OE}$ to $2Y_n$	1.5	6.0*	8.5		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time	–	6.5	–	ns	1.2	Figs 6, 7
	$1\overline{OE}$ to $1Y_n$;	1.5	3.4	9.0		2.7	
	$2\overline{OE}$ to $2Y_n$	1.5	3.3*	8.0		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

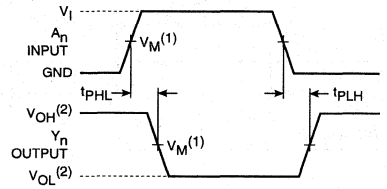


Fig.5 Waveforms showing the input ($1A_n$, $2A_n$) to output ($1Y_n$, $2Y_n$) propagation delays.

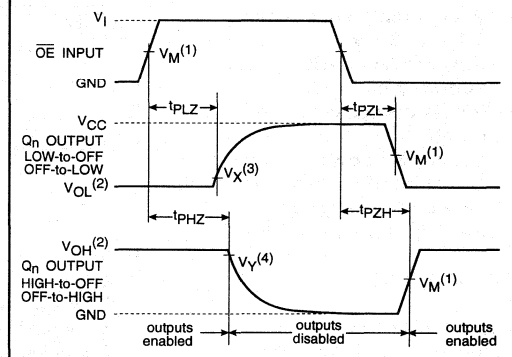
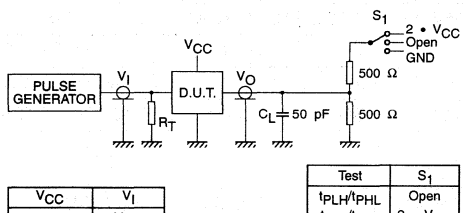


Fig.6 Waveforms showing the 3-state enable and disable times.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.7 Load circuitry for switching times.

Notes:

(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

Octal buffer/line driver; 3-state | 74LVC241

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **Inputs accept voltages up to 5.5 V**
- **CMOS low power consumption**
- **Direct interface with TTL levels**
- **Output drive capability 50 Ω transmission lines @ 85 °C**

DESCRIPTION

The 74LVC241 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment

The 74LVC241 is an octal non-inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $1\overline{OE}$ and 2OE. Schmitt-trigger action at all inputs makes the circuit highly tolerant for slower input rise and fall times.

FUNCTION TABLES

INPUTS		OUTPUT
$1\overline{OE}$	$1A_n$	$1Y_n$
L	L	L
L	H	H
H	X	Z

INPUTS		OUTPUT
2OE	$2A_n$	$2Y_n$
H	L	L
H	H	H
L	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	C_L = 50 pF V_{CC} = 3.3 V	4.8	ns
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	30	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC241D	20	SO	plastic	SO20/SOT163A
74LVC241DB	20	SSOP	plastic	SSOP20/SOT339
74LVC241PW	20	TSSOP	plastic	TSSOP20/SOT360

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	output enable input (active LOW)
2, 4, 6, 8	$1A_0$ to $1A_3$	data inputs
3, 5, 7, 9	$2Y_0$ to $2Y_3$	bus outputs
10	GND	ground (0 V)
17, 15, 13, 11	$2A_0$ to $2A_3$	data inputs
18, 16, 14, 12	$1Y_0$ to $1Y_3$	bus outputs
19	2OE	output enable input (active HIGH)
20	V_{CC}	positive power supply

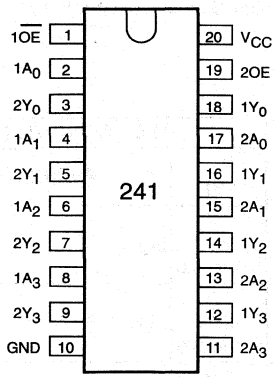


Fig.1 Pin configuration.

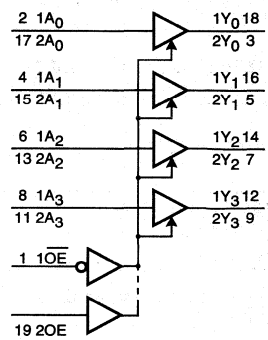


Fig.2 Logic symbol.

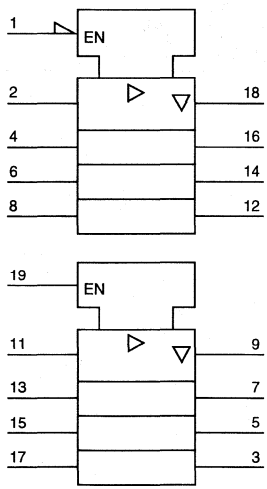


Fig.3 IEC logic symbol.

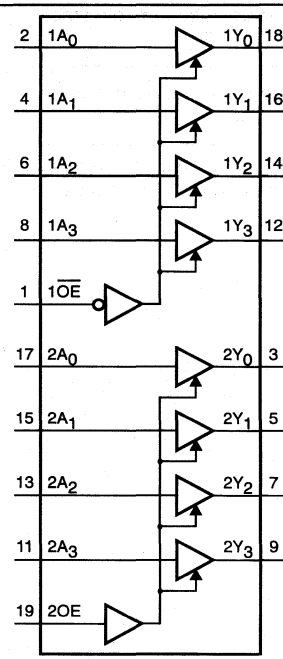


Fig.4 Functional diagram.

DC CHARACTERISTICS FOR 74LVC241

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LVC241

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C) -40 to +85			UNIT	TEST CONDITIONS	
		MIN.	TYP.	MAX.		V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	– 1.5 1.5	23 5.1 4.8*	– 7.7 7.3	ns	1.2 2.7 3.0 to 3.6	Fig.5
t_{PZH}/t_{PZL}	3-state output enable time $1\overline{OE}$ to $1Y_n$	– 1.5 1.5	48 5.9 5.6*	– 8.5 8.1	ns	1.2 2.7 3.0 to 3.6	Figs 6, 8
t_{PHZ}/t_{PLZ}	3-state output disable time $1\overline{OE}$ to 1Yn	– 1.5 1.5	5.8 3.8 3.6*	– 5.9 5.5	ns	1.2 2.7 3.0 to 3.6	Figs 6, 8
t_{PZH}/t_{PZL}	3-state output enable time $2\overline{OE}$ to $2Y_n$	– 1.5 1.5	42 5.9 5.6*	– 8.5 8.1	ns	1.2 2.7 3.0 to 3.6	Figs 7, 8
t_{PHZ}/t_{PLZ}	3-state output disable time $2\overline{OE}$ to $2Y_n$	– 1.5 1.5	7.5 3.8 3.6*	– 5.9 5.5	ns	1.2 2.7 3.0 to 3.6	Figs 7, 8

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

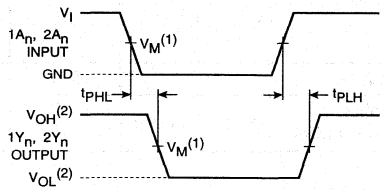


Fig. 5 Waveforms showing the input ($1A_n$, $2A_n$) to output ($1Y_n$, $2Y_n$) propagation delays.

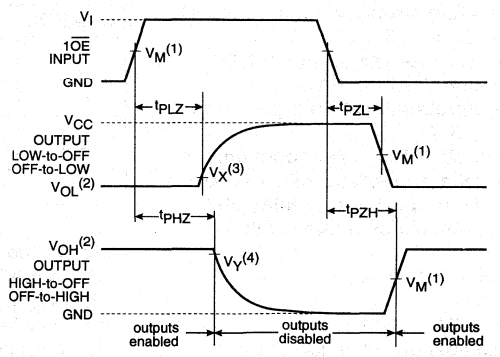


Fig.6 Waveforms showing the 3-state enable and disable times for input $1\overline{OE}$.

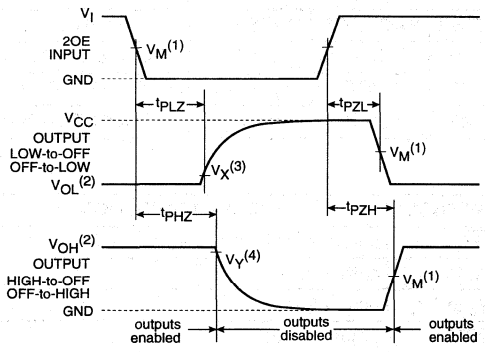
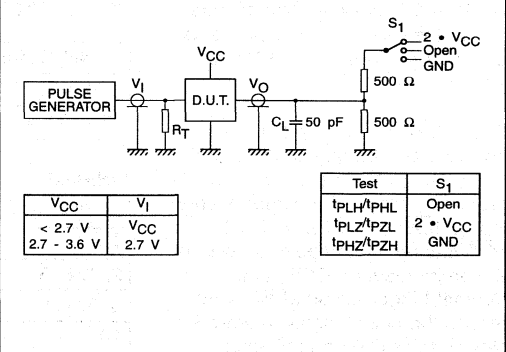


Fig.7 Waveforms showing the 3-state enable and disable times for input 2OE.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.8 Load circuitry for switching times

Notes:

(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

Octal buffer/line driver; 3-state | 74LVC244

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **Inputs accept voltages up to 5.5 V**
- **CMOS low power consumption**
- **Direct interface with TTL levels**
- **Output drive capability 50 Ω transmission lines @ 85 °C**

DESCRIPTION

The 74LVC244 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment

The 74LVC244 is an octal non-inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state. Schmitt-trigger action at all inputs makes the circuit highly tolerant for slower input rise and fall times. The '244' is identical to the '240' but has non-inverting outputs.

FUNCTION TABLE

INPUTS		OUTPUT
$n\overline{OE}$	nA_n	nY_n
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	C_L = 50 pF V_{CC} = 3.3 V	4.9	ns
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	30	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC244D	20	SO	plastic	SO20/SOT163A
74LVC244DB	20	SSOP	plastic	SSOP20/SOT339
74LVC244PW	20	TSSOP	plastic	TSSOP20/SOT360

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	output enable input (active LOW)
2, 4, 6, 8	$1A_0$ to $1A_3$	data inputs
3, 5, 7, 9	$2Y_0$ to $2Y_3$	bus outputs
10	GND	ground (0 V)
17, 15, 13, 11	$2A_0$ to $2A_3$	data inputs
18, 16, 14, 12	$1Y_0$ to $1Y_3$	bus outputs
19	$2\overline{OE}$	output enable input (active LOW)
20	V_{CC}	positive power supply

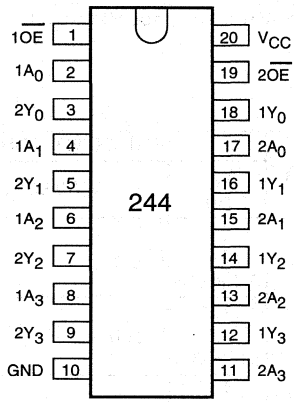


Fig.1 Pin configuration.

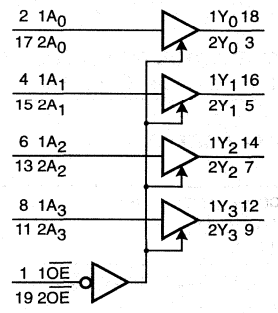


Fig.2 Logic symbol.

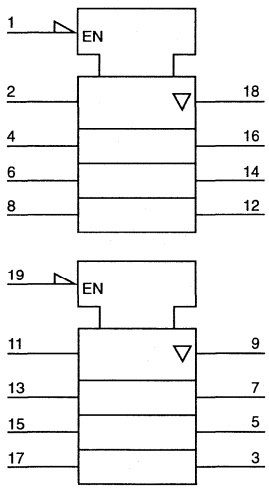


Fig.3 IEC logic symbol.

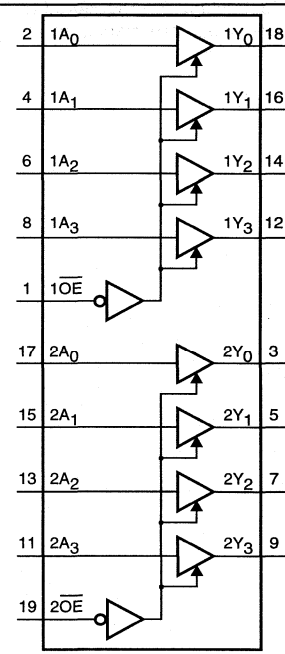


Fig.4 Functional diagram.

DC CHARACTERISTICS FOR 74LVC244

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LVC244

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C) -40 to +85			UNIT	TEST CONDITIONS	
		MIN.	TYP.	MAX.		V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay	–	21	–	ns	1.2	Fig. 5
	$1A_n$ to $1Y_n$;	1.5	5.2	8.0		2.7	
	$2A_n$ to $2Y_n$	1.5	4.9*	7.0		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time	–	45	–	ns	1.2	Figs 6, 7
	$1\overline{OE}$ to $1Y_n$;	1.5	6.1	10.0		2.7	
	$2\overline{OE}$ to $2Y_n$	1.5	5.8*	8.0		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time	–	5.8	–	ns	1.2	Figs 6, 7
	$1\overline{OE}$ to $1Y_n$;	1.5	3.5	8.5		2.7	
	$2\overline{OE}$ to $2Y_n$	1.5	3.3*	7.5		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

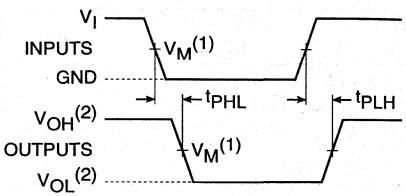


Fig.5 Waveforms showing the input ($1A_n$, $2A_n$) to output ($1Y_n$, $2Y_n$) propagation delays.

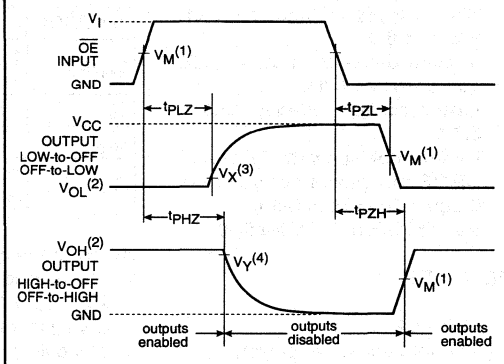
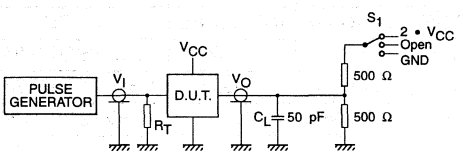


Fig.6 Waveforms showing the 3-state enable and disable times.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.7 Load circuitry for switching times.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

Octal bus transceiver with direction pin; 3-state — 74LVC245

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with the JEDEC standard no. 8-1A.**
- **Inputs accept voltages upto 5.5 V**
- **Direct interface with TTL levels**
- **CMOS low power consumption**
- **Output drive capability 50 Ω transmission lines @ 85 °C**

DESCRIPTION

The 74LVC245 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74LVC245 is an octal transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The '245' features an output enable ($\overline{OE}$) input for easy cascading and a send/receive (DIR) input for direction control. $\overline{OE}$ controls the outputs so that the buses are effectively isolated.
The '245' is identical to the '640' but has true (non-inverting) outputs.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUT	
$\overline{OE}$	DIR	A_n	B_n
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n	C_L = 50 pF V_{CC} = 3.3 V	4.1	ns
C_I	input capacitance		5.0	pF
$C_{I/O}$	input/output capacitance		10	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	40	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC245D	20	SO	plastic	SO20/SOT163A
74LVC245DB	20	SSOP	plastic	SSOP20/SOT339
74LVC245PW	20	TSSOP	plastic	TSSOP20/SOT360

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	DIR	direction control
2, 3, 4, 5, 6, 7, 8, 9	A_0 to A_7	data inputs/outputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	B_0 to B_7	data inputs/outputs
19	$\overline{OE}$	output enable input (active LOW)
20	V_{CC}	positive supply voltage

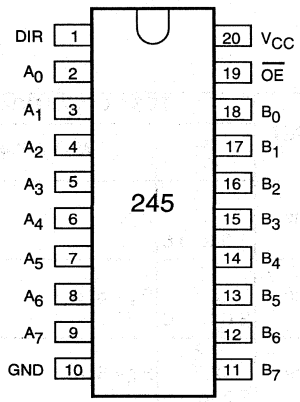


Fig.1 Pin configuration.

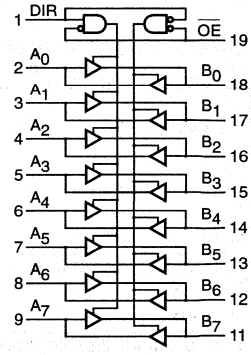


Fig.2 Logic symbol.

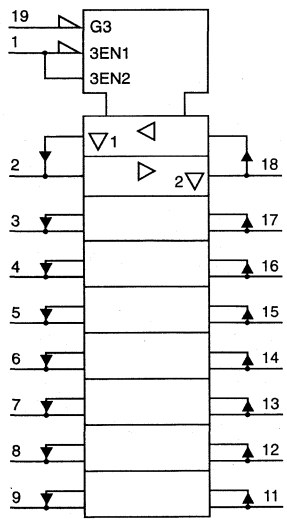


Fig.3 IEC logic symbol.

DC CHARACTERISTICS FOR 74LVC245

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LVC245

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C) -40 to +85			UNIT	TEST CONDITIONS	
		MIN.	TYP.	MAX.		V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay	–	21	–	ns	1.2	Fig. 4
	A_n to B_n;	1.5	4.6	8.0		2.7	
	B_n to A_n	1.5	4.1*	7.0		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time	–	25	–	ns	1.2	Figs 5, 6
	$\overline{OE}$ to A_n;	1.5	5.3	10.0		2.7	
	$\overline{OE}$ to B_n	1.5	4.5*	9.0		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time	–	8.0	–	ns	1.2	Figs 5, 6
	$\overline{OE}$ to A_n;	1.5	4.3	9.0		2.7	
	$\overline{OE}$ to B_n	1.5	4.0*	8.0		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

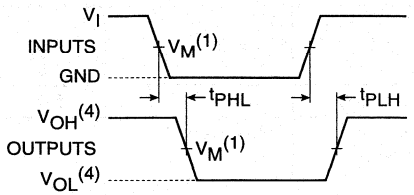


Fig. 4 Waveforms showing the input (A_n, B_n) to output (B_n, A_n) propagation delays.

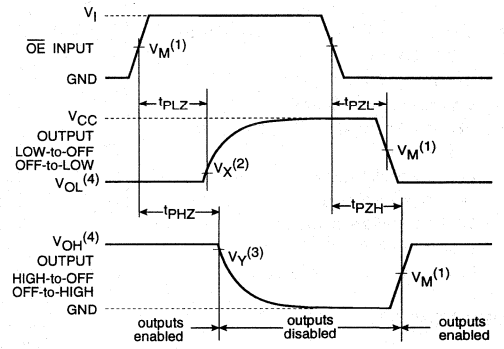
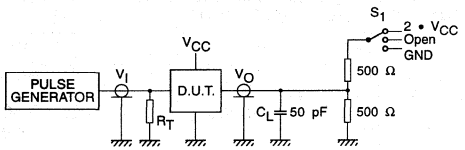


Fig.5 Waveforms showing the 3-state enable and disable times.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.6 Load circuitry for switching times.

Notes:

(1) V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
V_M = 0.5 · V_{CC} at V_{CC} < 2.7 V

(2) $V_X = V_{OL}$ + 0.3 V at $V_{CC} \geq$ 2.7 V
$V_X = V_{OL}$ + 0.1 · V_{CC} at V_{CC} < 2.7 V

(3) $V_Y = V_{OH}$ – 0.3 V at $V_{CC} \geq$ 2.7 V
$V_Y = V_{OH}$ – 0.1 · V_{CC} at V_{CC} < 2.7 V

(4) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **Inputs accept voltages upto 5.5 V**
- **CMOS low power consumption**
- **Direct interface with TTL levels**
- **Output drive capability 50 Ω transmission lines @ 85 °C**
- **Non-inverting data path**

DESCRIPTION

The 74LVC257 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74LVC257 is a quad 2-input multiplexer with 3-state outputs, which select 4 bits of data from two sources under the control of a common data select input (S). The data inputs from source 0 ($1I_0$ to $4I_0$) are selected when input S is LOW and the data inputs from source 1 ($1I_1$ to $4I_1$) are selected when S is HIGH. Data appears at the outputs (1Y to 4Y) in true (non-inverting) form from the selected inputs. The "257" is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S.
The outputs are forced to a high impedance OFF-state when $\overline{OE}$ is HIGH.

The logic equations for the outputs are:
$1Y = \overline{OE} \cdot (1I_1 \cdot S + 1I_0 \cdot \overline{S})$
$2Y = \overline{OE} \cdot (2I_1 \cdot S + 2I_0 \cdot \overline{S})$
$3Y = \overline{OE} \cdot (3I_1 \cdot S + 3I_0 \cdot \overline{S})$
$4Y = \overline{OE} \cdot (4I_1 \cdot S + 4I_0 \cdot \overline{S})$

The "257" is identical to the "258" but has non-inverting (true) outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nI_0, nI_1 to nY S to nY	C_L = 50 pF V_{CC} = 3.3 V	4.0 4.5	ns
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	30	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC257D	16	SO	plastic	SO16/SOT109A
74LVC257DB	16	SSOP	plastic	SSOP16/SOT338M
74LVC257PW	16	TSSOP	plastic	TSSOP16/SOT403

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	S	common data select input
2, 5, 11, 14	$1I_0$ to $4I_0$	data inputs from source 0
3, 6, 10, 13	$1I_1$ to $4I_1$	data inputs from source 1
4, 7, 9, 12	1Y to 4Y	3-state multiplexer outputs
8	GND	ground (0 V)
15	$\overline{OE}$	3-state output enable input (active LOW)
16	V_{CC}	positive supply voltage

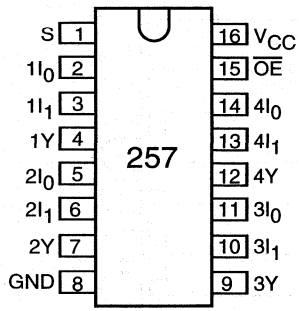


Fig.1 Pin configuration.

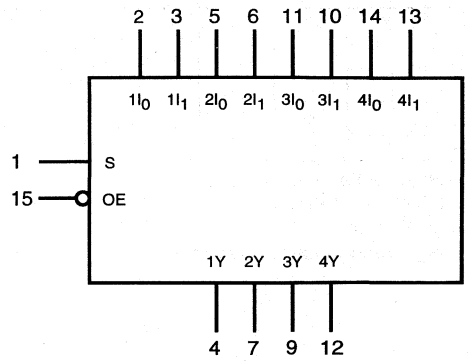


Fig.2 Logic symbol.

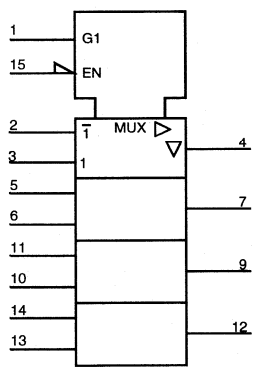


Fig.3 IEC Logic symbol.

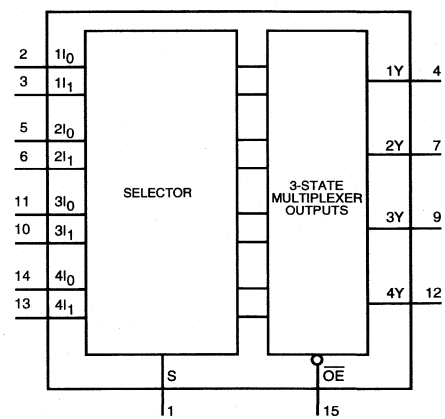


Fig.4 Functional diagram.

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	S	nI_0	nI_1	nY
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = high impedance OFF-state

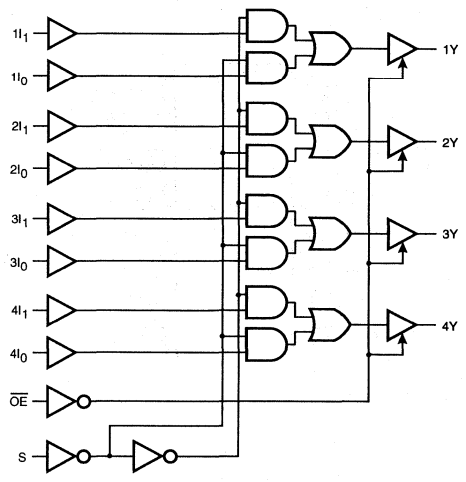


Fig.5 Logic diagram

DC CHARACTERISTICS FOR 74LVC257

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74LVC257

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C) −40 to +85			UNIT	TEST CONDITIONS	
		MIN.	TYP.	MAX.		V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay nI_0 to nY; nI_1 to nY	– – –	– 4.8 4.0*	– 8.0 7.0	ns	1.2 2.7 3.0 to 3.6	Fig.6
t_{PHL}/t_{PLH}	propagation delay S to nY	– – –	– 5.2 4.5*	– 10.5 9.5	ns	1.2 2.7 3.0 to 3.6	Fig.6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to nY	– – –	– 5.2 4.5*	– 9.0 8.0	ns	1.2 2.7 3.0 to 3.6	Fig.7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to nY	– – –	– 4.0 3.8*	– 7.0 6.0	ns	1.2 2.7 3.0 to 3.6	Fig.7

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

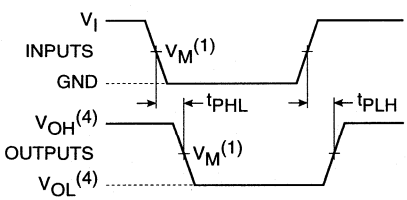


Fig. 6 Waveforms showing the input (S, nI_0, nI_1) to output (nY) propagation delays.

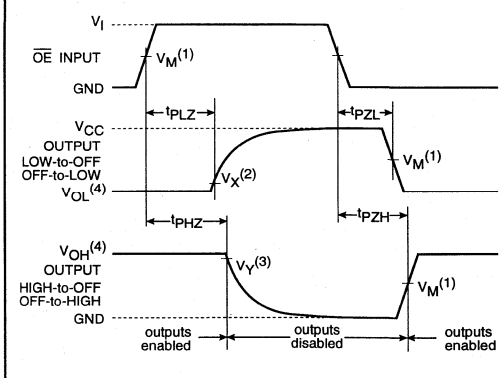
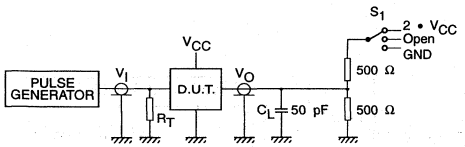


Fig. 7 Waveforms showing the 3-state enable and disable times.

Notes:
(1) $V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
$V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
(2) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
(3) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
(4) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig. 8 Load circuitry for switching times.

Octal D-type transparent latch; 3-state 74LVC373

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **Inputs accept voltages upto 5.5 V**
- **CMOS low power consumption**
- **Direct interface with TTL levels**
- **Common 3-state output enable input**
- **Output drive capability 50 Ω transmission lines @ 85 °C**

DESCRIPTION

The 74LVC373 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment.

The 74LVC373 is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. A latch enable (LE) input and an output enable ($\overline{OE}$) input are common to all internal latches.

The '373' consists of eight D-type transparent latches with 3-state true outputs. When LE is HIGH, data at the D_n inputs enters the latches. In this condition the latches are transparent, i.e. a latch output will change each time its corresponding D-input changes. When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the eight latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches. The '373' is functionally identical to the '573', but the '573' has different pin arrangement.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n; LE to Q_n	C_L = 50 pF V_{CC} = 3.3 V	4.3 4.6	ns
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	23	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC373D	20	SO	plastic	SO20/SOT163A
74LVC373DB	20	SSOP	plastic	SSOP20/SOT339
74LVC373PW	20	TSSOP	plastic	TSSOP20/SOT360

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	output enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q_0 to Q_7	3-state latch outputs
3, 4, 7, 8, 13, 14, 17, 18	D_0 to D_7	data inputs
10	GND	ground (0 V)
11	LE	latch enable input (active HIGH)
20	V_{CC}	positive supply voltage

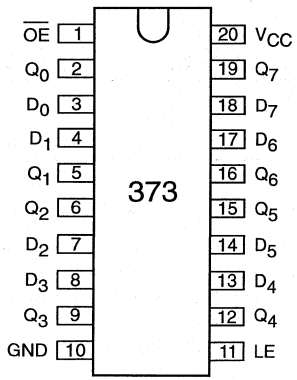


Fig.1 Pin configuration.

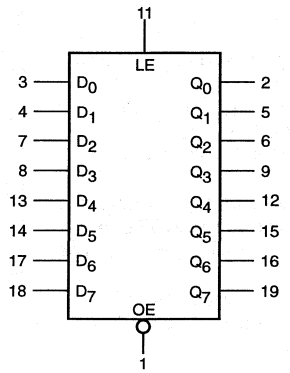


Fig.2 Logic symbol.

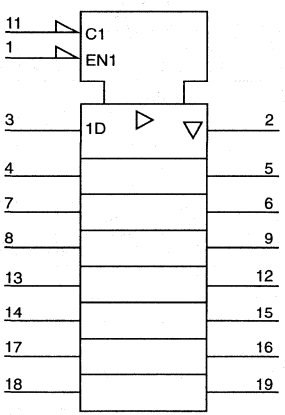


Fig3. IEC logic symbol.

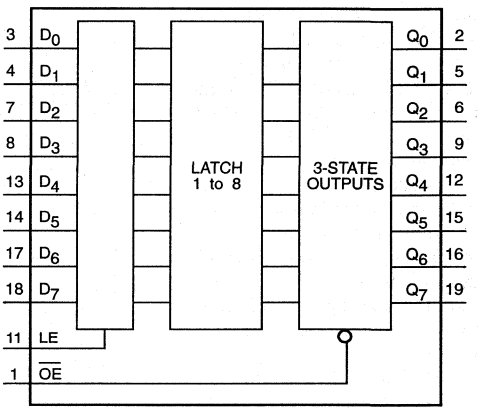


Fig.4 Functional diagram.

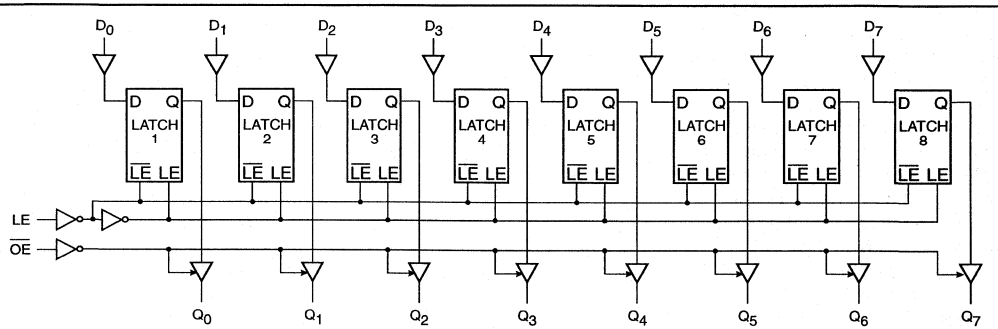


Fig.5 Logic diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$\overline{OE}$	LE	D_n		Q_0 to Q_7
enable and read register (transparent mode)	L L	H H	L H	L H	L H
latch and read register	L L	L L	l h	L H	L H
latch register and disable outputs	H H	L L	l h	L H	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
X = don't care
Z = high impedance OFF-state

DC CHARACTERISTICS FOR 74LVC373

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74LVC373

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		–40 to +85				V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n	– 1.5 1.5	21 4.7 4.3*	– 8.0 7.8	ns	1.2 2.7 3.0 to 3.6	Fig.6
t_{PHL}/t_{PLH}	propagation delay LE to Q_n	– 1.5 1.5	23 5.3 4.6*	– 10 8.5	ns	1.2 2.7 3.0 to 3.6	Fig.7
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n	– 1.5 1.5	17 4.4 3.8*	– 8.0 7.5	ns	1.2 2.7 3.0 to 3.6	Fig.8
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n	– 1.5 1.5	8.0 4.0 3.5*	– 6.5 6.0	ns	1.2 2.7 3.0 to 3.6	Fig.8
t_W	LE pulse width HIGH	– –	3.0 3.0*	– –	ns	2.7 3.0 to 3.6	Fig.7
t_{su}	set-up time D_n to LE	1.0 1.0	0.5 0.4*	– –	ns	2.7 3.0 to 3.6	Fig.9
t_h	hold time D_n to LE	1.0 1.0	0 0*	– –	ns	2.7 3.0 to 3.6	Fig.9

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

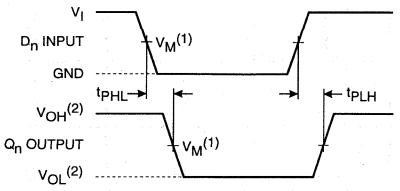


Fig.6 Waveforms showing the input (D_n) to output (Q_n) propagation delays.

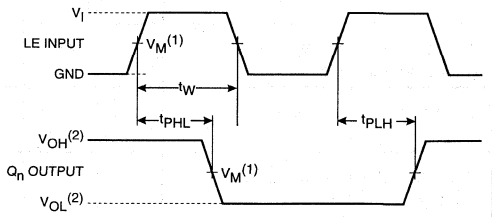


Fig.7 Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output (Q_n) propagation delays.

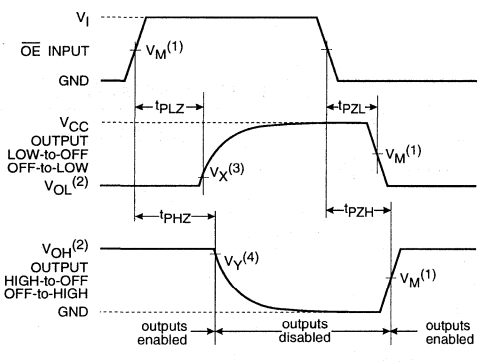


Fig.8 Waveforms showing the 3-state enable and disable times

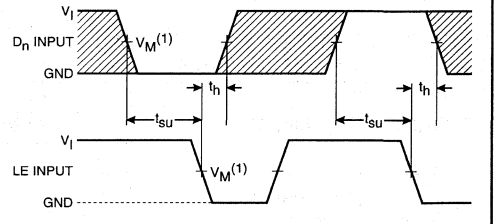
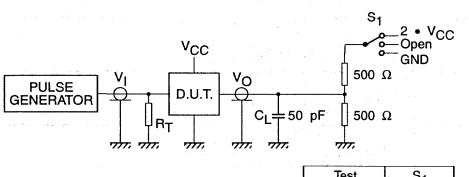


Fig.9 Waveforms showing the data set-up and hold times for the D_n input to the LE input.

Note to Fig.9:

The shaded areas indicate when the input is permitted to change for predictable output performance.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.10 Load circuitry for switching times.

Notes:

(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

Octal D-type flip-flop; positive-edge trigger; 3-state 74LVC374

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **Inputs accept voltages upto 5.5 V**
- **CMOS low power consumption**
- **Direct interface with TTL levels**
- **8-bit positive edge-triggered register**
- **Independent register and 3-state buffer operation**
- **Output drive capability 50 Ω transmission lines @ 85 °C**

DESCRIPTION

The 74LVC374 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment.

The 74LVC374 is an octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A clock (CP) and an output enable ($\overline{OE}$) input are common to all flip-flops.

The eight flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition.

When $\overline{OE}$ is LOW, the contents of the eight flip-flops is available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops. The '374' is functionally identical to the '574', but the '574' has a different pin arrangement.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 50 pF; V_{CC} = 3.3 V	4.8	ns
f_{max}	maximum clock frequency		150	MHz
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	28	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC374D	20	SO	plastic	SO20/SOT163A
74LVC374DB	20	SSOP	plastic	SSOP20/SOT339
74LVC374PW	20	TSSOP	plastic	TSSOP/SOT360

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	output enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q_0 to Q_7	3-state flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	D_0 to D_7	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
20	V_{CC}	positive supply voltage

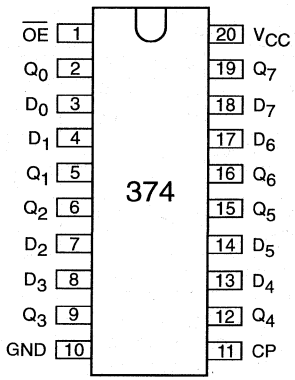


Fig.1 Pin configuration.

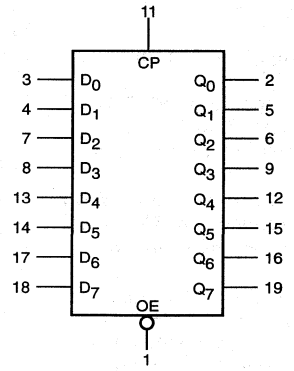


Fig.2 Logic symbol.

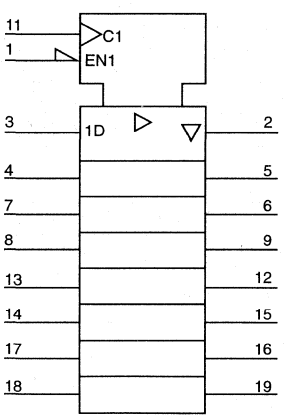


Fig3. IEC logic symbol.

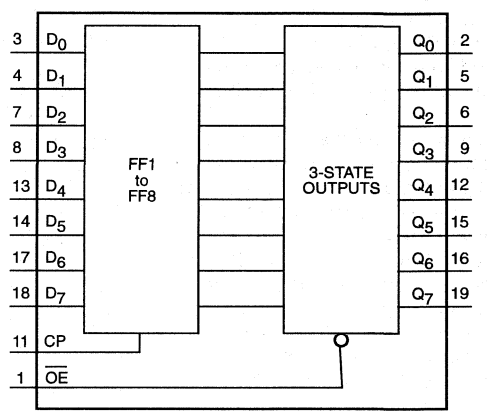


Fig.4 Functional diagram.

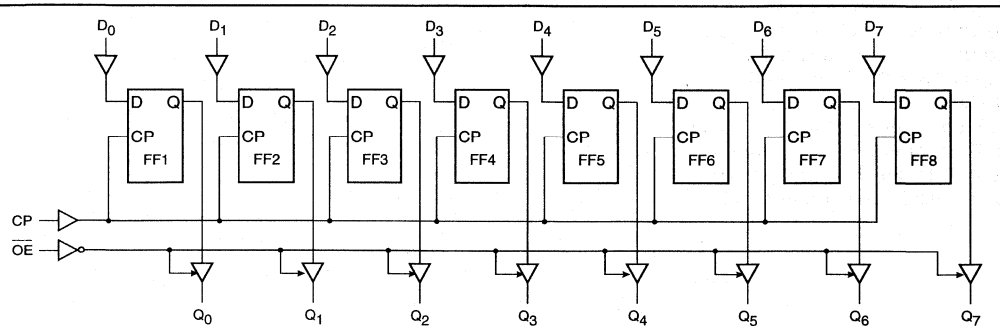


Fig.5 Logic diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	CP	D_n		Q_0 to Q_7
load and read register	L L	↑ ↑	l h	L H	L H
load register and disable outputs	H H	↑ ↑	l h	L H	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
Z = high impedance OFF-state
↑ = LOW-to-HIGH clock transition

DC CHARACTERISTICS FOR 74LVC374

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74LVC374

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		−40 to +85				V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	– 1.5 1.5	21 5.2 4.8*	– 9.5 8.5	ns	1.2 2.7 3.0 to 3.6	Fig.6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n	– 1.5 1.5	17 4.4 4.0*	– 8.0 7.5	ns	1.2 2.7 3.0 to 3.6	Fig.7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n	– 1.5 1.5	8.0 3.6 3.5*	– 6.5 6.0	ns	1.2 2.7 3.0 to 3.6	Fig.7
t_W	clock pulse width HIGH or LOW	– –	3.0 3.0*	– –	ns	2.7 3.0 to 3.6	Fig.6
t_{su}	set-up time D_n to CP	– –	0.5 0.4*	– –	ns	2.7 3.0 to 3.6	Fig.8
t_h	hold time D_n to CP	1.0 1.0	−0.5 −0.4*	– –	ns	2.7 3.0 to 3.6	Fig.8
f_{max}	maximum clock pulse frequency	– 75	– 150*	– –	MHz	2.7 3.0 to 3.6	Fig.6

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

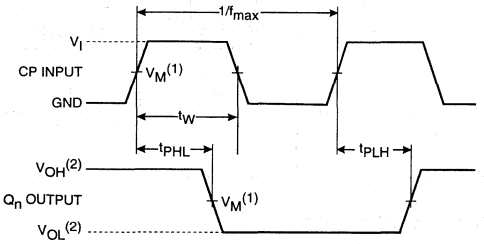


Fig.6 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width and the maximum clock pulse frequency.

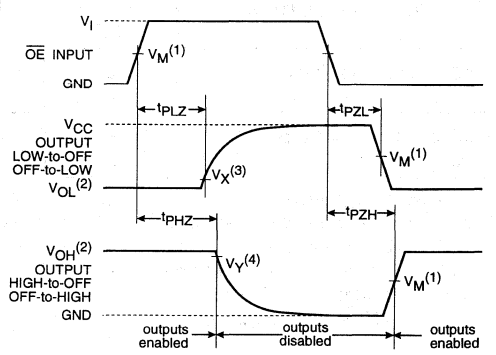


Fig.7 Waveforms showing the 3-state enable and disable times.

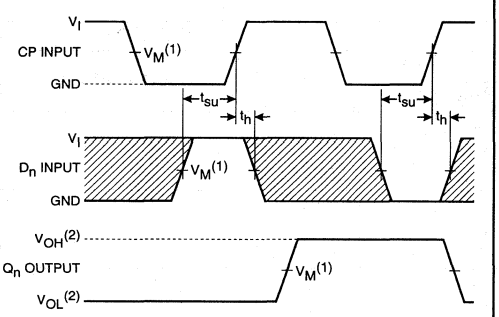
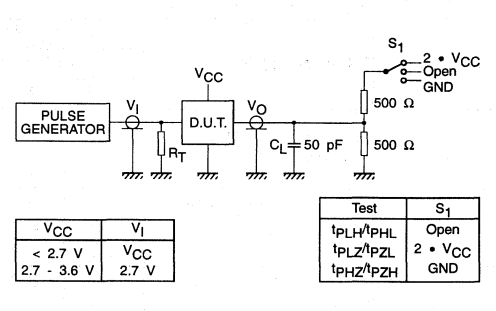


Fig.8 Waveforms showing the data set-up and hold times for the D_n input to the CP input.

Note to Fig.8:

The shaded areas indicate when the input is permitted to change for predictable output performance.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.9 Load circuitry for switching times.

Notes:

(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

Octal registered transceiver; 3-state | 74LVC543

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **CMOS low power consumption**
- **Direct interface with TTL levels**
- **Combines 74LVC245 and 74LVC373 type functions in one chip**
- **Octal transceiver with D-type latch**
- **Back-to-back registers for storage**
- **Seperate controls for data flow in each direction**
- **3-state non-inverting outputs for bus oriented applications**

DESCRIPTION

The 74LVC543 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74LVC543 is an octal registered transceiver containing two sets of D-type latches for temporary storage of the data flow in either direction. Seperate latch enable ($\overline{LEAB}$, $\overline{LEBA}$) and output enable ($\overline{OEAB}$, $\overline{OEBA}$) inputs are provided for each register to permit independent control of inputting and outputting in either direction of the data flow.
The '543 contains eight D-type latches, with seperate inputs and controls for each set. For data flow from A to B, for example, the A-to-B enable ($\overline{EAB}$) input must be LOW in order to enter data from A_0-A_7 or take data from B_0-B_7, as indicated in the function table. With $\overline{EAB}$ LOW, a LOW signal on the A-to-B latch enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With $\overline{EAB}$ and $\overline{OEAB}$ both low, the 3-State B output buffers are active and display the data present at the outputs of the A latches.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n to B_n	C_L = 50 pF V_{CC} = 3.3 V	5.4	ns
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	33	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC543D	24	SO	plastic	SO24/SOT137A
74LVC543DB	24	SSOP	plastic	SSOP24/SOT340
74LVC543PW	24	TSSOP	plastic	TSSOP20/SOT360

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	$\overline{LEBA}$	'B' to 'A' latch enable input (active low)
2	$\overline{OEBA}$	'B' to 'A' output enable input (active low)
3, 4, 5, 6, 7, 8, 9, 10	A_0 to A_7	'A' data inputs/outputs
11	$\overline{EAB}$	'B' to 'A' enable input (active low)
12	GND	ground (0 V)
22, 21, 20, 19, 18, 17, 16, 15	B_0 to B_7	'B' data inputs/outputs
13	$\overline{OEAB}$	'A' to 'B' output enable input (active low)
14	$\overline{LEAB}$	'A' to 'B' latch enable input (active low)
23	$\overline{EBA}$	'A' to 'B' enable input (active low)
24	V_{CC}	positive supply voltage

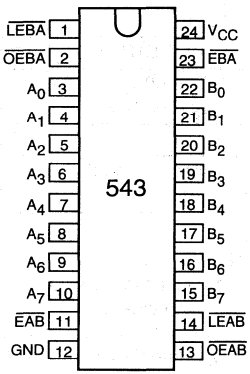


Fig.1 Pin configuration.

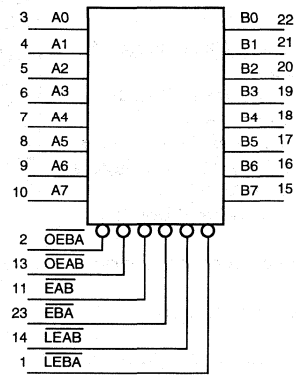


Fig.2 Logic symbol.

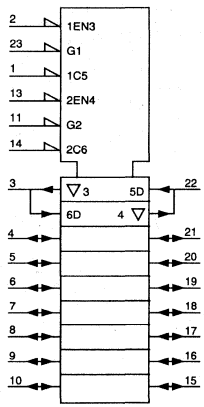


Fig3. IEC logic symbol.

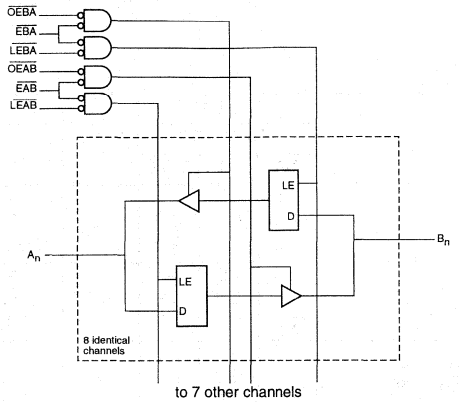


Fig.4 Logic diagram

FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
$\overline{OEXX}$	$\overline{EXX}$	$\overline{LEXX}$	DATA		
H	X	X	X	Z	Disabled
X	H	X	X	Z	Disables
L L	↑ ↑	L L	h l	Z Z	Disabled + Latch
L L	L L	↑ ↑	h l	H L	Latch + Display
L L	L L	L L	H L	H L	Transparent
L	L	H	X	NC	Hold

XX = AB for A-to-B direction, BA for B-to-A direction
H = HIGH voltage level
L = LOW voltage level
h = High state must be present one setup time before the low-to-high transition of $\overline{LEAB}$, $\overline{LEBA}$, $\overline{EAB}$ or $\overline{EBA}$
l = Low state must be present one setup time before the low-to-high transition of $\overline{LEAB}$, $\overline{LEBA}$, $\overline{EAB}$ or $\overline{EBA}$
X = Don't care
↑ = LOW-to-HIGH level transition
NC = No change
Z = High impedance "off" state

DC CHARACTERISTICS FOR 74LVC543

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LVC543

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		-40 to +85				V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t_{PHL}/t_{PLH}	propagation delay A_n to B_n, B_n to A_n	1.5 1.5 1.5	23 6.1 5.4*	– 9.6 9.0	ns	1.2 2.7 3.0 to 3.6	Fig.5
t_{PHL}/t_{PLH}	propagation delay $\overline{LEBA}$ to A_n, $\overline{LEAB}$ to B_n	1.5 1.5 1.5	26 6.8 6.0*	– 11 10	ns	1.2 2.7 3.0 to 3.6	Fig.6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OEBA}$ to A_n, $\overline{OEAB}$ to B_n	1.5 1.5 1.5	– 6.2 5.5*	– 9.7 9.1	ns	1.2 2.7 3.0 to 3.6	Fig.7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OEBA}$ to A_n, $\overline{OEAB}$ to B_n	1.5 1.5 1.5	– 5.2 4.5*	– 7.5 7.0	ns	1.2 2.7 3.0 to 3.6	Fig.7
t_{PZH}/t_{PZL}	3-state output enable time $\overline{EBA}$ to A_n, $\overline{EAB}$ to B_n	1.5 1.5 1.5	– 6.5 5.7*	– 10 9.5	ns	1.2 2.7 3.0 to 3.6	Fig.7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{EBA}$ to A_n, $\overline{EAB}$ to B_n	1.5 1.5 1.5	– 5.2 4.5*	– 7.5 7.0	ns	1.2 2.7 3.0 to 3.6	Fig.7

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		-40 to +85				V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t_W	LE pulse width LOW	4.0 4.0	– –	– –	ns	2.7 3.0 to 3.6	Fig.6
t_{su}	set-up time A_n/B_n to $\overline{LEXX}$, A_n/B_n to $\overline{EXX}$	– 1.5 1.5	– – –	– – –	ns	1.2 2.7 3.0 to 3.6	Fig.8
t_h	hold time A_n/B_n to $\overline{LEXX}$, A_n/B_n to $\overline{EXX}$	– 2.5 2.5	– – –	– – –	ns	1.2 2.7 3.0 to 3.6	Fig.8

Notes: All typical values are measured at T_{amb} = 25 °C.
* Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

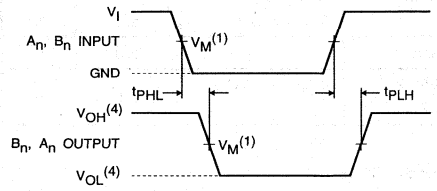


Fig.5 Waveforms showing the input (A_n, B_n) to output (B_n, A_n) propagation delays.

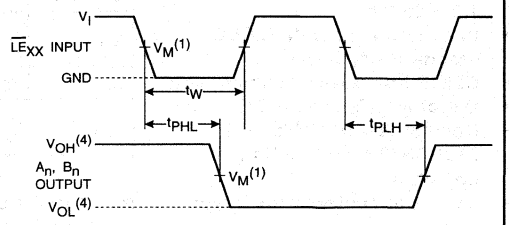


Fig.6 Waveforms showing the latch enable input ($\overline{LEXX}$) pulse width, the latch enable input to output (A_n, B_n) propagation delays.

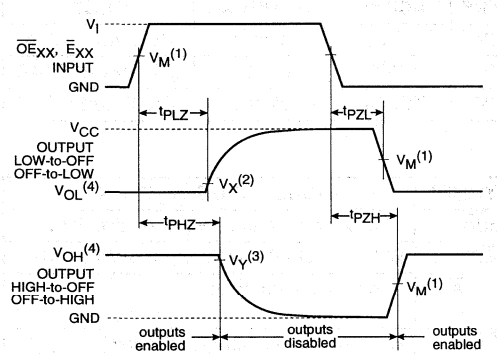


Fig.7 Waveforms showing the 3-state enable and disable times

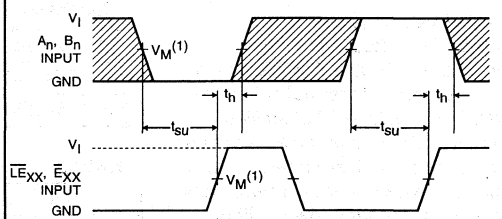
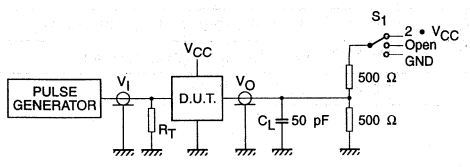


Fig.8 Waveforms showing the data set-up and hold times for the (A_n, B_n) input to the $\overline{LEXX}$ and $\overline{EXX}$ input.

Note to Fig.8:

The shaded areas indicate when the input is permitted to change for predictable output performance.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.9 Load circuitry for switching times.

Notes:

(1) V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
V_M = 0.5 · V_{CC} at V_{CC} < 2.7 V

(2) $V_X = V_{OL}$ + 0.3 V at $V_{CC} \geq$ 2.7 V
$V_X = V_{OL}$ +0.1 · V_{CC} at V_{CC} < 2.7 V

(3) $V_Y = V_{OH}$ – 0.3 V at $V_{CC} \geq$ 2.7 V
$V_Y = V_{OH}$ –0.1 · V_{CC} at V_{CC} < 2.7 V

(4) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **CMOS low power consumption**
- **Direct interface with TTL levels**
- **Combines 74LVC640 and 74LVC533 type functions in one chip**
- **Octal transceiver with D-type latch**
- **Back-to-back registers for storage**
- **Seperate controls for data flow in each direction**
- **3-state inverting outputs for bus oriented applications**

DESCRIPTION

The 74LVC544 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.
The 74LVC544 is an octal registered inverting transceiver containing two sets of D-type latches for temporary storage of the data flow in either direction. Seperate latch enable ($\overline{LEAB}$, $\overline{LEBA}$) and output enable ($\overline{OEAB}$, $\overline{OEBA}$) inputs are provided for each register to permit independent control of inputting and outputting in either direction of the data flow.
The '544 contains eight D-type latches, with seperate inputs and controls for each set. For data flow from A to B, for example, the A-to-B enable ($\overline{EAB}$) input must be LOW in order to enter data from $\overline{A}_0$-$\overline{A}_7$ or take data from $\overline{B}_0$-$\overline{B}_7$, as indicated in the function table. With $\overline{EAB}$ LOW, a LOW signal on the A-to-B latch enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With $\overline{EAB}$ and $\overline{OEAB}$ both low, the 3-State B output buffers are active and display the data present at the outputs of the A latches.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay $\overline{A}_n$ to $\overline{B}_n$	C_L = 50 pF V_{CC} = 3.3 V	5.1	ns
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	34	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC544D	24	SO	plastic	SO24/SOT137A
74LVC544DB	24	SSOP	plastic	SSOP24/SOT340
74LVC544PW	24	TSSOP	plastic	TSSOP20/SOT360

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	$\overline{LEBA}$	'B' to 'A' latch enable input (active low)
2	$\overline{OEBA}$	'B' to 'A' output enable input (active low)
3, 4, 5, 6, 7, 8, 9, 10	$\overline{A}_0$ to $\overline{A}_7$	'$\overline{A}$' data inputs/outputs
11	$\overline{EBA}$	'B' to 'A' enable input (active low)
12	GND	ground (0 V)
22, 21, 20, 19, 18, 17, 16, 15	$\overline{B}_0$ to $\overline{B}_7$	'$\overline{B}$' data inputs/outputs
13	$\overline{OEAB}$	'A' to 'B' output enable input (active low)
14	$\overline{LEAB}$	'A' to 'B' latch enable input (active low)
23	$\overline{EAB}$	'A' to 'B' enable input (active low)
24	V_{CC}	positive supply voltage

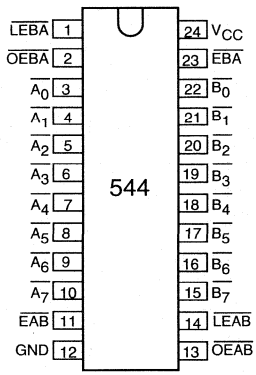


Fig.1 Pin configuration.

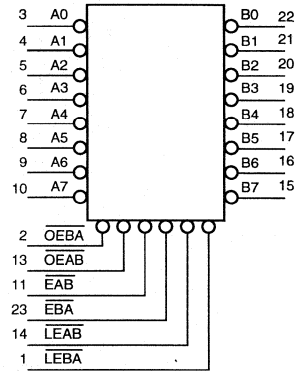


Fig.2 Logic symbol.

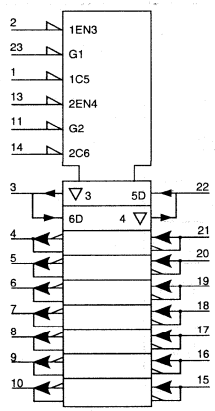


Fig3. IEC logic symbol.

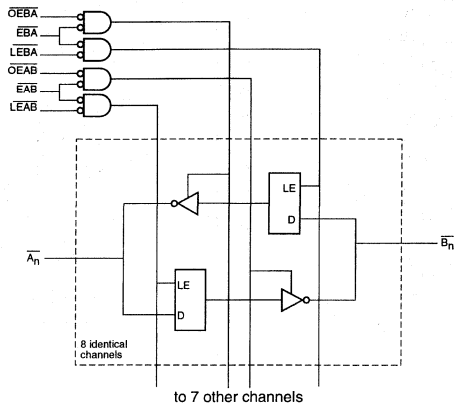


Fig.4 Logic diagram

FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
$\overline{OEXX}$	$\overline{EXX}$	$\overline{LEXX}$	DATA		
H	X	X	X	Z	Disabled
X	H	X	X	Z	Disables
L L	↑ ↑	L L	h l	Z Z	Disabled + Latch
L L	L L	↑ ↑	h l	L H	Latch + Display
L L	L L	L L	H L	L H	Transparent
L	L	H	X	NC	Hold

XX = AB for A-to-B direction, BA for B-to-A direction
H = HIGH voltage level
L = LOW voltage level
h = High state must be present one setup time before the low-to-high transition of $\overline{LEAB}$, $\overline{LEBA}$, $\overline{EAB}$ or $\overline{EBA}$
l = Low state must be present one setup time before the low-to-high transition of $\overline{LEAB}$, $\overline{LEBA}$, $\overline{EAB}$ or $\overline{EBA}$
X = Don't care
↑ = LOW-to-HIGH level transition
NC = No change
Z = High impedance "off" state

DC CHARACTERISTICS FOR 74LVC544

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LVC544

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		-40 to +85				V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t_{PHL}/t_{PLH}	propagation delay $\overline{A_n}$ to $\overline{B_n}$, $\overline{B_n}$ to $\overline{A_n}$	1.5 1.5 1.5	22 5.8 5.1*	– 9.1 8.5	ns	1.2 2.7 3.0 to 3.6	Fig.5
t_{PHL}/t_{PLH}	propagation delay $\overline{LEBA}$ to $\overline{A_n}$, $\overline{LEAB}$ to $\overline{B_n}$	1.5 1.5 1.5	26 6.8 6.0*	– 11 10	ns	1.2 2.7 3.0 to 3.6	Fig.6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OEBA}$ to $\overline{A_n}$, $\overline{OEAB}$ to $\overline{B_n}$	1.5 1.5 1.5	– 6.2 5.5*	– 9.7 9.1	ns	1.2 2.7 3.0 to 3.6	Fig.7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OEBA}$ to $\overline{A_n}$, $\overline{OEAB}$ to $\overline{B_n}$	1.5 1.5 1.5	– 5.2 4.5*	– 7.5 7.0	ns	1.2 2.7 3.0 to 3.6	Fig.7
t_{PZH}/t_{PZL}	3-state output enable time $\overline{EBA}$ to $\overline{A_n}$, $\overline{EAB}$ to $\overline{B_n}$	1.5 1.5 1.5	– 6.5 5.7*	– 10 9.5	ns	1.2 2.7 3.0 to 3.6	Fig.7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{EBA}$ to $\overline{A_n}$,$\overline{EAB}$ to $\overline{B_n}$	1.5 1.5 1.5	– 5.2 4.5*	– 7.5 7.0	ns	1.2 2.7 3.0 to 3.6	Fig.7

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		-40 to +85				V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t_W	LE pulse width LOW	4.0 4.0	– –	– –	ns	2.7 3.0 to 3.6	Fig.6
t_{su}	set-up time $\overline{A_n}/\overline{B_n}$ to $\overline{LEXX}$, $\overline{A_n}/\overline{B_n}$ to $\overline{EXX}$	– 1.0 1.0	– – –	– – –	ns	1.2 2.7 3.0 to 3.6	Fig.8
t_h	hold time $\overline{A_n}/\overline{B_n}$ to $\overline{LEXX}$, $\overline{A_n}/\overline{B_n}$ to $\overline{EXX}$	– 1.0 1.0	– – –	– – –	ns	1.2 2.7 3.0 to 3.6	Fig.8

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

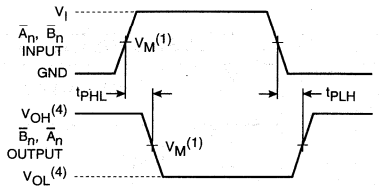


Fig.5 Waveforms showing the input ($\overline{A}_n$, $\overline{B}_n$) to output ($\overline{B}_n$, $\overline{A}_n$) propagation delays.

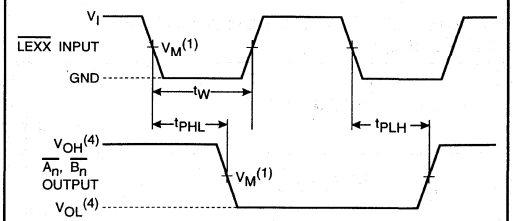


Fig.6 Waveforms showing the latch enable input ($\overline{LEXX}$) pulse width, the latch enable input to output ($\overline{A}_n$, $\overline{B}_n$) propagation delays.

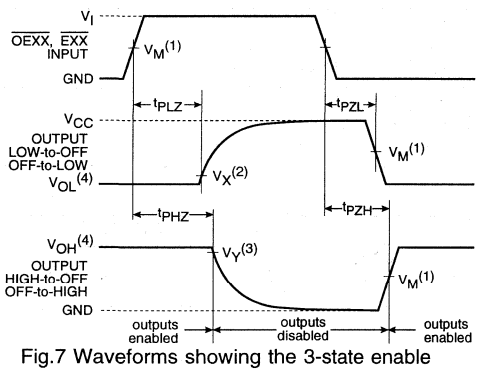


Fig.7 Waveforms showing the 3-state enable and disable times

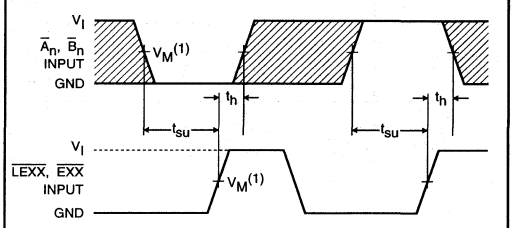
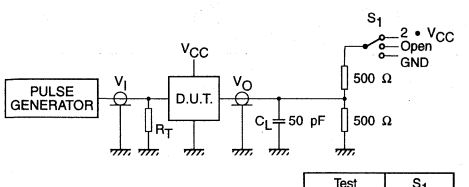


Fig.8 Waveforms showing the data set-up and hold times for the ($\overline{A}_n$, $\overline{B}_n$) input to the $\overline{LEXX}$ and $\overline{EXX}$ inputs.

Note to Fig.8:
The shaded areas indicate when the input is permitted to change for predictable output performance.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.9 Load circuitry for switching times.

Notes:

(1) V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
V_M = 0.5 · V_{CC} at V_{CC} < 2.7 V

(2) $V_X = V_{OL}$ + 0.3 V at $V_{CC} \geq$ 2.7 V
$V_X = V_{OL}$ + 0.1 · V_{CC} at V_{CC} < 2.7 V

(3) $V_Y = V_{OH}$ − 0.3 V at $V_{CC} \geq$ 2.7 V
$V_Y = V_{OH}$ − 0.1 · V_{CC} at V_{CC} < 2.7 V

(4) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **Inputs accept voltages upto 5.5 V**
- **CMOS low power consumption**
- **Direct interface with TTL levels**
- **Flow-through pin-out architecture**
- **Output drive capability 50 Ω transmission lines @ 85 °C**

DESCRIPTION

The 74LVC573 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment.

The 74LVC573 is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. A latch enable ($\overline{LE}$) input and an output enable ($\overline{OE}$) input are common to all internal latches.

The '573' consists of eight D-type transparent latches with 3-state true outputs. When LE is HIGH, data at the D_n inputs enters the latches. In this condition the latches are transparent, i.e. a latch output will change each time its corresponding D-input changes. When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the eight latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

The '573' is functionally identical to the '373', but the '373' has a different pin arrangement.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n; LE to Q_n	C_L = 50 pF V_{CC} = 3.3 V	4.3 4.6	ns
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	23	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC573D	20	SO	plastic	SO20/SOT163A
74LVC573DB	20	SSOP	plastic	SSOP20/SOT339
74LVC573PW	20	TSSOP	plastic	TSSOP20/SOT360

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D_0 to D_7	data inputs
19, 18, 17, 16, 15, 14, 13, 12	Q_0 to Q_7	3-state latch outputs
10	GND	ground (0 V)
11	LE	latch enable input (active HIGH)
20	V_{CC}	positive supply voltage

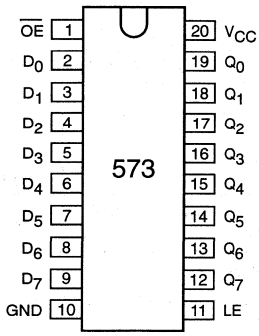


Fig.1 Pin configuration.

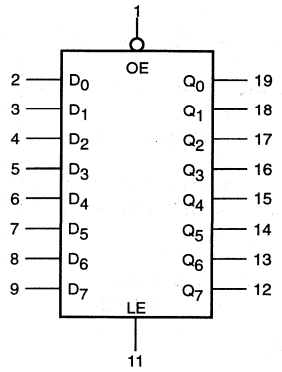


Fig.2 Logic symbol.

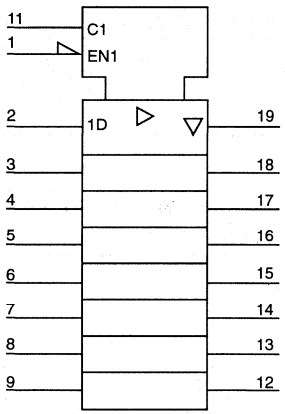


Fig3. IEC logic symbol.

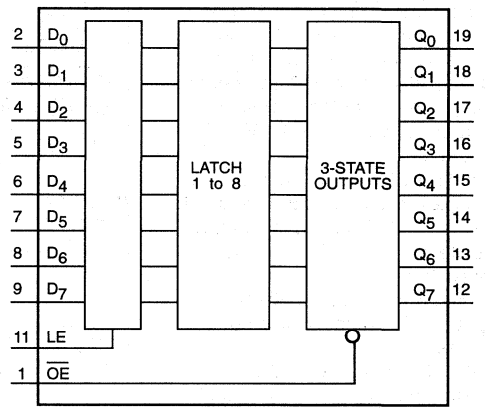


Fig.4 Functional diagram.

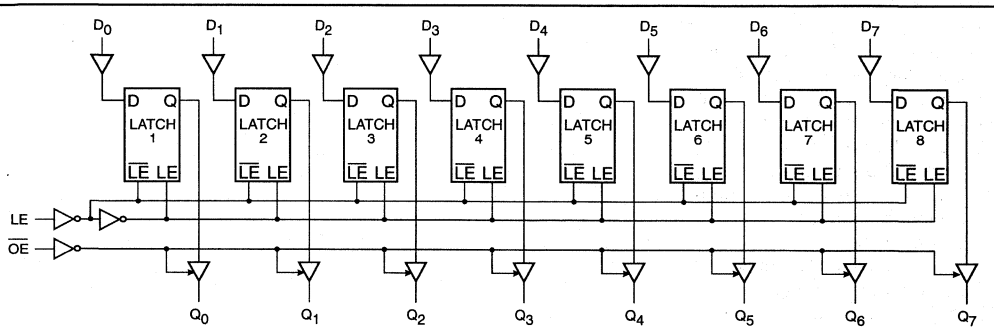


Fig.5 Logic diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$\overline{OE}$	LE	D_n		Q_0 to Q_7
enable and read register (transparent mode)	L L	H H	L H	L H	L H
latch and read register	L L	L L	l h	L H	L H
latch register and disable outputs	H H	L L	l h	L H	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
X = don't care
Z = high impedance OFF-state

DC CHARACTERISTICS FOR 74LVC573

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74LVC573

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		-40 to +85				V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n	– 1.5 1.5	21 4.7 4.3*	– 8.0 7.8	ns	1.2 2.7 3.0 to 3.6	Fig.6
t_{PHL}/t_{PLH}	propagation delay LE to Q_n	– 1.5 1.5	23 5.3 4.6*	– 10 8.5	ns	1.2 2.7 3.0 to 3.6	Fig.7
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n	– 1.5 1.5	17 4.4 3.8*	– 8.0 7.5	ns	1.2 2.7 3.0 to 3.6	Fig.8
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n	– 1.5 1.5	8.0 4.0 3.5*	– 6.5 6.0	ns	1.2 2.7 3.0 to 3.6	Fig.8
t_W	LE pulse width HIGH	– –	3.0 3.0*	– –	ns	2.7 3.0 to 3.6	Fig.7
t_{su}	set-up time D_n to LE	1.0 1.0	0.2 0.2*	– –	ns	2.7 3.0 to 3.6	Fig.9
t_h	hold time D_n to LE	1.0 1.0	0 0*	– –	ns	2.7 3.0 to 3.6	Fig.9

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

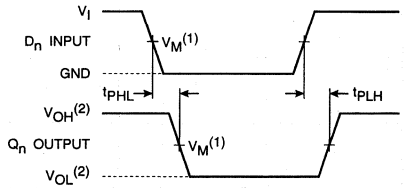


Fig.6 Waveforms showing the input (D_n) to output (Q_n) propagation delays.

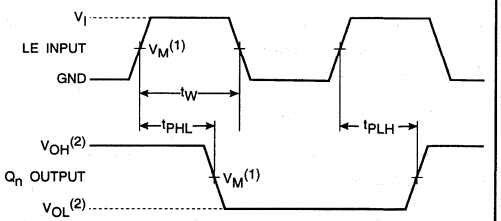


Fig.7 Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output (Q_n) propagation delays.

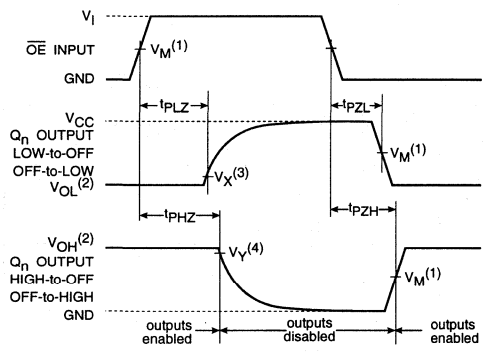


Fig.8 Waveforms showing the 3-state enable and disable times

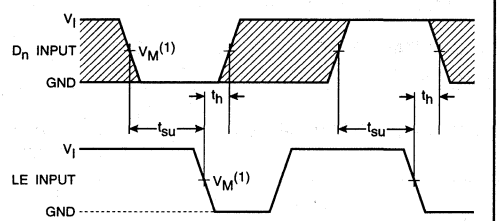
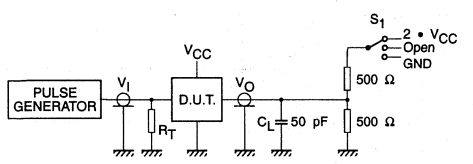


Fig.9 Waveforms showing the data set-up and hold times for the D_n input to the LE input.

Note to Fig.9:

The shaded areas indicate when the input is permitted to change for predictable output performance.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.10 Load circuitry for switching times.

Notes:

(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

Octal D-type flip-flop; positive-edge trigger; 3-state 74LVC574

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **Inputs accept voltages upto 5.5 V**
- **CMOS low power consumption**
- **Direct interface with TTL levels**
- **8-bit positive edge-triggered register**
- **Independent register and 3-state buffer operation**
- **Flow-through pin-out architecture**
- **Output drive capability 50 Ω transmission lines @ 85 °C**

DESCRIPTION

The 74LVC574 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment.

The 74LVC574 is an octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A clock (CP) and an output enable ($\overline{OE}$) input are common to all flip-flops.

The eight flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition.

When $\overline{OE}$ is LOW, the contents of the eight flip-flops is available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops. the '574' is functionally identical to the '374', but the '374' has a different pin arrangement.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 50 pF; V_{CC} = 3.3 V	4.8	ns
f_{max}	maximum clock frequency		150	MHz
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	28	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC574D	20	SO	plastic	SO20/SOT163A
74LVC574DB	20	SSOP	plastic	SSOP20/SOT339
74LVC574PW	20	TSSOP	plastic	TSSOP20/SOT360

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D_0 to D_7	data inputs
19, 18, 17, 16, 15, 14, 13, 12	Q_0 to Q_7	3-state flip-flop outputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
20	V_{CC}	positive supply voltage

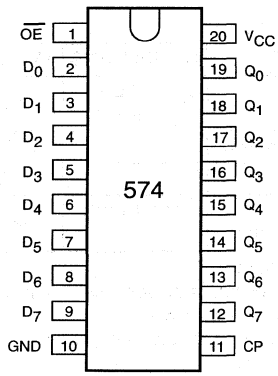


Fig.1 Pin configuration.

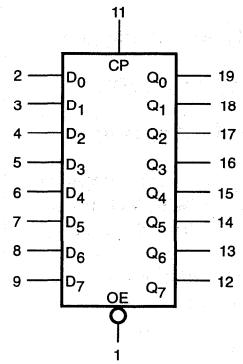


Fig.2 Logic symbol.

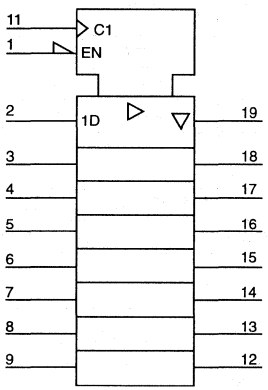


Fig3. IEC logic symbol.

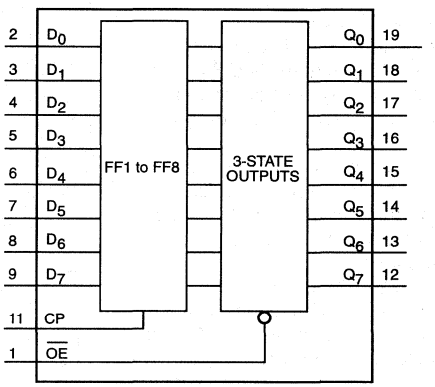


Fig.4 Functional diagram.

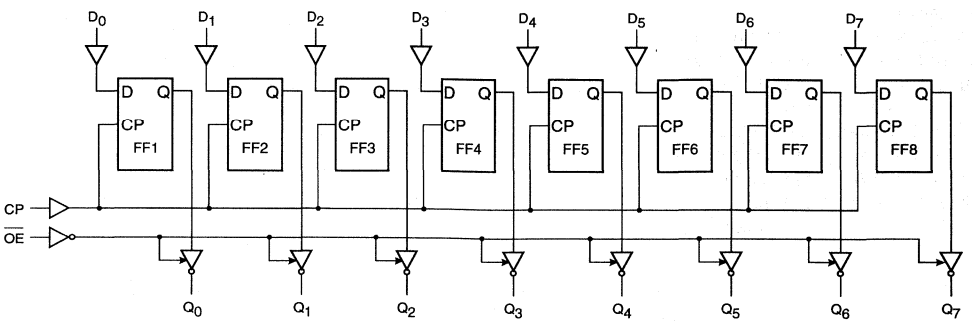


Fig.5 Logic diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	CP	D_n		Q_0 to Q_7
load and read register	L	↑	l	L	L
	L	↑	h	H	H
load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
Z = high impedance OFF-state
↑ = LOW-to-HIGH clock transition

DC CHARACTERISTICS FOR 74LVC574

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74LVC574

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		–40 to +85				V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	–	21	–	ns	1.2	Fig.6
		1.5	5.2	9.5		2.7	
		1.5	4.8*	8.5		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n	–	17	–	ns	1.2	Fig.7
		1.5	4.4	8.0		2.7	
		1.5	4.0*	7.5		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n	–	8.0	–	ns	1.2	Fig.7
		1.5	3.6	6.5		2.7	
		1.5	3.5*	6.0		3.0 to 3.6	
t_W	clock pulse width HIGH or LOW	–	3.0	–	ns	2.7	Fig.6
		–	3.0*	–		3.0 to 3.6	
t_{su}	set-up time D_n to CP	1.0	0.3	–	ns	2.7	Fig.8
		1.0	0.3*	–		3.0 to 3.6	
t_h	hold time D_n to CP	1.0	–0.2	–	ns	2.7	Fig.8
		1.0	–0.2*	–		3.0 to 3.6	
f_{max}	maximum clock pulse frequency	–	–	–	MHz	2.7	Fig.6
		75	150*	–		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

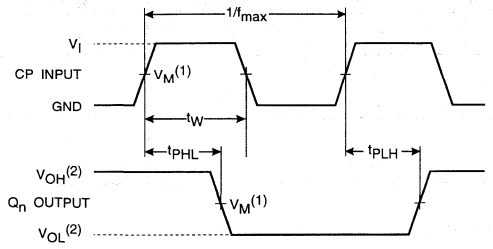


Fig.6 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width and the maximum clock pulse frequency.

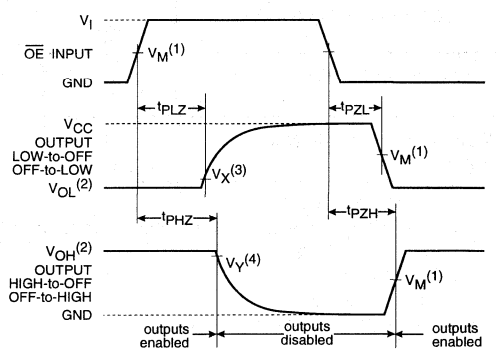


Fig.7 Waveforms showing the 3-state enable and disable times.

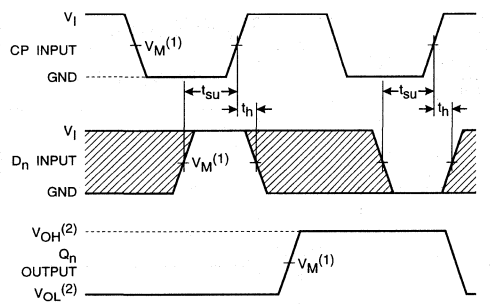
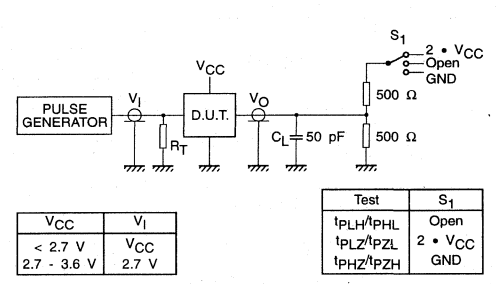


Fig.8 Waveforms showing the data set-up and hold times for the D_n input to the CP input.

Note to Fig.8:

The shaded areas indicate when the input is permitted to change for predictable output performance.



VCC	VI
< 2.7 V	VCC
2.7 - 3.6 V	2.7 V

Test	S1
tPLH/tPHL	Open
tPLZ/tPZL	2 • VCC
tPHZ/tPZH	GND

Fig.9 Load circuitry for switching times.

Notes:

(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

Octal transceiver with dual enable; 3-state 74LVC623

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with the JEDEC standard no. 8-1A**
- **Flow-through pin-out architecture**
- **CMOS low power consumption**
- **inputs accept voltages upto 5.5 V**
- **Direct interface with TTL levels**
- **Output drive capability 50 Ω transmission lines @ 85 °C**

DESCRIPTION

The 74LVC623 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families. The 74LVC623 is an octal transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. This octal bus transceiver is designed for asynchronous two-way communication between data buses. The control function implementation allows maximum flexibility in timing. This device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the enable inputs (OE_{AB}, $\overline{OE}_{BA}$). The enable inputs can be used to disable the device so that the buses are effectively isolated. The dual enable function configuration gives this transceiver the capability to store data by simultaneous enabling of OE_{AB} and $\overline{OE}_{BA}$. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance OFF-state, both sets of bus lines will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical.

The '623' is identical to the '620' but has true (non-inverting) outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n	C_L = 50 pF V_{CC} = 3.3 V	3.8	ns
C_I	input capacitance		5.0	pF
$C_{I/O}$	input/output capacitance		10	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	40	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC623D	20	SO	plastic	SO20/SOT163A
74LVC623DB	20	SSOP	plastic	SSOP20/SOT339
74LVC623PW	20	TSSOP	plastic	TSSOP20/SOT360

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	OE_{AB}	output enable input (active HIGH)
2, 3, 4, 5, 6, 7, 8, 9	A_0 to A_7	data inputs/outputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	B_0 to B_7	data inputs/outputs
19	$\overline{OE}_{BA}$	output enable input (active LOW)
20	V_{CC}	positive supply voltage

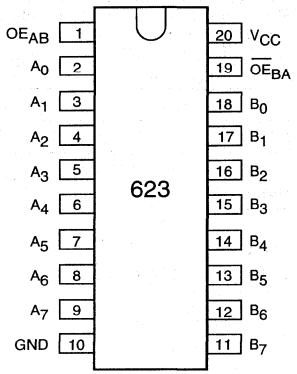


Fig.1 Pin configuration.

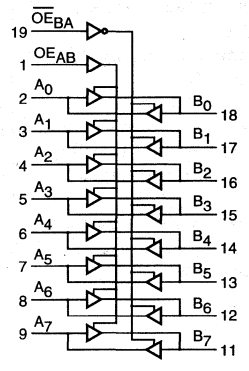


Fig.2 Logic symbol.

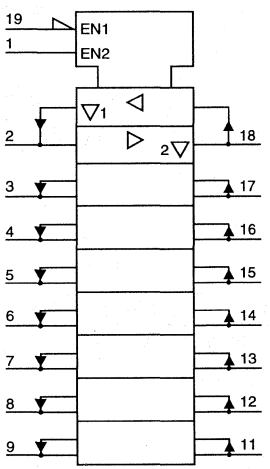


Fig.3 IEC logic symbol.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
OE_{AB}	$\overline{OE}_{BA}$	A_n	B_n
L	L	A = B	inputs
H	H	inputs	B = A
L	H	Z	Z
H	L	A = B inputs	inputs B = A

H = HIGH voltage level
L = LOW voltage level
Z = high impedance OFF-state

DC CHARACTERISTICS FOR 74LVC623

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LVC623

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		-40 to +85				V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n	– 1.5 1.5	21 4.6 4.1*	– 8.5 7.5	ns	1.2 2.7 3.0 to 3.6	Fig.4
t_{PZH}/t_{PZL}	3-state output enable time OE_{AB} to B_n	– 1.5 1.5	25 5.0 4.5*	– 8.5 7.5	ns	1.2 2.7 3.0 to 3.6	Fig.6, 7
t_{PHZ}/t_{PLZ}	3-state output disable time OE_{AB} to B_n	– 1.5 1.5	8 4.5 4.0*	– 7.5 6.5	ns	1.2 2.7 3.0 to 3.6	Fig.6, 7
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_{BA}$ to A_n	– 1.5 1.5	25 5.0 4.5*	– 8.5 7.5	ns	1.2 2.7 3.0 to 3.6	Fig.5, 7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_{BA}$ to A_n	– 1.5 1.5	8 4.5 4.0*	– 7.5 6.5	ns	1.2 2.7 3.0 to 3.6	Fig.5, 7

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

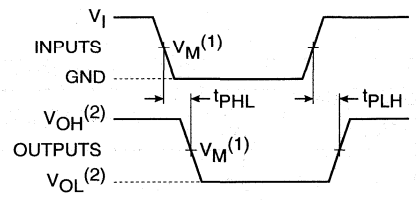


Fig. 4 Waveforms showing the input (A_n, B_n) to output (B_n, A_n) propagation delays.

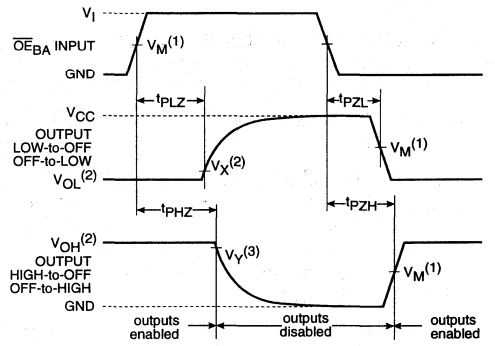


Fig.5 Waveforms showing the 3-state enable and disable times for $\overline{OE}_{BA}$ input.

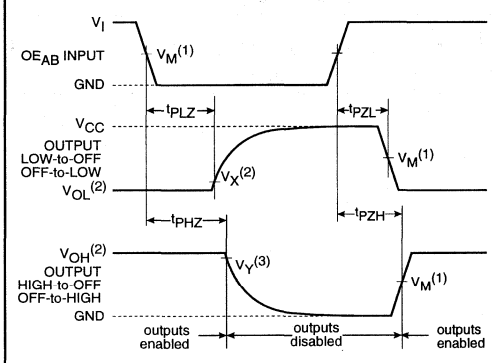
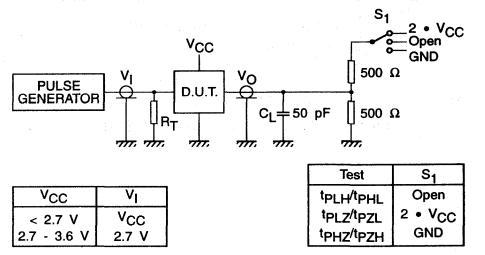


Fig.6 Waveforms showing the 3-state enable and disable times for OE_{AB} input.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.7 Load circuitry for switching times.

Notes:

(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

Octal bus transceiver/register; 3-state 74LVC646

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **Inputs accept voltages upto 5.5 V**
- **CMOS low power consumption**
- **Direct interface with TTL levels**
- **Flow-through pin-out architecture**

DESCRIPTION

The 74LVC646 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74LVC646 consist of 8 non-inverting bus transceiver circuits with 3-state outputs, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the internal registers. Data on the 'A' or 'B' bus will be clocked in the internal registers, as the appropiate clock (CP_{AB} or CP_{BA}) goes to a HIGH logic level. Output enable ($\overline{OE}$) and direction (DIR) inputs are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the 'A' or 'B' register, or in both.The select source inputs (S_{AB} and S_{BA}) can multiplex stored and real-time (transparent mode) data. The direction (DIR) input determines which bus will receive data when $\overline{OE}$ is active (LOW). In the isolation mode ($\overline{OE}$ = HIGH), 'A' data may be stored in the 'B' register and/or 'B' data may be stored in the 'A' register.
When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, 'A' or 'B' may be driven at a time.

The '646' is functionally identical to the '648', but has non-inverting data paths.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to B_n, A_n	C_L = 50 pF V_{CC} = 3.3 V	4.7	ns
f_{max}	maximum clock frequency		150	MHz
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	47	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PACKAGE	MATERIAL	CODE
74LVC646D	24	SO	plastic	SO24/SOT137A
74LVC646DB	24	SSOP	plastic	SSOP24/SOT340
74LVC646PW	24	TSSOP	plastic	TSSOP/SOT355

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	CP_{AB}	'A' to 'B' clock input (Low-to-High, edge-triggered)
2	S_{AB}	select 'A' to 'B' source input
3	DIR	direction control input
4, 5, 6, 7, 8, 9, 10, 11	A_0 to A_7	'A' data inputs/outputs
12	GND	ground (0 V)
20, 19, 18, 17, 16,15, 14, 13	B_0 to B_7	'B' data inputs/outputs
21	$\overline{OE}$	output enable input (active LOW)
22	S_{BA}	select 'B' to 'A' source input
23	CP_{BA}	'B' to 'A' clock input (Low-to-High, edge-triggered)
24	V_{CC}	positive supply voltage

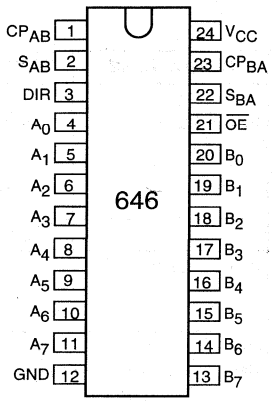


Fig.1 Pin configuration.

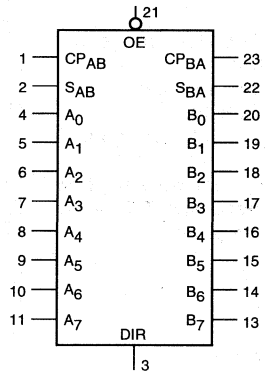


Fig.2 Logic symbol.

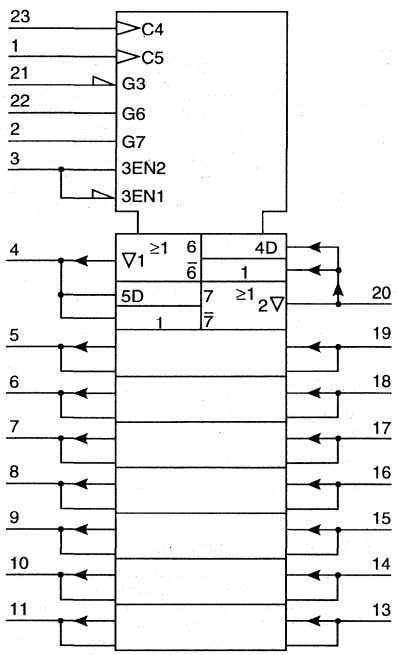


Fig3. IEC logic symbol.

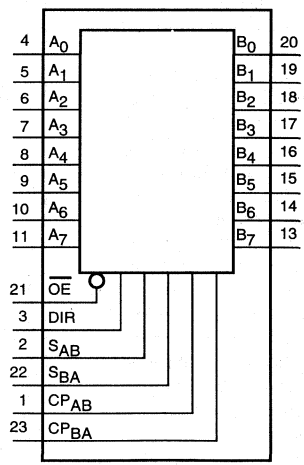


Fig.4 Functional diagram.

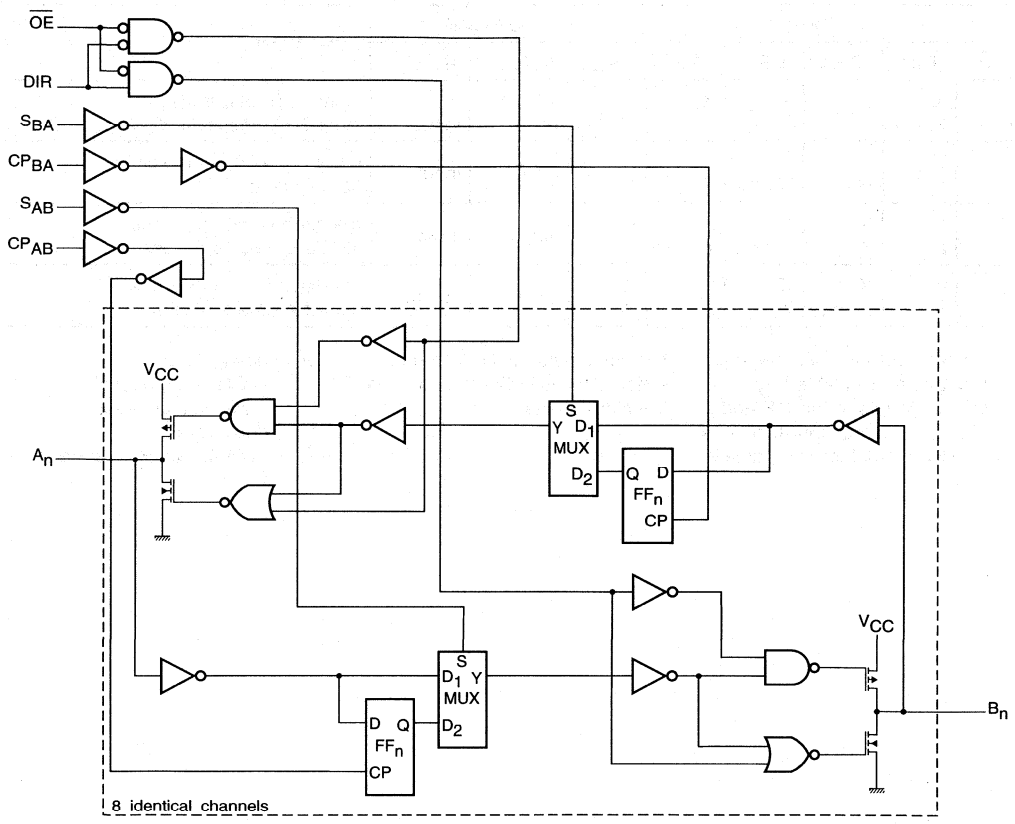


Fig.5 Logic diagram.

FUNCTION TABLE

INPUTS						DATA I/O *		FUNCTION
$\overline{OE}$	DIR	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	A_0 to A_7	B_0 to B_7	
X X	X X	↑ X	X ↑	X X	X X	input un*	un* input	store A, B unspecified* store B, A unspecified*
H H	X X	↑ H or L	↑ H or L	X X	X X	input	input	store A and B data, isolation hold storage
L L	L L	X X	X H or L	X X	L H	output	input	real-time B data to A bus stored B data to A bus
L L	H H	X H or L	X X	L H	X X	input	output	real-time A data to B bus stored A data to B bus

* The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

un = unspecified
H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH level transition

DC CHARACTERISTICS FOR 74LVC646

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74LVC646

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C) -40 to +85			UNIT	TEST CONDITIONS	
		MIN.	TYP.	MAX.		V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to B_n, A_n	1.5 1.5 1.5	24 5.2 4.6*	– 9.2 7.9	ns	1.2 2.7 3.0 to 3.6	Fig.6
t_{PHL}/t_{PLH}	propagation delay CP_{AB}, CP_{BA} to B_n, A_n	1.5 1.5 1.5	26 6.0 5.2*	– 11 8.9	ns	1.2 2.7 3.0 to 3.6	Fig.7
t_{PHL}/t_{PLH}	propagation delay S_{AB}, S_{BA} to B_n, A_n	1.5 1.5 1.5	27 6.4 5.2*	– 11 8.8	ns	1.2 2.7 3.0 to 3.6	Fig.8
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to A_n, B_n	1.5 1.5 1.5	21 5.3 4.8*	– 9.5 8.5	ns	1.2 2.7 3.0 to 3.6	Fig.9
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to A_n, B_n	1.5 1.5 1.5	16 4.3 4.0*	– 7.5 6.5	ns	1.2 2.7 3.0 to 3.6	Fig.9
t_{PZH}/t_{PZL}	3-state output enable time DIR to A_n, B_n	1.5 1.5 1.5	21 5.3 4.8	– 9.5 8.5	ns	1.2 2.7 3.0 to 3.6	Fig.10
t_{PHZ}/t_{PLZ}	3-state output disable time DIR to A_n, B_n	1.5 1.5 1.5	16 4.3 4.0*	– 7.5 6.5	ns	1.2 2.7 3.0 to 3.6	Fig.10
t_W	clock pulse width HIGH or LOW CP_{AB} or CP_{BA}	– –	3.0 3.0*	– –	ns	2.7 3.0 to 3.6	Figs 6 and 8
t_{su}	set-up time A_n, B_n to CP_{AB}, CP_{BA}	1.5 1.5	0.5 0.5*	– –	ns	2.7 3.0 to 3.6	Fig.7
t_h	hold time A_n, B_n to CP_{AB}, CP_{BA}	1.0 1.0	0 0*	– –	ns	2.7 3.0 to 3.6	Fig.7
f_{max}	maximum clock pulse frequency	– 75	– 150*	– –	ns	2.7 3.0 to 3.6	Fig.7

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

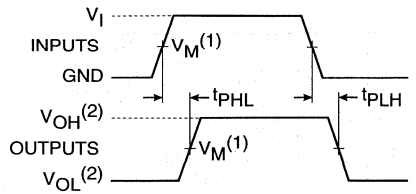


Fig.6 Waveforms showing the input A_n, B_n to output B_n, A_n propagation delays.

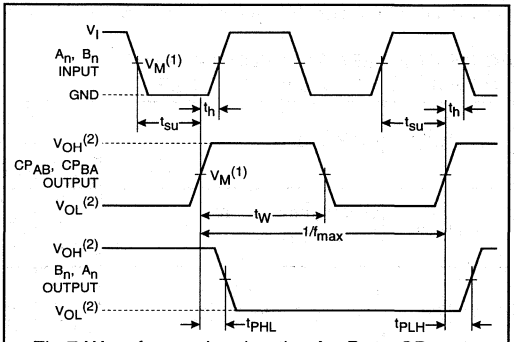


Fig.7 Waveforms showing the A_n, B_n to CP_{AB}, CP_{BA} set-up and hold times, clock CP_{AB}, CP_{BA} pulse width, maximum clock pulse frequency and the CP_{AB}, CP_{BA} to output B_n, A_n propagation delays.

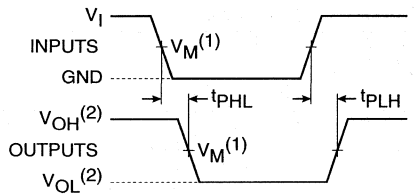


Fig.8 Waveforms showing the input S_{AB}, S_{BA} to output B_n, A_n propagation delay times.

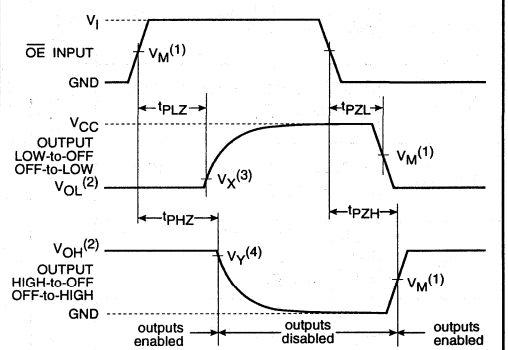


Fig.9 Waveforms showing the input $\overline{OE}$ to output A_n, B_n 3-state enable and disable times.

Notes:

(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

AC WAVEFORMS *(Continued)*

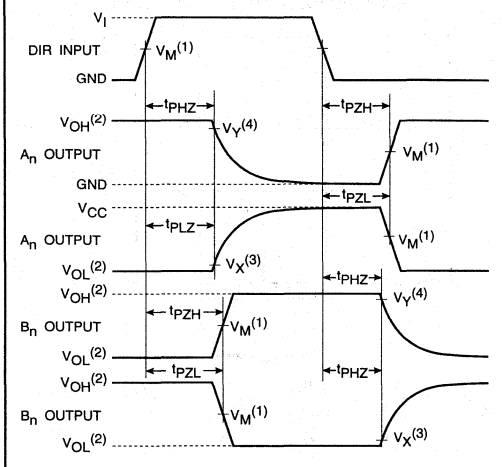
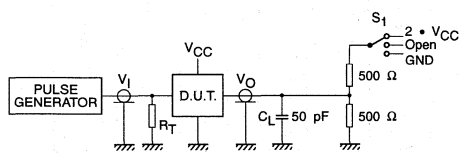


Fig.10 Waveforms showing the input DIR to output A_n, B_n 3-state enable and disable times.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.11 Load circuitry for switching times.

Notes:

(1) V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
$V_M = 0.5 \cdot V_{CC}$ at V_{CC} < 2.7 V

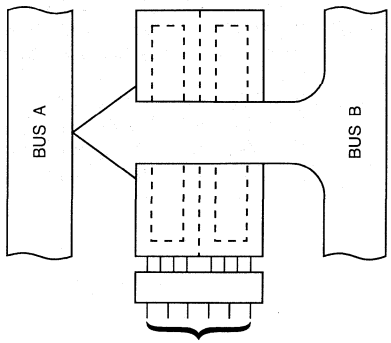
(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

(3) $V_X = V_{OL}$ + 0.3 V at $V_{CC} \geq$ 2.7 V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at V_{CC} < 2.7 V

(4) $V_Y = V_{OH}$ – 0.3 V at $V_{CC} \geq$ 2.7 V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at V_{CC} < 2.7 V

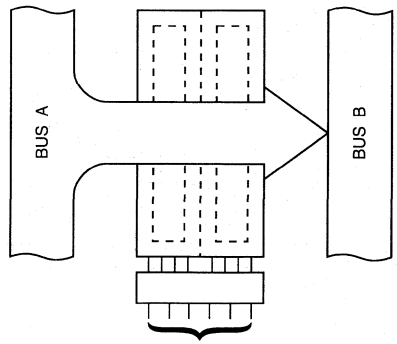
APPLICATION INFORMATION

Real-time transfer; bus B to bus A



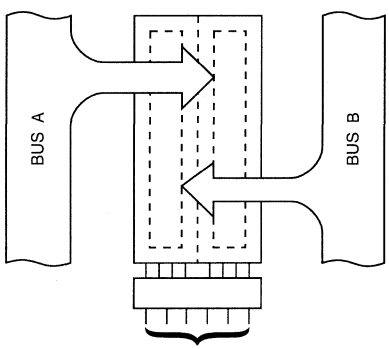
(1) $\overline{OE}$	(14) DIR	(28) CP_{AB}	(16) CP_{BA}	(27) S_{AB}	(15) S_{BA}
L	L	X	X	X	L

Real-time transfer; bus A to bus B



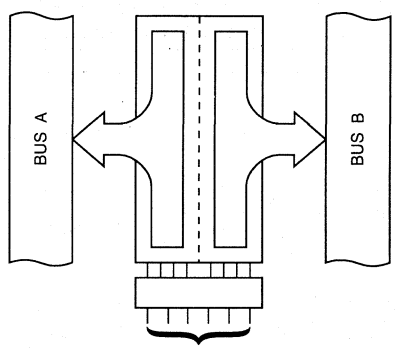
(1) $\overline{OE}$	(14) DIR	(28) CP_{AB}	(16) CP_{BA}	(27) S_{AB}	(15) S_{BA}
L	H	X	X	L	X

Storage from A, B or A and B



(1) $\overline{OE}$	(14) DIR	(28) CP_{AB}	(16) CP_{BA}	(27) S_{AB}	(15) S_{BA}
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

Transfer storage data to A or B



(1) $\overline{OE}$	(14) DIR	(28) CP_{AB}	(16) CP_{BA}	(27) S_{AB}	(15) S_{BA}
L	L	X	H or L	X	H
L	H	H or L	X	H	X

Octal transceiver/register with dual enable; 3-state 74LVC652

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **Flow-through pin-out architecture**
- **Inputs accept voltages upto 5.5 V**
- **CMOS low power consumption**
- **Direct interface with TTL levels**

DESCRIPTION

The 74LVC652 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74LVC652 consist of 8 non–inverting bus transceiver circuits with 3-state outputs, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Data on the "A" or "B" or both buses, will be stored in the internal registers, at the appropiate clock inputs (CP_{AB} or CP_{BA}) regardless of the select inputs (S_{AB} and S_{BA}) or output enable (OE_{AB} and $\overline{OE}_{BA}$) control inputs. Depending on the select inputs S_{AB} and S_{BA} data can directly go from input to output (real time mode) or data can be controlled by the clock (storage mode), this is when the OE_n inputs this operating mode permits. The output enable inputs OE_{AB} and $\overline{OE}_{BA}$ determine the operation mode of the transceiver. When OE_{AB} is LOW, no data transmission from A_n to B_n is possible and when $\overline{OE}_{BA}$ is HIGH, there is no data transmission from B_n to A_n possible. When S_{AB} and S_{BA} are in the real time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OE_{AB} and $\overline{OE}_{BA}$. In this configuration each output reinforces its input. The '652' is functionally identical to the '651', but has non–inverting data paths.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to B_n, A_n	C_L = 50 pF V_{CC} = 3.3 V	5.0	ns
f_{max}	maximum clock frequency		150	MHz
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	45	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC652D	24	SO	plastic	SO24/SOT137A
74LVC652DB	24	SSOP	plastic	SSOP24/SOT340
74LVC652PW	24	TSSOP	plastic	TSSOP24/SOT355

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	CP_{AB}	'A' to 'B' clock input (Low-to-High, edge-triggered)
2	S_{AB}	select 'A' to 'B' source input
3	OE_{AB}	output enable B to A input
4, 5, 6, 7, 8, 9, 10, 11	A_0 to A_7	'A' data inputs/outputs
12	GND	ground (0 V)
20, 19, 18, 17, 16,15, 14, 13	B_0 to B_7	'B' data inputs/outputs
21	$\overline{OE}_{BA}$	output enable A to B input
22	S_{BA}	select 'B' to 'A' source input
23	CP_{BA}	'B' to 'A' clock input (Low-to-High, edge-triggered)
24	V_{CC}	positive supply voltage

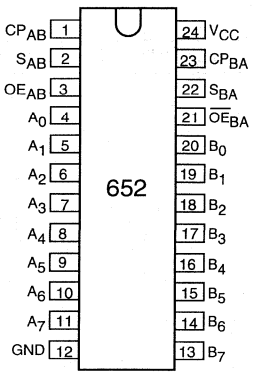


Fig.1 Pin configuration.

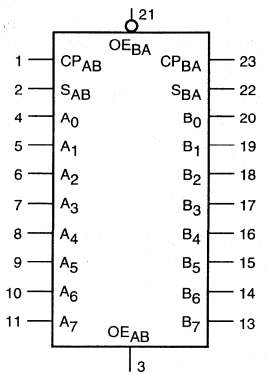


Fig.2 Logic symbol.

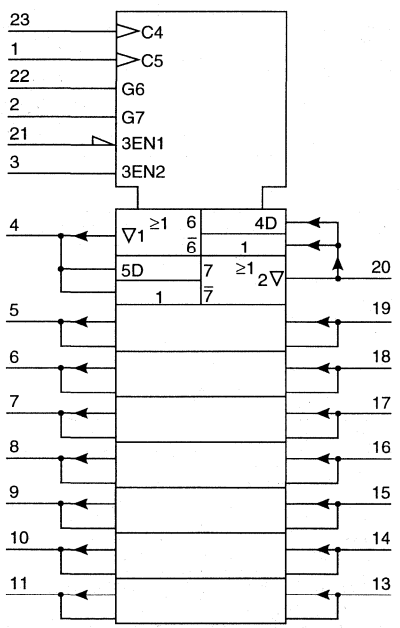


Fig3. IEC logic symbol.

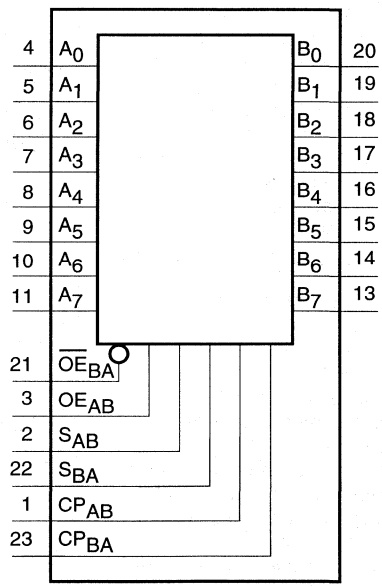


Fig.4 Functional diagram.

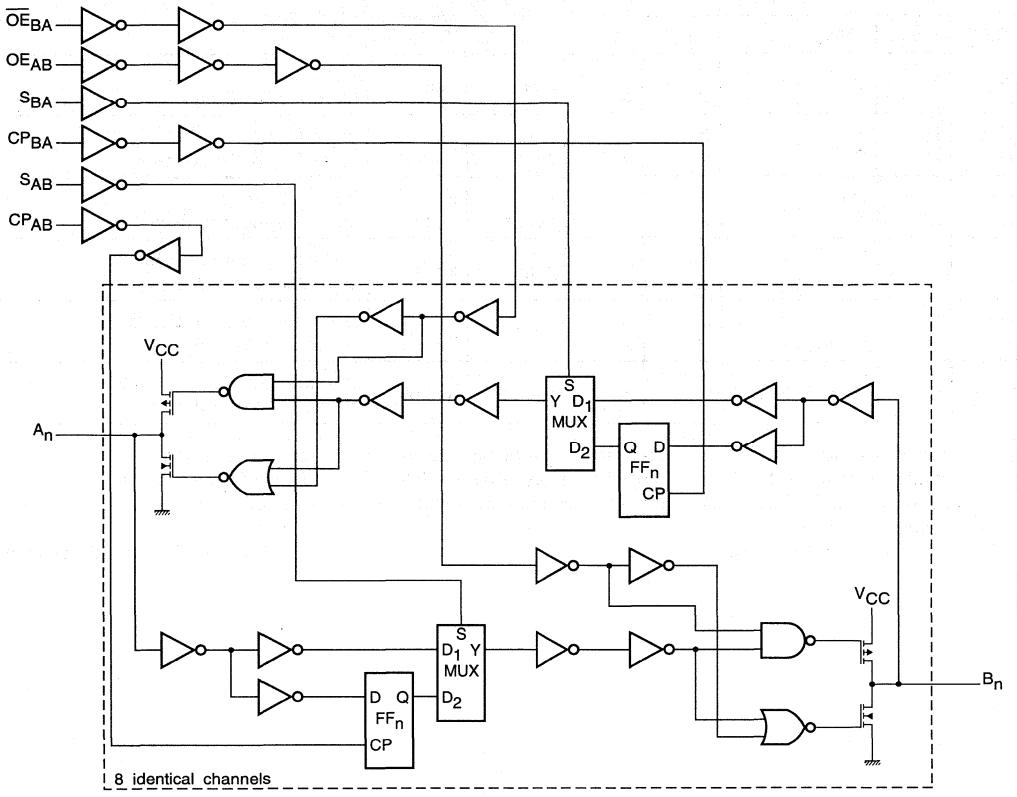


Fig.5 Logic diagram.

FUNCTION TABLE

INPUTS						DATA I/O *		FUNCTION
OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	A_0 to A_7	B_0 to B_7	
L L	H H	H or L ↑	H or L ↑	X X	X X	input	input	isolation store A and B data
X H	H H	↑ ↑	H or L ↑	X L	X X	input input	un* output	store A, hold B store A in both registers
L L	X L	H or L ↑	↑ ↑	X X	X L	un* output	input input	hold A, store B store B in both registers
L L	L L	X X	X H or L	X X	L H	output	input	real time B data to A bus stored B data to A bus
H H	H H	X H or L	X X	L H	X X	input	output	real-time A data to B bus stored A data to B bus
H	L	H or L	H or L	H	H	output	output	stored A data to B bus and stored B data to A bus

* The data output functions may be enabled or disabled by various signals at the OE_{AB} and $\overline{OE}_{BA}$ inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

un = unspecified
H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH level transition

DC CHARACTERISTICS FOR 74LVC652

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74LVC652

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C) −40 to +85			UNIT	TEST CONDITIONS	
		MIN.	TYP.	MAX.		V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to B_n, A_n	1.5 1.5 1.5	24 5.2 4.6*	– 9.2 7.9	ns	1.2 2.7 3.0 to 3.6	Fig.6
t_{PHL}/t_{PLH}	propagation delay CP_{AB}, CP_{BA} to B_n, A_n	1.5 1.5 1.5	26 6.0 5.2*	– 11 8.9	ns	1.2 2.7 3.0 to 3.6	Fig.7
t_{PHL}/t_{PLH}	propagation delay S_{AB}, S_{BA} to B_n, A_n	1.5 1.5 1.5	27 6.4 5.2*	– 11 8.8	ns	1.2 2.7 3.0 to 3.6	Fig.8
t_{PZH}/t_{PZL}	3-state output enable time OE_{AB} to B_n	1.5 1.5 1.5	20 5.3 4.8*	– 9.5 8.5	ns	1.2 2.7 3.0 to 3.6	Fig.9
t_{PHZ}/t_{PLZ}	3-state output disable time OE_{AB} to B_n	1.5 1.5 1.5	16 4.3 4.0*	– 7.5 6.5	ns	1.2 2.7 3.0 to 3.6	Fig.9
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_{BA}$ to A_n	1.5 1.5 1.5	20 5.3 4.8*	– 9.5 8.5	ns	1.2 2.7 3.0 to 3.6	Fig.9
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_{BA}$ to A_n	1.5 1.5 1.5	16 4.3 4.0*	– 7.5 6.5	ns	1.2 2.7 3.0 to 3.6	Fig.9
t_W	clock pulse width HIGH or LOW CP_{AB} or CP_{BA}	– –	3.0 3.0*	– –	ns	2.7 3.0 to 3.6	Figs 6 and 8
t_{su}	set-up time A_n, B_n to CP_{AB}, CP_{BA}	1.5 1.5	0.5 0.5*	– –	ns	2.7 3.0 to 3.6	Fig.7
t_h	hold time A_n, B_n to CP_{AB}, CP_{BA}	1.0 1.0	0 0*	– –	ns	2.7 3.0 to 3.6	Fig.7
f_{max}	maximum clock pulse frequency	– 75	– 150*	– –	MHz	2.0 3.0 to 3.6	Fig.7

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

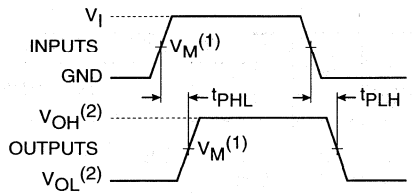


Fig.6 Waveforms showing the input A_n, B_n to output B_n, A_n propagation delays.

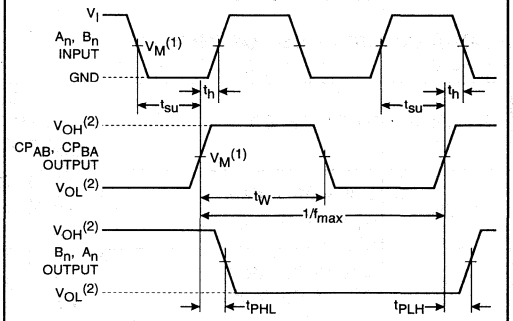


Fig.7 Waveforms showing the A_n, B_n to CP_{AB}, CP_{BA} set-up and hold times, clock CP_{AB}, CP_{BA} pulse width, maximum clock pulse frequency and the CP_{AB}, CP_{BA} to output B_n, A_n propagation delays.

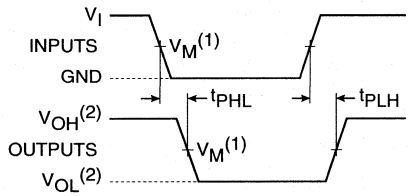


Fig.8 Waveforms showing the input S_{AB}, S_{BA} to output B_n, A_n propagation delay times.

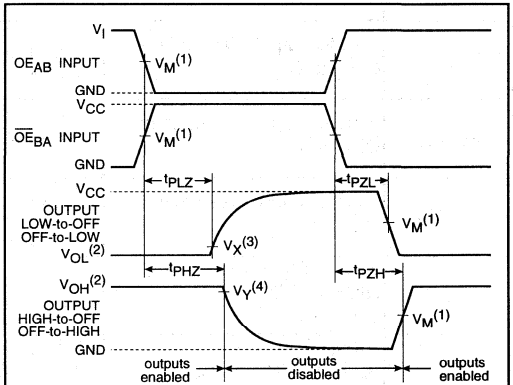


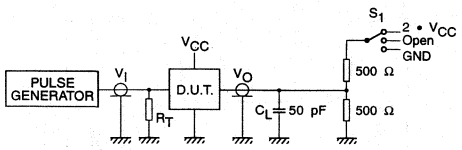
Fig.9 Waveforms showing the OE inputs (OE_{AB}, $\overline{OE}_{BA}$) to outputs A_n, B_n enable and disable times.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V



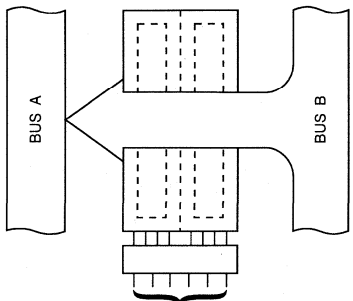
V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.11 Load circuitry for switching times.

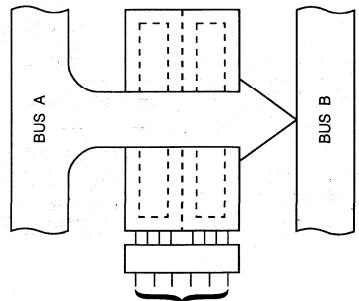
APPLICATION INFORMATION

Real-time transfer; bus B to bus A



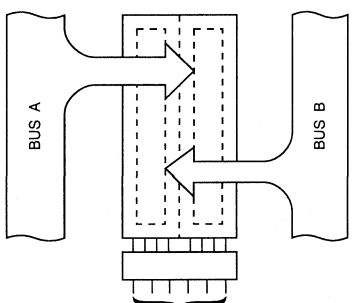
OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
L	L	X	X	X	L

Real-time transfer; bus A to bus B



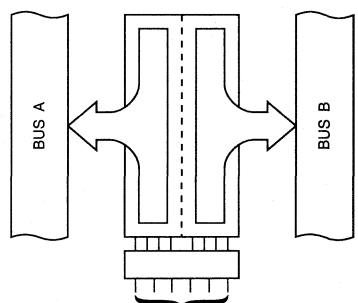
OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
H	H	X	X	L	X

Store A, B or A and B in one register



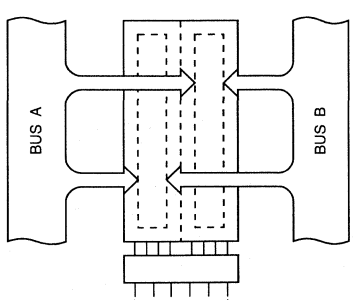
OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

Transfer A stored data to B bus or B stored data to A bus or both at the same time



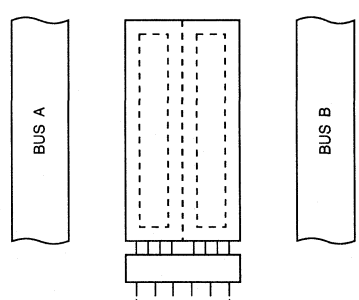
OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
H	H	H or L	X	H	X
L	L	X	H or L	X	H
H	L	H or L	H or L	H	H

Store bus A in both registers or store bus B in both registers



OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
H	H	↑	↑	L	X
L	L	↑	↑	X	L

Isolation



OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
L	H	H or L	H or L	X	X

10-Bit D-type flip-flop; positive-edge trigger; 3-state 74LVC821

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **Inputs accept voltages upto 5.5 V**
- **CMOS low power consumption**
- **Direct interface with TTL levels**
- **8-bit positive edge-triggered register**
- **Independent register and 3-state buffer operation**
- **Flow-through pin-out architecture**
- **Output drive capability 50 Ω transmission lines @ 85 °C**

DESCRIPTION

The 74LVC821 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment.

The 74LVC821 is a 10-bit D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A clock (CP) and an output enable ($\overline{OE}$) input are common to all flip-flops.

The ten flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition.

When $\overline{OE}$ is LOW, the contents of the ten flip-flops is available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 50 pF V_{CC} = 3.3 V	4.8	ns
f_{max}	maximum clock frequency		150	MHz
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	28	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC821D	24	SO	plastic	SO24/SOT137
74LVC821DB	24	SSOP	plastic	SSOP24/SOT340
74LVC821PW	24	TSSOP	plastic	TSSOP24/SOT355

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9, 10, 11	D_0 to D_9	data inputs
23, 22, 21, 20, 19, 18, 17, 16, 15, 14	Q_0 to Q_9	3-state flip-flop outputs
12	GND	ground (0 V)
13	CP	clock input (LOW-to-HIGH, edge-triggered)
24	V_{CC}	positive supply voltage

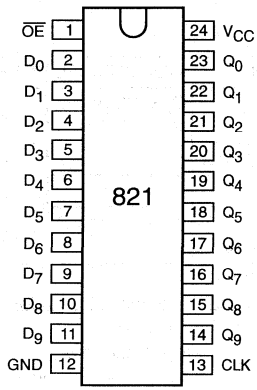


Fig.1 Pin configuration.

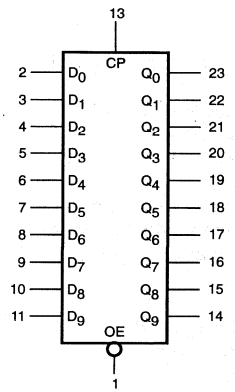


Fig.2 Logic symbol.

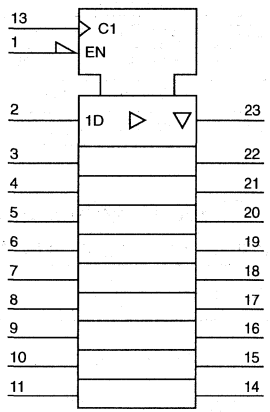


Fig3. IEC logic symbol.

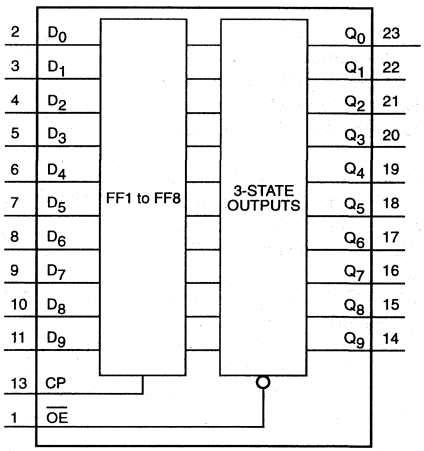


Fig.4 Functional diagram.

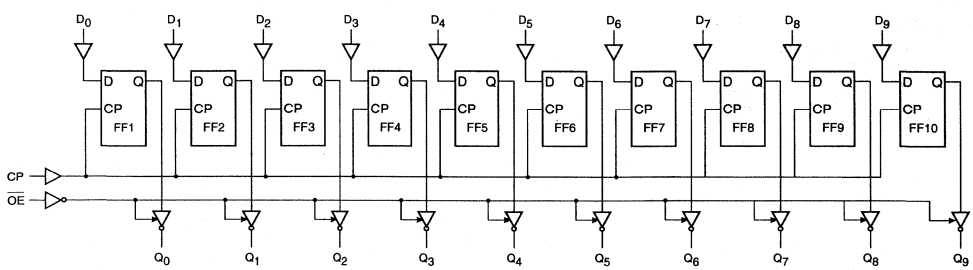


Fig.5 Logic diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	CP	D_n		Q_0 to Q_9
load and read register	L L	↑ ↑	l h	L H	L H
load register and disable outputs	H H	↑ ↑	l h	L H	Z Z
hold	L	H or L	X	NC	NC

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
Z = high impedance OFF-state
↑ = LOW-to-HIGH clock transition
NC = no change

DC CHARACTERISTICS FOR 74LVC821

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74LVC821

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		−40 to +85				V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	– – –	– – –	– 8.0 7.0	ns	1.2 2.7 3.0 to 3.6	Fig.6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n	– – –	– – –	– 8.5 8.0	ns	1.2 2.7 3.0 to 3.6	Fig.7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n	– – –	– – –	– 7.5 7.0	ns	1.2 2.7 3.0 to 3.6	Fig.7
t_W	clock pulse width HIGH or LOW	5.0 5.0	3.0 3.0*	– –	ns	2.7 3.0 to 3.6	Fig.6
t_{su}	set-up time D_n to CP	1.0 1.0	0.3 0.3*	– –	ns	2.7 3.0 to 3.6	Fig.8
t_h	hold time D_n to CP	1.0 1.0	−0.2 −0.2*	– –	ns	2.7 3.0 to 3.6	Fig.8
f_{max}	maximum clock pulse frequency	– 75	– 150*	– –	MHz	2.7 3.0 to 3.6	Fig.6

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

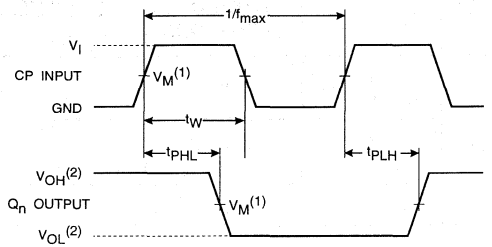


Fig.6 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width and the maximum clock pulse frequency.

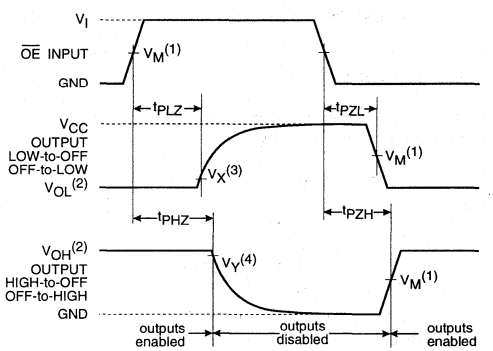


Fig.7 Waveforms showing the 3-state enable and disable times.

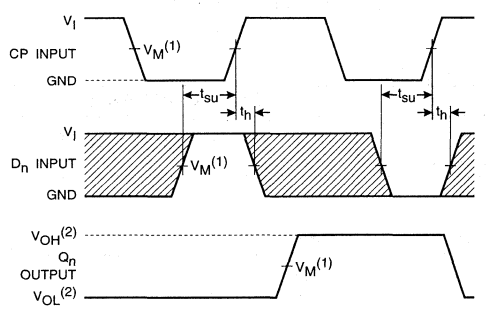
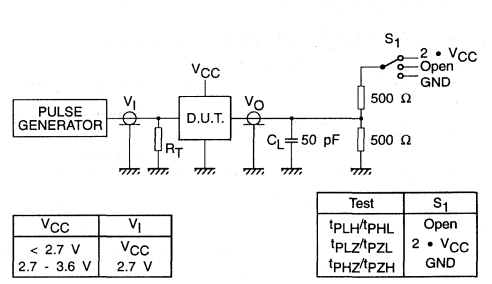


Fig.8 Waveforms showing the data set-up and hold times for the D_n input to the CP input.

Note to Fig.8:

The shaded areas indicate when the input is permitted to change for predictable output performance.



VCC	VI
< 2.7 V	VCC
2.7 - 3.6 V	2.7 V

Test	S1
tPLH/tPHL	Open
tPLZ/tPZL	2 • VCC
tPHZ/tPZH	GND

Fig.9 Load circuitry for switching times.

Notes:

(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

9-Bit D-type flip-flop; positive-edge trigger; 3-state — 74LVC823

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **Inputs accept voltages upto 5.5 V**
- **CMOS low power consumption**
- **Direct interface with TTL levels**
- **8-bit positive edge-triggered register**
- **Independent register and 3-state buffer operation**
- **Flow-through pin-out architecture**
- **Output drive capability 50 Ω transmission lines @ 85 °C**

DESCRIPTION

The 74LVC823 is a low-power, low-voltage, high-performance, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment.
The 74LVC823 is a 9-bit D-type flip-flop with common clock (CP), Clock Enable ($\overline{CE}$), Master Reset ($\overline{MR}$) and 3-state outputs for bus oriented applications.
The nine flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition, provided $\overline{CE}$ is LOW. When $\overline{CE}$ is HIGH the flip-flops hold their data.
A low on $\overline{MR}$ resets all flip-flops.

When $\overline{OE}$ is LOW, the contents of the nine flip-flops is available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 50 pF; V_{CC} = 3.3 V	4.8	ns
f_{max}	maximum clock frequency		150	MHz
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	28	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC823D	24	SO	plastic	SO24/SOT137
74LVC823DB	24	SSOP	plastic	SSOP24/SOT340
74LVC823PW	24	TSSOP	plastic	TSSOP24/SOT355

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9, 10	D_0 to D_8	data inputs
11	$\overline{MR}$	mater reset (active Low)
12	GND	ground (0 V)
13	CP	clock pulse (active rising)
14	$\overline{CE}$	clock enable (active Low)
23, 22, 21, 20, 19, 18, 17, 16, 15	Q_0 to Q_8	3-state flip-flop outputs
24	V_{CC}	positive supply voltage

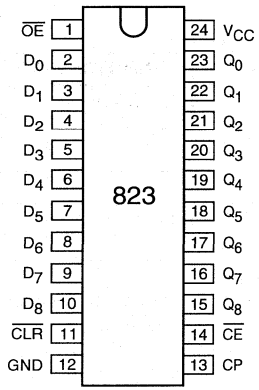


Fig.1 Pin configuration.

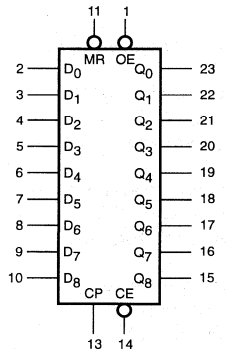


Fig.2 Logic symbol.

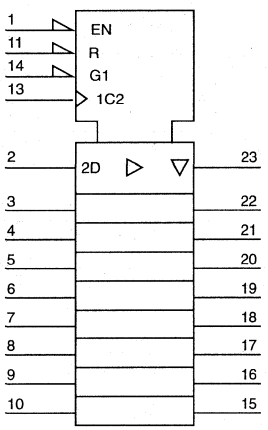


Fig3. IEC logic symbol.

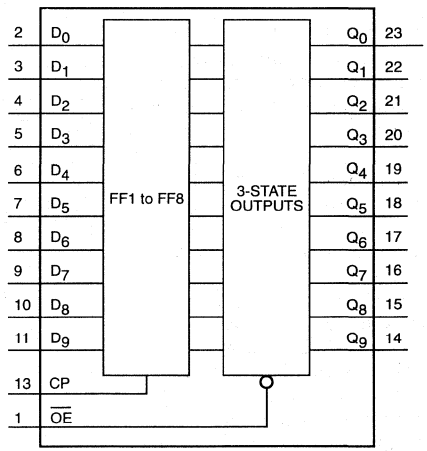


Fig.4 Functional diagram.

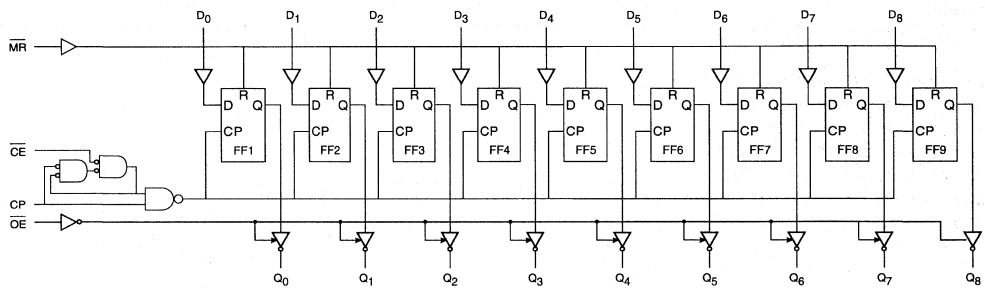


Fig.5 Logic diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS					INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	$\overline{MR}$	$\overline{CE}$	CP	D_n		Q_0 to Q_8
clear	L	L	X	X	X	L	L
load and read register	L	H	L	↑	l	L	L
	L	H	L	↑	h	H	H
load register and disable outputs	H	H	L	X	l	L	Z
	H	H	L	X	h	H	Z
hold	L	H	H	NC	X	NC	NC

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
Z = high impedance OFF-state
↑ = LOW-to-HIGH clock transition
NC = no change

DC CHARACTERISTICS FOR 74LVC823

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74LVC823

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		−40 to +85				V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	–	–	–	ns	1.2	Fig.6
		–	–	9.5		2.7	
		–	–	8.5		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n	–	–	–	ns	1.2	Fig.7
		–	–	8.5		2.7	
		–	–	8.0		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n	–	–	–	ns	1.2	Fig.7
		–	–	7.5		2.7	
		–	–	7.0		3.0 to 3.6	
t_w	clock pulse width HIGH or LOW	–	3.0	–	ns	2.7	Fig.6
		–	3.0*	–		3.0 to 3.6	
t_{su}	set-up time D_n to CP	1.0	0.3	–	ns	2.7	Fig.8
		1.0	0.3*	–		3.0 to 3.6	
t_h	hold time D_n to CP	1.0	−0.2	–	ns	2.7	Fig.8
		1.0	−0.2*	–		3.0 to 3.6	
f_{max}	maximum clock pulse frequency	–	–	–	MHz	2.7	Fig.6
		75	150*	–		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

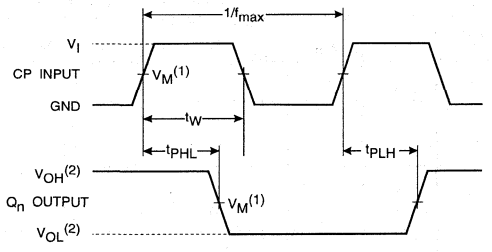


Fig.6 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width and the maximum clock pulse frequency.

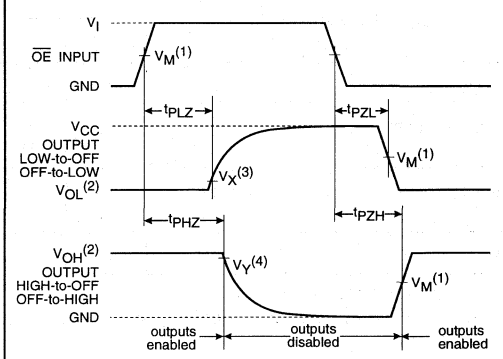


Fig.7 Waveforms showing the 3-state enable and disable times.

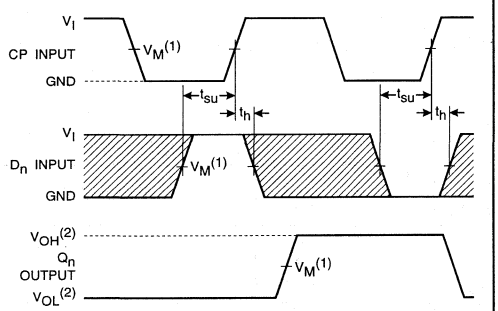
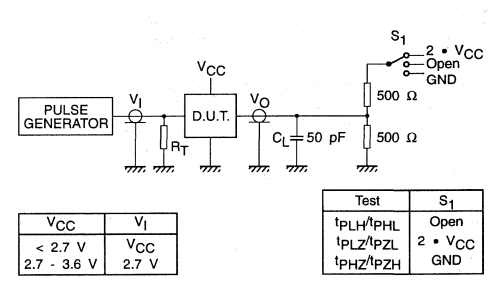


Fig.8 Waveforms showing the data set-up and hold times for the D_n input to the CP input.

Note to Fig.8:

The shaded areas indicate when the input is permitted to change for predictable output performance.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.9 Load circuitry for switching times.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

10-Bit buffer/line driver; 3-state | 74LVC827

FEATURES

- **Optimized for Low Voltage applications: 1.0 to 3.6 V**
- **Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V**
- **Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.**
- **Non-inverting outputs**
- **Output capability: bus driver**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74LVC821 is a low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74LVC827 is an 10-bit buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $\overline{OE}1$ and $\overline{OE}2$.
A HIGH on $\overline{OE}n$ causes the outputs to assume a high impedance OFF-state.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}_1$	$\overline{OE}_2$	nA	nY
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n to Y_n	C_L = 15 pF V_{CC} = 3.3 V	10	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	37	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC827D	24	SO	plastic	SO24/SOT137
74LVC827DB	24	SSOP	plastic	SSOP24/SOT340
74LVC827PW	24	TSSOP	plastic	TSSOP24/SOT355

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 13	$\overline{OE}_1$, $\overline{OE}_2$	output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9, 10, 11	A_0 to A_9	data inputs
10	GND	ground (0 V)
23, 22, 21, 20, 19, 18, 17, 16, 15, 14	Y_0 to Y_9	bus outputs
20	V_{CC}	positive supply voltage

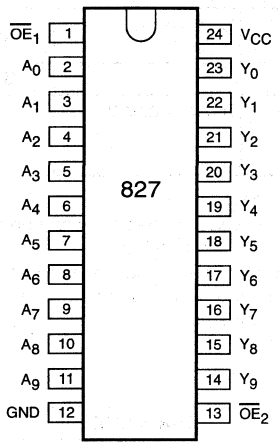


Fig.1 Pin configuration.

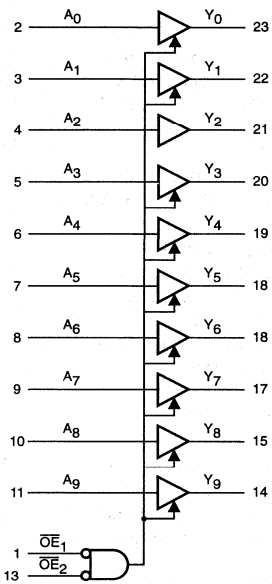


Fig.2 Logic symbol.

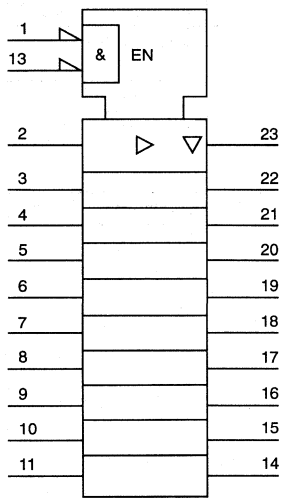


Fig.3 IEC logic symbol.

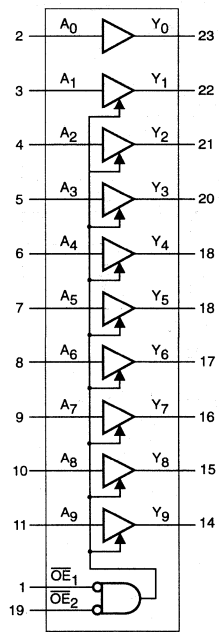


Fig.4 Functional diagram.

DC CHARACTERISTICS FOR 74LVC827

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".
Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LVC827

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C) −40 to +85			UNIT	TEST CONDITIONS	
		MIN.	TYP.	MAX.		V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay	–	–	–	ns	1.2	Fig. 5
	$1A_n$ to $1Y_n$;	–	–	8.0		2.7	
	$2A_n$ to $2Y_n$	–	–	7.0		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time	–	–	–	ns	1.2	Figs 6
	$1\overline{OE}$ to $1Y_n$;	–	–	9.0		2.7	
	$2\overline{OE}$ to $2Y_n$	–	–	8.5		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time	–	–	–	ns	1.2	Figs 6
	$1\overline{OE}$ to $1Y_n$;	–	–	8.0		2.7	
	$2\overline{OE}$ to $2Y_n$	–	–	7.5		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

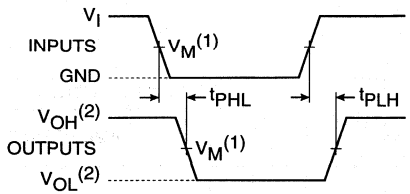


Fig.5 Waveforms showing the input (A_n) to output (Y_n) propagation delays.

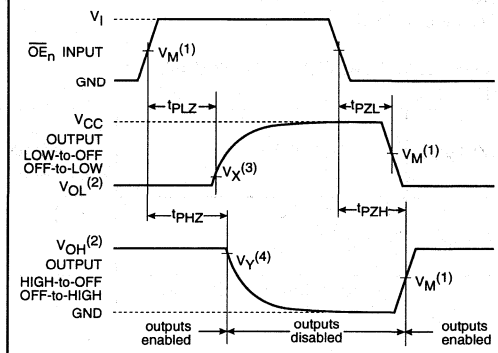
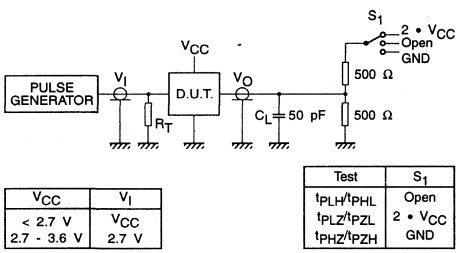


Fig.6 Waveforms showing the 3-state enable and disable times.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.7 Load circuitry for switching times.

Notes:

(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **Inputs accept voltages upto 5.5 V**
- **CMOS low power consumption**
- **Direct interface with TTL levels**
- **Flow-through pin-out architecture**
- **Output drive capability 50 Ω transmission lines @ 85 °C**

DESCRIPTION

The 74LVC841 is a low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment.

The 74LVC841 is an 10-bit transparent latch featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. A latch enable ($\overline{LE}$) input and an output enable ($\overline{OE}$) input are common to all internal latches.

The '841' consists of ten transparent latches with 3-state true outputs. When LE is HIGH, data at the D_n inputs enters the latches. In this condition the latches are transparent, i.e. a latch output will change each time its corresponding D-input changes. When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the ten latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n; LE to Q_n	C_L = 50 pF; V_{CC} = 3.3 V	4.3 4.6	ns
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	23	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC841D	24	SO	plastic	SO24/SOT137
74LVC841DB	24	SSOP	plastic	SSOP24/SOT340
74LVC841PW	24	TSSOP	plastic	TSSOP24/SOT355

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9, 10, 11	D_0 to D_9	data inputs
23, 22, 21, 20, 19, 18, 17, 16, 15, 14	Q_0 to Q_9	3-state latch outputs
12	GND	ground (0 V)
13	LE	latch enable input (active HIGH)
24	V_{CC}	positive supply voltage

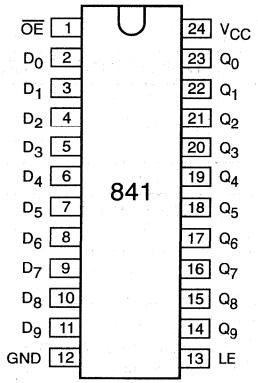


Fig.1 Pin configuration.

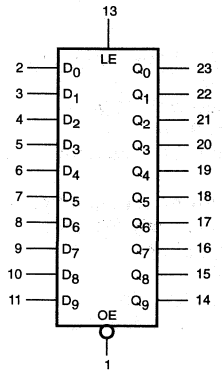


Fig.2 Logic symbol.

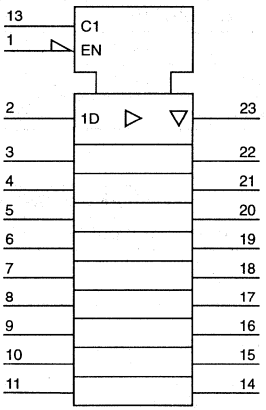


Fig3. IEC logic symbol.

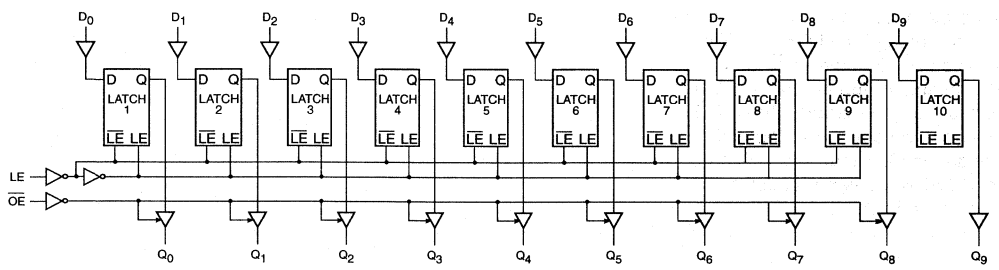


Fig.4 Logic diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$\overline{OE}$	LE	D_n		Q_0 to Q_8
enable and read register (transparent mode)	L L	H H	L H	L H	L H
latch and read register	L L	↓ ↓	l h	L H	L H
latch register and disable outputs	H H	X X	l h	L H	Z Z
hold	L	L	X	NC	NC

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
X = don't care
Z = high impedance OFF-state
NC = no change

DC CHARACTERISTICS FOR 74LVC841

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74LVC841

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		−40 to +85				V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n	– 1.5 1.5	– – –	– 8.5 7.5	ns	1.2 2.7 3.0 to 3.6	Fig.5
t_{PHL}/t_{PLH}	propagation delay LE to Q_n	– 1.5 1.5	– – –	– 9.0 8.0	ns	1.2 2.7 3.0 to 3.6	Fig.6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n	– 1.5 1.5	– – –	– 8.5 8.0	ns	1.2 2.7 3.0 to 3.6	Fig.7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n	– 1.5 1.5	– – –	– 7.5 7.0	ns	1.2 2.7 3.0 to 3.6	Fig.7
t_W	LE pulse width HIGH	– –	3.0 3.0*	– –	ns	2.7 3.0 to 3.6	Fig.8
t_{su}	set-up time D_n to LE	1.0 1.0	0.2 0.2*	– –	ns	2.7 3.0 to 3.6	Fig.8
t_h	hold time D_n to LE	1.0 1.0	0 0*	– –	ns	2.7 3.0 to 3.6	Fig.8

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

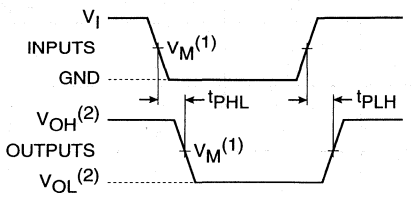


Fig.5 Waveforms showing the input (D_n) to output (Q_n) propagation delays.

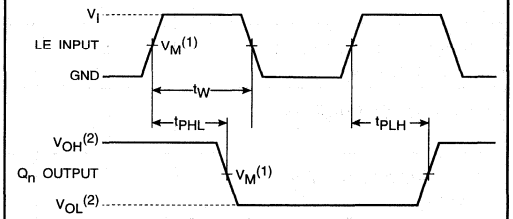


Fig.6 Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output (Q_n) propagation delays.

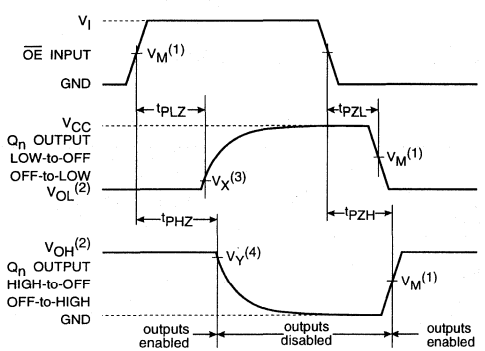


Fig.7 Waveforms showing the 3-state enable and disable times

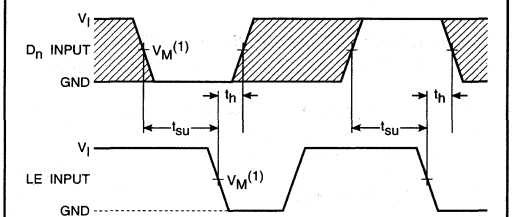
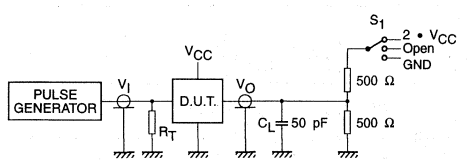


Fig.8 Waveforms showing the data set-up and hold times for the D_n input to the LE input.

Note to Fig.8:

The shaded areas indicate when the input is permitted to change for predictable output performance.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.9 Load circuitry for switching times.

Notes:

(1) V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
V_M = 0.5 · V_{CC} at V_{CC} < 2.7 V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

(3) $V_X = V_{OL}$ + 0.3 V at $V_{CC} \geq$ 2.7 V
$V_X = V_{OL}$ + 0.1 · V_{CC} at V_{CC} < 2.7 V

(4) $V_Y = V_{OH}$ − 0.3 V at $V_{CC} \geq$ 2.7 V
$V_Y = V_{OH}$ − 0.1 · V_{CC} at V_{CC} < 2.7 V

Octal registered transceiver; 3-state — 74LVC2952

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **CMOS low power consumption**
- **Direct interface with TTL levels.**
- **Inputs accept voltages upto 5.5 V**
- **Flow-through pin-out architecture**
- **3-state outputs**
- **Direct interface with TTL levels**
- **Output drive capability 50Ω transmission lines @ 85°C**

DESCRIPTION

The 74LVC2952 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74LVC2952 is an octal non-inverting registered transceiver. Two 8-bit back to back registers store data flowing in both directions between two bi-directional busses. Data applied to the inputs is entered and stored on the rising edge of the clock (CP_{nn}) provided that the clock enable ($\overline{CE}_{nn}$) is LOW. The data is then present at the 3-state output buffers, but is only accessible when the output enable input ($\overline{OE}_{nn}$) is LOW. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

The '952' is identical to the '953' but has non-inverting outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay CP_{nn} to A_n, B_n	C_L = 50 pF; V_{CC} = 3.3 V	3.2	ns
f_{max}	maximum clock frequency		350	MHz
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	35	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC2952D	24	SO	plastic	SO24/SOT137A
74LVC2952DB	24	SSOP	plastic	SSOP24/SOT340
74LVC2952PW	24	TSSOP	plastic	TSSOP24/SOT355

PINNING

PIN	SYMBOL	NAME AND FUNCTION
8, 7, 6, 5, 4, 3, 2, 1	B_0 to B_7	B data inputs/outputs
6, 7, 8, 9	GND	ground (0 V)
9, 15	$\overline{OE}_{AB}$, $\overline{OE}_{BA}$	output enable inputs (active LOW)
10, 14	CP_{AB}, CP_{BA}	clock inputs
11, 13	$\overline{CE}_{AB}$, $\overline{CE}_{BA}$	clock enable inputs
16, 17, 18, 19, 20, 21, 22, 23	A_0 to A_7	A data inputs/outputs
24	V_{CC}	positive supply voltage

FUNCTION TABLE for register A_n or B_n

INPUTS			INTERNAL Q	OPERATING MODE
A_n or B_n	CP_{nn}	$\overline{CE}_{nn}$		
X	X	H	NC	Hold data
L	↑	L	L	Load data
H	↑	L	H	Load data

H = HIGH voltage level
L = LOW voltage level
↑ = Low-to-High transition

FUNCTION TABLE for output enable

INPUTS	INTERNAL Q	A_n or B_n OUTPUTS	OPERATING MODE
$\overline{OE}_{nn}$			
H	X	Z	disable outputs
L	L	L	enable outputs
L	H	H	enable outputs

NC = no change
X = don't care
Z = high impedance OFF-state

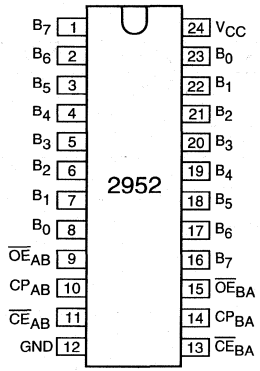


Fig.1 Pin configuration.

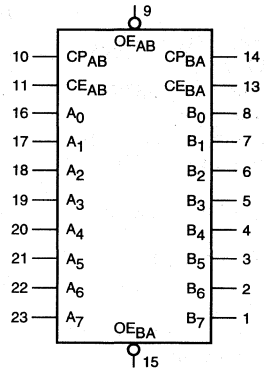


Fig.2 Logic symbol.

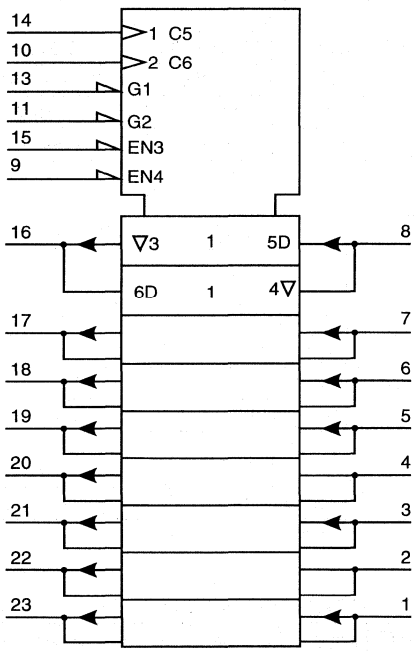


Fig.3 IEC logic symbol.

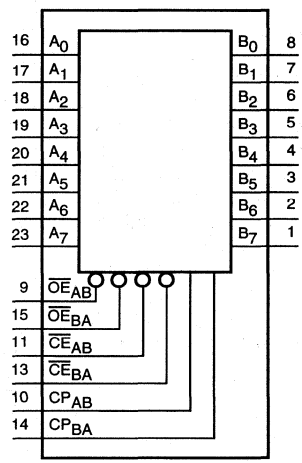


Fig.4 Functional diagram.

DC CHARACTERISTICS FOR 74LVC2952

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74LVC2952

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		−40 to +85				V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t_{PHL}/t_{PLH}	propagation delay CP_{BA}, CP_{AB} to A_n, B_n	– – –	– – 3.2*	– 10 9.0	ns	1.2 2.7 3.0 to 3.6	Fig.5
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_{BA}$, $\overline{OE}_{AB}$ to A_n, B_n	– – –	– – –	– 11 10	ns	1.2 2.7 3.0 to 3.6	Fig.7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_{BA}$, $\overline{OE}_{AB}$ to A_n, B_n	– – –	– – –	– 10 9.0	ns	1.2 2.7 3.0 to 3.6	Fig.7
t_W	CP_{AB}, CP_{BA} pulse width, HIGH or LOW	3.0 3.0	– –	– –	ns	2.7 3.0 to 3.6	Fig.5
t_{su}	set–up time, HIGH or LOW A_n, B_n to CP_{AB}, CP_{BA}	−5.0 −5.0	– –	– –	ns	2.7 3.0 to 3.6	Fig.6
t_{su}	set–up time, HIGH or LOW $\overline{CE}_{AB}$, $\overline{CE}_{BA}$ to CP_{AB}, CP_{BA}	4.0 4.0	– –	– –	ns	2.7 3.0 to 3.6	Fig.6
t_h	hold time A_n, B_n to CP_{AB}, CP_{BA}	0 0	– –	– –	ns	2.7 3.0 to 3.6	Fig.6
t_h	hold time $\overline{CE}_{AB}$, $\overline{CE}_{BA}$ to CP_{AB}, CP_{BA}	3.0 3.0	– –	– –	ns	2.7 3.0 to 3.6	Fig.6
f_{max}	maximum clock pulse frequency	145 150	– –	– –	MHz	2.0 3.0 to 3.6	Fig.5

Notes: All typical values are measured at T_{amb} = 25 °C.
* Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

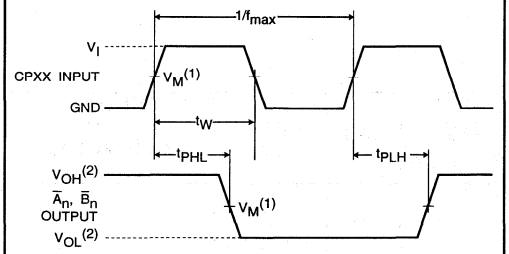


Fig. 5 Waveforms showing the clock input (CP_{BA}, CP_{AB}) to output ($\overline{B}_n$, $\overline{A}_n$) propagation delays, the clock pulse width and the maximum clock pulse frequency.

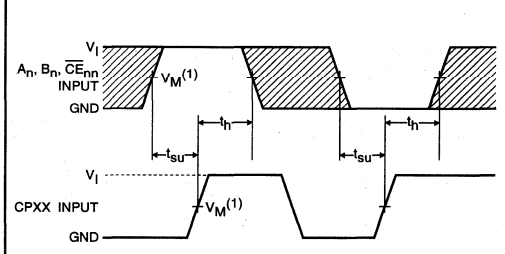


Fig.6 Waveforms showing the set-up and hold times for the A_n, B_n and $\overline{CE}_{nn}$ inputs.

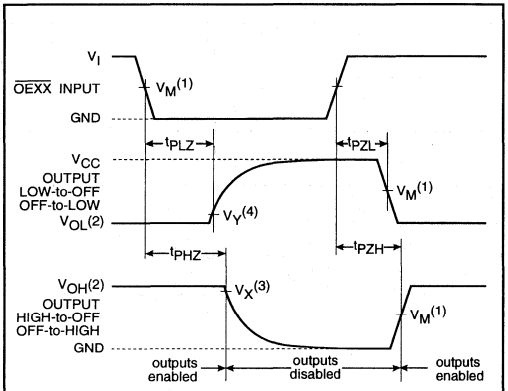


Fig.7 Waveforms showing the 3-state enable and disable times.

Note to Fig.6

The shaded areas indicate when the input is permitted to change for predictable output performance.

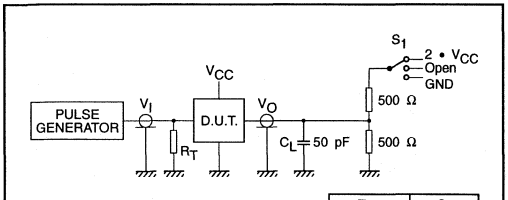
Notes:

(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.8 Load circuitry for switching times.

Octal dual supply translating transceiver; 3-state 74LVC4245

FEATURES

- **Wide supply voltage range**
  3 Volt port: 1.2 to 3.6 V
  5 Volt port: 1.2 to 5.5 V
- **In accordance with JEDEC standard no. 8-1A.**
- **Control inputs accept voltages upto 5.5 V**
- **CMOS low power consumption**
- **Direct interface with TTL levels**

DESCRIPTION

The 74LVC4245 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74LVC4245 is an octal dual supply translating transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions.
It is designed to interface between a 3 V bus and 5 V bus in a mixed 3 V/5 V supply environment.

The '4245' features an output enable ($\overline{OE}$) input for easy cascading and a send/receive (DIR) input for direction control. $\overline{OE}$ controls the outputs so that the buses are effectivly isolated.

In suspend mode, when V_{CCA} is zero, there will be no current flow from one supply to the other supply. The A-outputs must be set 3-state and the voltage on the A bus must be smaller then V_{diode} (typ. 0.7V). $V_{CCA} \geq V_{CCB}$ (except in suspend mode).

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA to nB nB to nA	C_L = 50 pF V_{CCA} = 5.0 V V_{CCB} = 3.3 V	 4.3 4.3	ns
C_I	input capacitance		5.0	pF
$C_{I/O}$	input/output capacitance		10	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	t.b.f.	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC4245D	24	SO	plastic	SO24/SOT137A
74LVC4245DB	24	SSOP	plastic	SSOP24/SOT340
74LVC4245PW	24	TSSOP	plastic	TSSOP24/SOT355

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	V_{CCA}	positive supply voltage (5 V bus)
2	DIR	direction control
3, 4, 5, 6, 7, 8, 9, 10	A_0 to A_7	data inputs
11, 12, 13	GND	GND
14, 15, 16, 17, 18, 19, 20, 21	B_7 to B_0	data inputs
22	$\overline{OE}$	output enable input (active LOW)
23, 24	V_{CCB}	positive supply voltage (3 V bus)

FUNCTION TABLE

INPUTS		OUTPUTS	
$\overline{OE}$	DIR	A_n	B_n
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

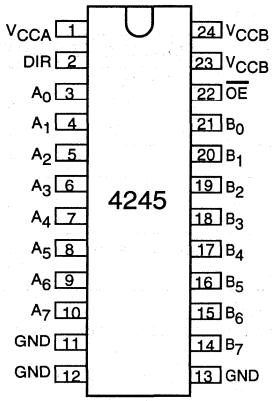


Fig.1 Pin configuration.

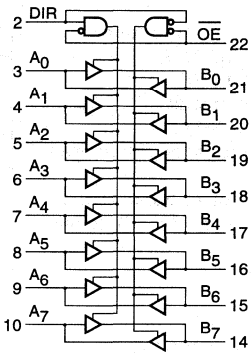


Fig.2 Logic symbol.

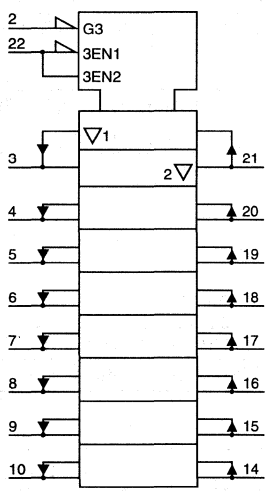


Fig.3 IEC Logic symbol.

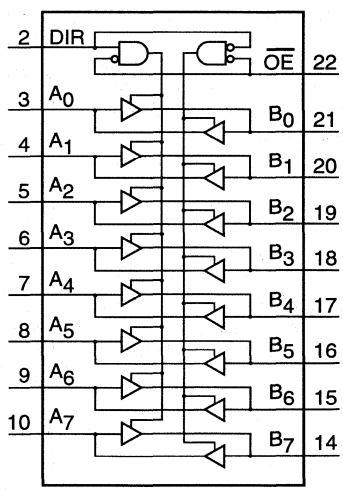


Fig.4 Functional diagram

RECOMMENDED OPERATING CONDITIONS FOR THE 74LVC4245

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CCA}	DC supply voltage 5 V port	1.2	5.5	V	see fig.8
V_{CCB}	DC supply voltage 3 V port	1.2	3.6	V	see fig.8
V_I	DC input voltage range (control inputs)	0	5.5	V	
$V_{I/O}$	DC input voltage range for I/Os	0	V_{CC}	V	
T_{amb}	operating ambient temperature range in free air	−40	+85	°C	see DC and AC characteristics per device
t_r, t_f	input rise and fall times	0 0 0 0	20 10 20 10	ns/V	V_{CCB} = 2.7 to 3.0 V V_{CCB} = 3.0 to 3.6 V V_{CCA} 3.0 to 4.5 V V_{CCA} 4.5 to 5.5 V

LIMITING VALUES FOR THE 74LVC4245 (Note 1)

In accordance with the Absolute Maximum Rating System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CCA}	DC supply voltage 5 V port	−0.5	+6.5	V	
V_{CCB}	DC supply voltage 3 V port	−0.5	+4.6	V	
I_{IK}	DC input diode current	–	−50	mA	$V_I < 0$
V_I	DC input voltage	−0.5	+5.5	V	note 2
$V_{I/O}$	DC input voltage range for I/Os	−0.5	V_{CC} + 0.5	V	
I_{OK}	DC output diode current	–	±50	mA	$V_O > V_{CC}$ or $V_O < 0$
V_O	DC output voltage	−0.5	V_{CC} + 0.5	V	note 2
I_O	DC output source or sink current	–	±50	mA	V_O = 0 to V_{CC}
I_{GND}, I_{CC}	DC V_{CC} or GND current	–	±100	mA	
T_{stg}	storage temperature range	−60	+150	°C	
P_{tot}	See introduction, "Package thermal data"	–	–	mW	

Notes to the limiting values

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those under 'recommended operating conditions' is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS FOR THE 74LVC4245

Over recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C) −40 to +85			UNIT	TEST CONDITIONS		
		MIN.	TYP.	MAX.		$V_{CCA/B}$ (V)	V_I	OTHER
V_{IH}	HIGH level input voltage (3 V port)	2.0	–	–	V	2.7 to 3.6		
V_{IH}	HIGH level input voltage (5 V port)	2.0	–	–	V	4.5 to 5.5		
V_{IL}	LOW level input voltage (3 V port)	–	–	0.8	V	2.7 to 3.6		
V_{IL}	LOW level input voltage (5 V port)	–	–	0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage (3 V port)	V_{CC} − 0.6 V_{CC} − 0.2 V_{CC} − 1.0	– V_{CC} –	– – –	V	2.7 3.0 3.0	V_{IH}	I_O = −12 mA I_O = −100 µA I_O = −24 mA
V_{OH}	HIGH level output voltage (5 V port)	V_{CC} − 0.2 V_{CC} − 0.8	V_{CC} –	– –	V	4.5 4.5	V_{IH}	I_O = −100 µA I_O = −24 mA
V_{OL}	LOW level output voltage (3 V port)	– – –	– – –	0.40 0.20 0.55	V	2.7 3.0 3.0	V_{IL}	I_O = 12 mA I_O = 100 µA I_O = 24 mA
V_{OL}	LOW level output voltage (5 V port)	– – –	– – –	0.40 0.20 0.55	V	4.5 4.5 4.5	V_{IL}	I_O = 12 mA I_O = 100 µA I_O = 24 mA
I_I	input leakage current (control inputs)	–	±0.1	±5	µA	3.6	5.5 V or GND	not for I/O pins
I_{IHZ}/I_{ILZ}	input current for common I/O pins (3 V port)	–	±0.1	±15	µA	3.6	V_{CC} or GND	
I_{IHZ}/I_{ILZ}	input current for common I/O pins (5 V port)	–	±0.1	±15	µA	5.5	V_{CC} or GND	
I_{OZ}	3-state output OFF-state current (3 V port)	–	0.1	±10	µA	3.6	V_{IH} or V_{IL}	V_O = V_{CC} or GND
I_{OZ}	3-state output OFF-state current (5 V port)	–	0.1	±10	µA	5.5	V_{IH} or V_{IL}	V_O = V_{CC} or GND
I_{CC}	quiescent supply current (3 V port)	–	0.1	20	µA	3.6	V_{CC} or GND	I_O = 0
I_{CC}	quiescent supply current (5 V port)	–	t.b.f.	t.b.f.	µA	5.5	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current given per input pin (3 V port)	–	5	500	µA	2.7 to 3.6	V_{CC} − 0.6 V	I_O = 0
ΔI_{CC}	additional quiescent supply current given per input pin (5 V port)	–	5	500	µA	4.5 to 5.5	V_{CC} − 2.1 V	I_O = 0

Note: All typical values are measured at V_{CCA} = 5.0 V, V_{CCB} = 3.3 V and T_{amb} = 25 °C.

DC CHARACTERISTICS FOR 74LVC4245

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74LVC4245

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C) -40 to +85			UNIT	TEST CONDITIONS		
		MIN.	TYP.	MAX.		V_{CCA} (V)	V_{CCB} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay A_n to B_n	1.5 1.5	4.8 4.3*	7.5 7.0	ns	4.5 to 5.5 4.5 to 5.5	2.7 3.0 to 3.6	Fig. 5
t_{PHL}/t_{PLH}	propagation delay B_n to A_n	1.5 1.5	4.8 4.3*	7.5 7.0	ns	4.5 to 5.5 4.5 to 5.5	2.7 3.0 to 3.6	Fig. 5
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to A_n	1.5 1.5	6.5 5.5*	10.0 9.0	ns	4.5 to 5.5 4.5 to 5.5	2.7 3.0 to 3.6	Figs 6, 7
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to B_n	1.5 1.5	5.5 4.8*	8.0 7.5	ns	4.5 to 5.5 4.5 to 5.5	2.7 3.0 to 3.6	Figs 6, 7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to A_n	1.5 1.5	5.7 5.3*	8.0 7.5	ns	4.5 to 5.5 4.5 to 5.5	2.7 3.0 to 3.6	Figs 6, 7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to B_n	1.5 1.5	5.7 5.3*	8.0 7.5	ns	4.5 to 5.5 4.5 to 5.5	2.7 3.0 to 3.6	Figs 6, 7

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CCA} = 5.0$ V and $V_{CCB} = 3.3$ V.

AC WAVEFORMS

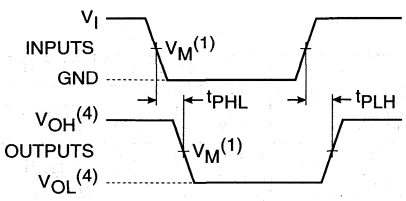


Fig. 5 Waveforms showing the input (A_n, B_n) to output (B_n, A_n) propagation delays and the output transition times.

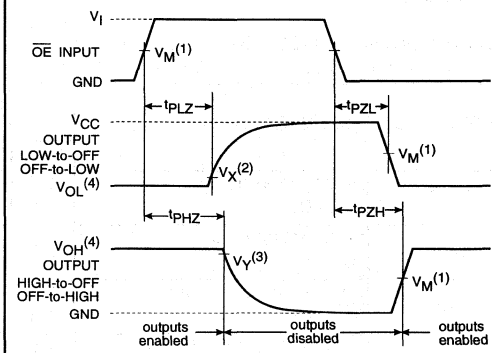
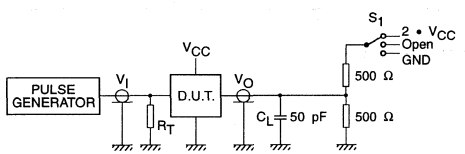


Fig.6 Waveforms showing the 3-state enable and disable times.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.7 Load circuitry for switching times.

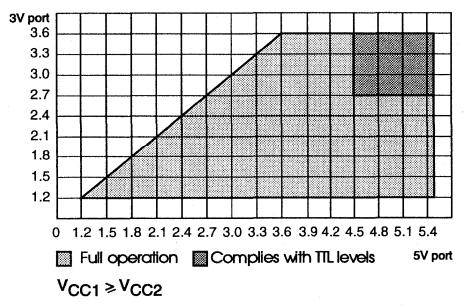


Fig.8 Supply operating area

Notes:

(1) $V_M = 0.5 \cdot V_{CCB}$ at $V_{CCB} < 2.7$ V
$V_M = 1.5$ V at $V_{CCB} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CCA}$

(2) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(3) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

DEVICE DATA

HLL

Octal buffer/line driver; 3-state; inverting — 74HL33240

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with the JEDEC 3.3 V ±0.3 V supply**
- **CMOS low power consumption**
- **Flow-through pin-out architecture**
- **Low inductance, multiple centre power and ground pins for minimum noise and ground bounce**
- **3-state outputs**
- **Direct interface with TTL levels**
- **5 V to 3.3 V level shifting**

DESCRIPTION

The 74HL33240 is a high-performance, low-power, low-voltage, Si-gate CMOS device superior to most advanced CMOS compatible TTL families.

The 74HL33240 is an octal inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state. The "240" is identical to the "244" but has inverting outputs.

FUNCTION TABLE

INPUTS		OUTPUT
$n\overline{OE}$	nA_n	nY_n
L	L	H
L	H	L
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	C_L = 50 pF; V_{CC} = 3.3 V	2.1	ns
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	35	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74HL33240D	24	SO	plastic	SO24/SOT137A
74HL33240DB	24	SSOP	plastic	SSOP24/SOT340

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4	$1Y_0$ to $1Y_3$	bus outputs
5, 6, 7, 8	GND	ground (0 V)
9, 10, 11, 12	$2Y_0$ to $2Y_3$	bus outputs
13	$2\overline{OE}$	output enable input (active LOW)
14, 15, 16, 17	$2A_3$ to $2A_0$	data inputs
18, 19	V_{CC}	positive supply voltage
20, 21, 22, 23	$1A_3$ to $1A_0$	data inputs
24	$1\overline{OE}$	output enable input (active LOW)

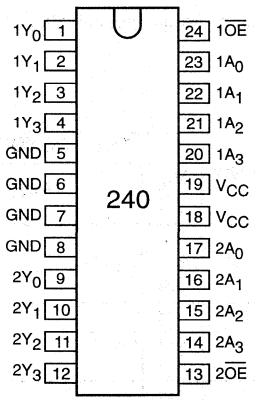


Fig.1 Pin configuration.

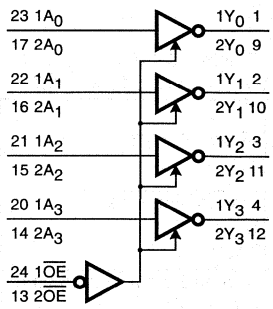


Fig.2 Logic symbol.

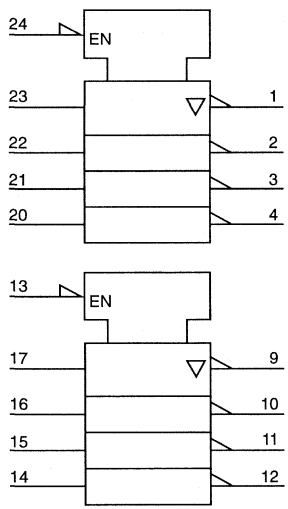


Fig.3 IEC logic symbol.

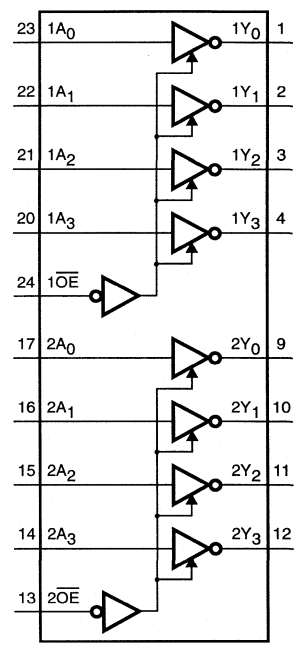


Fig.4 Functional diagram.

DC CHARACTERISTICS FOR 74HL33240

For the DC characteristics see chapter "HLL family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74HL33240

GND = 0 V; $t_r = t_f$ = 2.0 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)				UNIT	TEST CONDITIONS	
		+25		−40 to +85			V_{CC} (V)	WAVEFORMS
		MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay	–	14.0	–	16.0	ns	1.2	Fig. 5
	$1A_n$ to $1Y_n$;	–	5.3	–	6.0		2.0	
	$2A_n$ to $2Y_n$	–	3.5	–	4.0		3.0	
t_{PZH}/t_{PZL}	3–state output enable time	–	15.6	–	17.6	ns	1.2	Fig. 6, 7
	$1\overline{OE}$ to $1Y_n$;	–	5.9	–	6.6		2.0	
	$2\overline{OE}$ to $2Y_n$	–	3.9	–	4.4		3.0	
t_{PHZ}/t_{PLZ}	3–state output disable time	–	12.3	–	13.9	ns	1.2	Fig. 6, 7
	$1\overline{OE}$ to $1Y_n$;	–	5.4	–	6.0		2.0	
	$2\overline{OE}$ to $2Y_n$	–	4.0	–	4.4		3.0	

AC WAVEFORMS

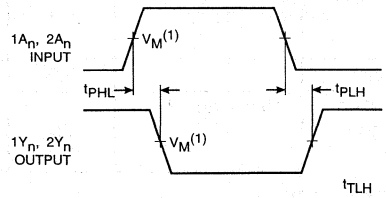


Fig. 5 Waveforms showing the input ($1A_n$, $2A_n$) to output ($1Y_n$, $2Y_n$) propagation delays and the output transition times.

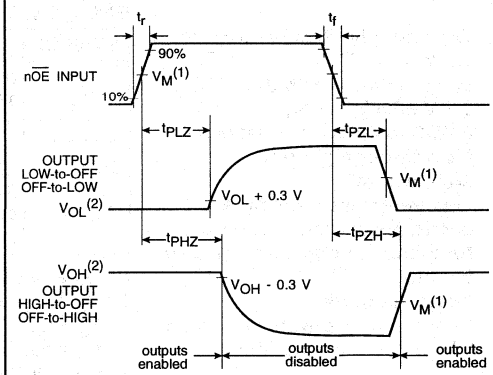


Fig.6 Waveforms showing the 3-state enable and disable times.

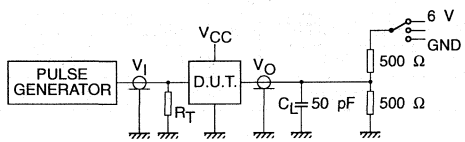


Fig. 7 Test conditions: Load circuitry for enable / disable times; switch set to 6 V for t_{PLZ}/t_{PZL}, switch set to GND for t_{PHZ}/t_{PZH} otherwise do not connect.

Notes: (1) $V_M = 0.6$ V at $V_{CC} = 1.2$ V.
$V_M = 1.0$ V at $V_{CC} = 2.0$ V.
$V_M = 1.5$ V at $V_{CC} = 3.0$ V.

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-state output load.

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with the JEDEC 3.3 V ±0.3 V supply**
- **CMOS low power consumption**
- **Flow-through pin-out architecture**
- **Low inductance, multiple centre power and ground pins for minimum noise and ground bounce**
- **3-state outputs**
- **Direct interface with TTL levels**
- **5 V to 3.3 V level shifting**

DESCRIPTION

The 74HL33241 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74HL33241 is an octal non-inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $1\overline{OE}$ and 2OE.

FUNCTION TABLES

INPUTS		OUTPUT
$1\overline{OE}$	$1A_n$	$1Y_n$
L	L	L
L	H	H
H	X	Z

INPUTS		OUTPUT
2OE	$2A_n$	$2Y_n$
H	L	L
H	H	H
L	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	C_L = 15 pF; V_{CC} = 3.3 V	2.1	ns
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	35	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PIN POSITION	MATERIAL	CODE
74HL33241D	24	SO	plastic	SOT137A
74HL33241DB	24	SSOP	plastic	SOT340

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4	$1Y_0$ to $1Y_3$	bus outputs
5, 6, 7, 8	GND	ground (0 V)
9, 10, 11, 12	$2Y_0$ to $2Y_3$	bus outputs
13	2OE	output enable input (active HIGH)
14, 15, 16, 17	$2A_3$ to $2A_0$	data inputs
18, 19	V_{CC}	positive power supply
20, 21, 22, 23	$1A_3$ to $1A_0$	data inputs
24	$1\overline{OE}$	output enable input (active LOW)

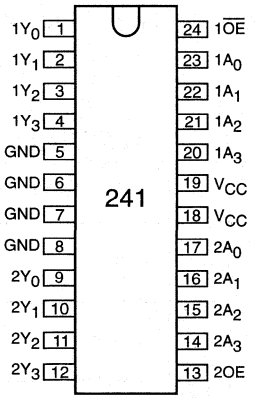


Fig.1 Pin configuration.

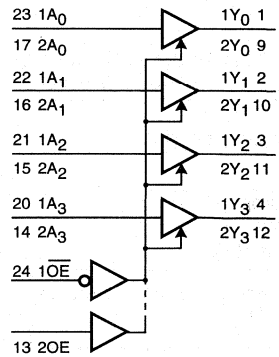


Fig.2 Logic symbol.

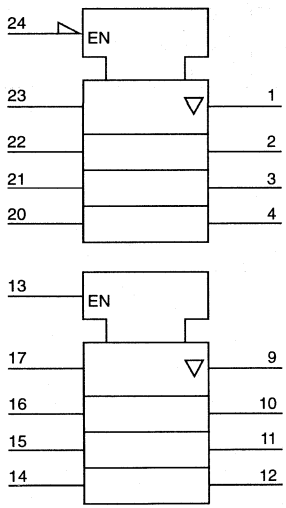


Fig.3 IEC logic symbol.

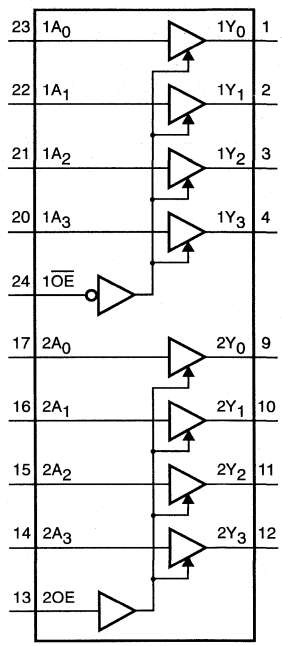


Fig.4 Functional diagram.

DC CHARACTERISTICS FOR 74HL33241

For the DC characteristics see chapter "HLL family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74HL33241

GND = 0 V; $t_r = t_f$ = 2.0 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)				UNIT	TEST CONDITIONS	
		+25		−40 to +85			V_{CC} (V)	WAVEFORMS
		MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	– – –	14.0 5.3 3.5	– – –	16.0 6.0 4.0	ns	1.2 2.0 3.0	Fig. 5
t_{PZH}/t_{PZL}	3-state output enable time $1\overline{OE}$ to $1Y_n$	– – –	15.6 5.9 3.9	– – –	17.6 6.6 4.4	ns	1.2 2.0 3.0	Fig. 6, 8
t_{PHZ}/t_{PLZ}	3-state output disable time $1\overline{OE}$ to 1Yn	– – –	12.3 5.4 4.0	– – –	13.9 6.0 4.4	ns	1.2 2.0 3.0	Fig. 6. 8
t_{PZH}/t_{PZL}	3-state output enable time 2OE to $2Y_n$	– – –	15.6 5.9 3.9	– – –	17.6 6.6 4.4	ns	1.2 2.0 3.0	Fig. 7, 8
t_{PHZ}/t_{PLZ}	3-state output disable time 2OE to $2Y_n$	– – –	12.3 5.4 4.0	– – –	13.9 6.0 4.4	ns	1.2 2.0 3.0	Fig. 7, 8

AC WAVEFORMS

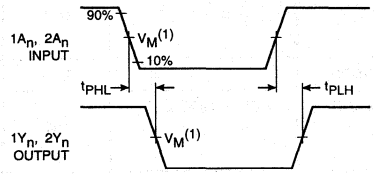


Fig. 5 Waveforms showing the input ($1A_n$, $2A_n$) to output ($1Y_n$, $2Y_n$) propagation delays and the output transition times.

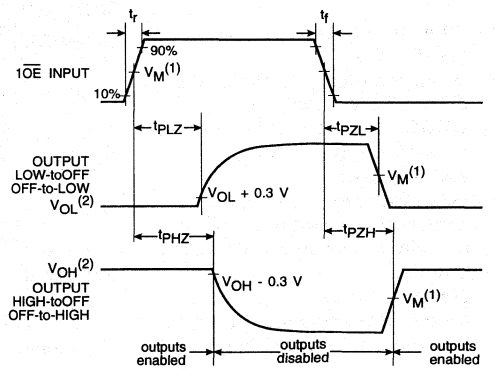


Fig.6 Waveforms showing the 3-state enable and disable times for input $1\overline{OE}$.

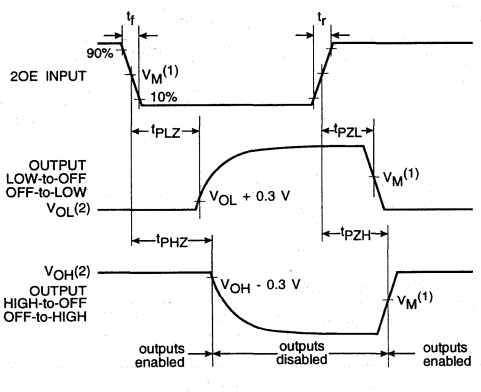


Fig.7 Waveforms showing the 3-state enable and disable times for input 2OE.

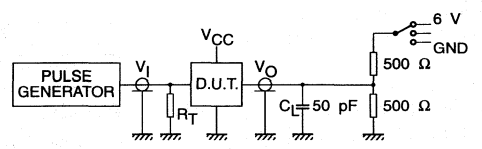


Fig. 8 Test conditions: Load circuitry for enable / disable times; switch set to 6 V for t_{PLZ}/t_{PZL}, switch set to GND for t_{PHZ}/t_{PZH} otherwise do not connect.

Notes: (1) V_M = 0.6 V at V_{CC}= 1.2 V.
V_M = 1.0 V at V_{CC}= 2.0 V.
V_M = 1.5 V at V_{CC}= 3.0 V.

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-state output load.

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with the JEDEC 3.3 V ±0.3 V supply**
- **CMOS low power consumption**
- **Flow-through pin-out architecture**
- **Low inductance, multiple centre power and ground pins for minimum noise and ground bounce**
- **3-state outputs**
- **Direct interface with TTL levels**
- **5 V to 3.3 V level shifting**

DESCRIPTION

The 74HL33244 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74HL33244 is an octal non-inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state. The "244" is identical to the "240" but has non-inverting outputs.

FUNCTION TABLE

INPUTS		OUTPUT
$n\overline{OE}$	nA_n	nY_n
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	C_L = 15 pF; V_{CC} = 3.3 V	2.1	ns
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	35	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PIN POSITION	MATERIAL	CODE
74HL33244D	24	SO	plastic	SOT137A
74HL33244DB	24	SSOP	plastic	SOT340

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4	$1Y_0$ to $1Y_3$	bus outputs
5, 6, 7, 8	GND	ground (0 V)
9, 10, 11, 12	$2Y_0$ to $2Y_3$	bus outputs
13	$2\overline{OE}$	output enable input (active LOW)
14, 15, 16, 17	$2A_3$ to $2A_0$	data inputs
18, 19	V_{CC}	positive power supply
20, 21, 22, 23	$1A_3$ to $1A_0$	data inputs
24	$1\overline{OE}$	output enable input (active LOW)

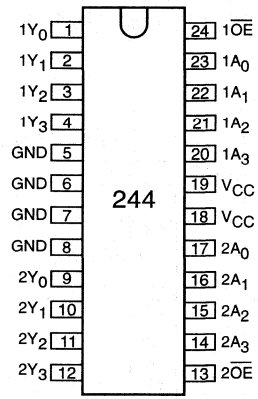


Fig.1 Pin configuration.

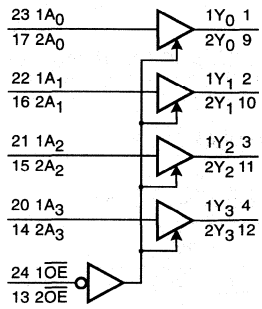


Fig.2 Logic symbol.

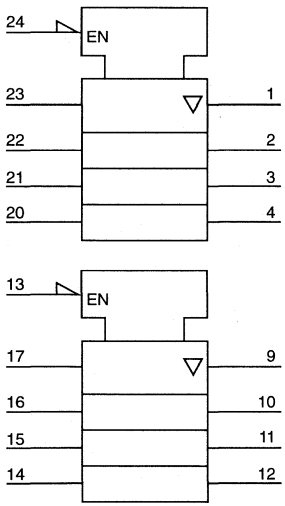


Fig.3 IEC logic symbol.

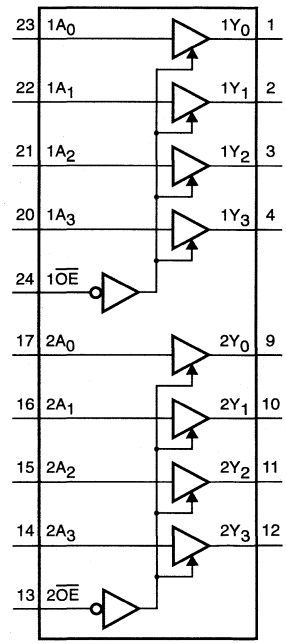


Fig.4 Functional diagram.

DC CHARACTERISTICS FOR 74HL33244

For the DC characteristics see chapter "HLL family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74HL33244

GND = 0 V; $t_r = t_f$ = 2.0 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)				UNIT	TEST CONDITIONS	
		+25		−40 to +85			V_{CC} (V)	WAVEFORMS
		MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	Propagation delay	–	14.0	–	16.0	ns	1.2	Fig. 5
	$1A_n$ to $1Y_n$;	–	5.3	–	6.0		2.0	
	$2A_n$ to $2Y_n$	–	3.5	–	4.0		3.0	
t_{PZH}/t_{PZL}	3-state output enable time	–	15.6	–	17.6	ns	1.2	Fig. 6, 7
	$1\overline{OE}$ to $1Y_n$;	–	5.9	–	6.6		2.0	
	$2\overline{OE}$ to $2Y_n$	–	3.9	–	4.4		3.0	
t_{PHZ}/t_{PLZ}	3-state output disable time	–	12.3	–	13.9	ns	1.2	Fig. 6, 7
	$1\overline{OE}$ to $1Y_n$;	–	5.4	–	6.0		2.0	
	$2\overline{OE}$ to $2Y_n$	–	4.0	–	4.4		3.0	

AC WAVEFORMS

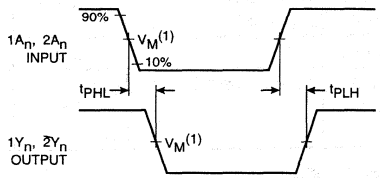


Fig. 5 Waveforms showing the input ($1A_n$, $2A_n$) to output ($1Y_n$, $2Y_n$) propagation delays and the output transition times.

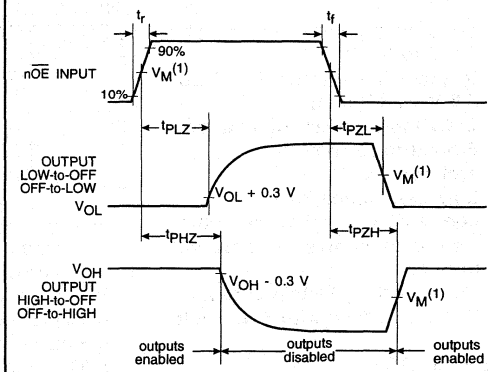


Fig.6 Waveforms showing the 3-state enable and disable times.

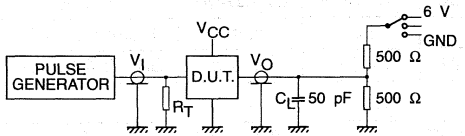


Fig. 8 Test conditions: Load circuitry for enable / disable times; switch set to 6 V for t_{PLZ}/t_{PZL}, switch set to GND for t_{PHZ}/t_{PZH} otherwise do not connect.

Notes: (1) V_M = 0.6 V at V_{CC}= 1.2 V.
V_M = 1.0 V at V_{CC}= 2.0 V.
V_M = 1.5 V at V_{CC}= 3.0 V.

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-state output load.

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with the JEDEC 3.3 V ±0.3 V supply**
- **CMOS low power consumption**
- **Flow-through pin-out architecture**
- **Low inductance, multiple centre power and ground pins for minimum noise and ground bounce**
- **Non-inverting 3-state outputs**
- **Direct interface with TTL levels**

DESCRIPTION

The 74HL33245 is a high-performance, low-power, low-voltage, Si-gate CMOS device superior to most advanced CMOS compatible TTL families.

The 74HL33245 is an octal transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The "245" features an output enable ($\overline{OE}$) input for easy cascading and a send/receive (DIR) input for direction control. $\overline{OE}$ controls the outputs so that the buses are effectively isolated.
The "245" is identical to the "640" but has true (non-inverting) outputs.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUT	
$\overline{OE}$	DIR	A_n	B_n
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n	C_L = 50 pF V_{CC} = 3.3 V	2.2	ns
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	35	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74HL33245D	24	SO	plastic	SO24/SOT137A
74HL33245DB	24	SSOP	plastic	SSOP24/SOT340

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 9, 10, 11, 12	A_0 to A_7	data inputs/outputs
5, 6, 7, 8	GND	ground (0 V)
13	$\overline{OE}$	output enable input (active LOW)
14, 15, 16, 17, 20, 21, 22, 23	B_7 to B_0	data inputs/outputs
18, 19	V_{CC}	positive supply voltage
24	DIR	direction control

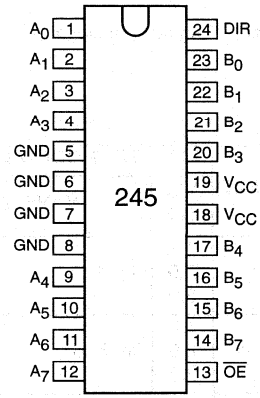


Fig.1 Pin configuration.

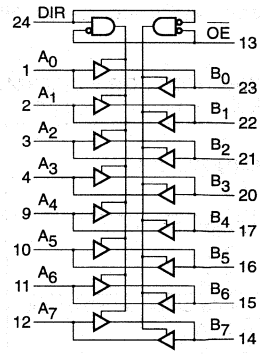


Fig.2 Logic symbol.

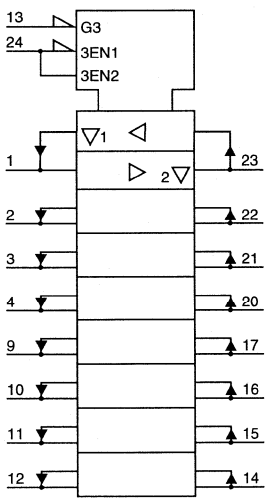


Fig.3 IEC logic symbol.

DC CHARACTERISTICS FOR 74HL33245

For the DC characteristics see chapter "HLL family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74HL33245

GND = 0 V; $t_r = t_f$ = 2.0 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)				UNIT	TEST CONDITIONS	
		+25		−40 to +85			V_{CC} (V)	WAVEFORMS
		MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay	–	14.0	–	16.0	ns	1.2	Fig. 4
	A_n to B_n;	–	5.3	–	6.0		2.0	
	B_n to A_n	–	3.5	–	4.0		3.0	
t_{PZH}/t_{PZL}	3–state output enable time	–	16.5	–	25.4	ns	1.2	Fig. 5, 6
	$\overline{OE}$ to A_n;	–	8.2	–	9.1		2.0	
	$\overline{OE}$ to B_n	–	5.5	–	6.3		3.0	
t_{PHZ}/t_{PLZ}	3–state output disable time	–	16.3	–	18.5	ns	1.2	Fig. 5, 6
	$\overline{OE}$ to A_n;	–	6.9	–	7.7		2.0	
	$\overline{OE}$ to B_n	–	5.0	–	5.6		3.0	

AC WAVEFORMS

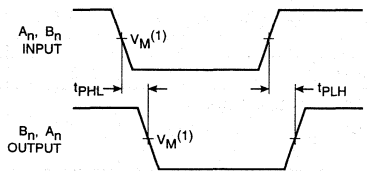


Fig.4 Waveforms showing the input (A_n, B_n) to output (B_n, A_n) propagation delays and the output transition times.

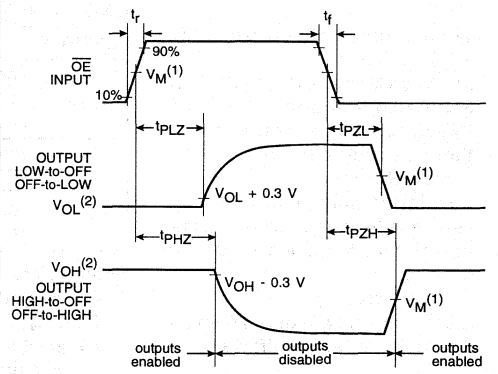


Fig.5 Waveforms showing the 3-state enable and disable times.

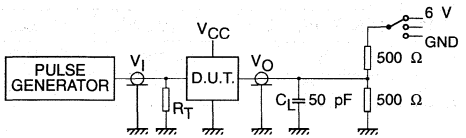


Fig.6 Test conditions: Load circuitry for enable / disable times; switch set to 6 V for t_{PLZ}/t_{PZL}, switch set to GND for t_{PHZ}/t_{PZH} otherwise do not connect.

Notes: (1) V_M = 0.6 V at V_{CC}= 1.2 V.
V_M = 1.0 V at V_{CC}= 2.0 V.
V_M = 1.5 V at V_{CC}= 3.0 V.

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-state output load.

Octal D-type transparent latch; 3-state | 74HL33373

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with the JEDEC 3.3 V ±0.3 V supply**
- **CMOS low power consumption**
- **Flow-through pin-out architecture**
- **Low inductance, multiple centre power and ground pins for minimum noise and ground bounce**
- **3-state outputs**
- **Direct interface with TTL levels**
- **5 V to 3.3 V level shifting**

DESCRIPTION

The 74HL33373 is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. A latch enable (LE) input and an output enable ($\overline{OE}$) are common to all internal latches.

The "373" consists of eight D-type transparent latches with 3-state true outputs. When LE is HIGH, data at the D_n inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the eight latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

The "373" is functionally identical to the "533", but the "533" has inverted outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n; LE to Q_n	C_L = 50 pF V_{CC} = 3.3 V	3.0 3.0	ns
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	25	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
74HL33373D	24	SO	plastic	SOT137A
74HL33373DB	24	SSOP	plastic	SOT340

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 9, 10, 11, 12	Q_0 to Q_7	data outputs
5, 6, 7, 8	GND	ground (0 V)
13	LE	latch enable
23, 22, 21, 20, 17, 16, 15, 14	D_0 to D_7	data inputs
18, 19	V_{CC}	positive supply voltage
24	$\overline{OE}$	output enable input (active LOW)

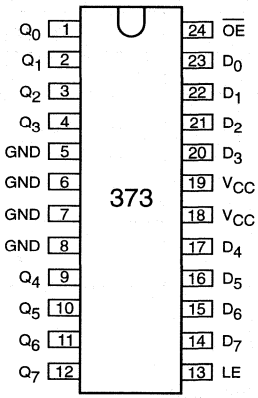


Fig.1 Pin configuration.

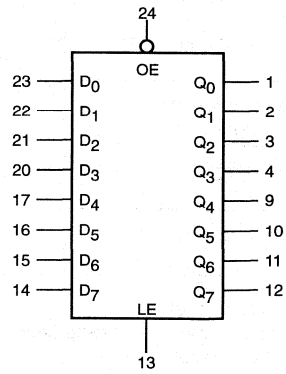


Fig.2 Logic symbol.

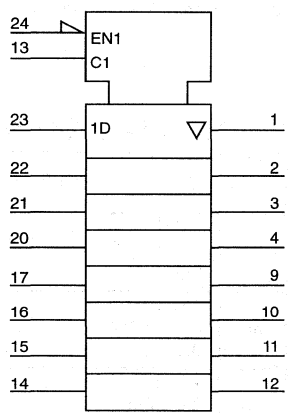


Fig3. IEC logic symbol.

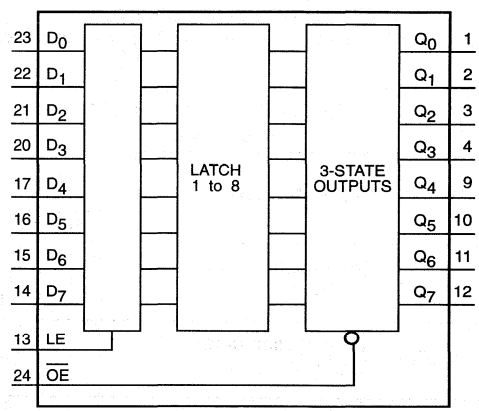


Fig.4 Functional diagram.

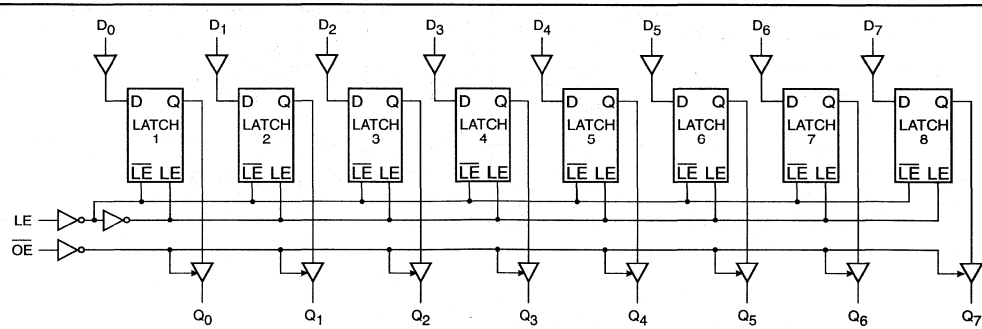


Fig.5 Logic diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS
	$\overline{OE}$	LE	D_n	Q_0 to Q_7
enable and read register (transparent mode)	L L	H H	L H	L H
latch and read register	L L	L L	l h	L H
latch register and disable outputs	H	X	X	Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
X = don't care
Z = high impedance OFF-state

DC CHARACTERISTICS FOR 74HL33373

For the DC characteristics see chapter "HLL family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74HL33373

GND = 0 V; $t_r = t_f$ = 2.0 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)				UNIT	TEST CONDITIONS	
		+25		−40 to +85			V_{CC} (V)	WAVEFORMS
		MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n	– – –	16.0 6.0 4.0	– – –	17.6 6.6 4.4	ns	1.2 2.0 3.0	Fig.6
t_{PHL}/t_{PLH}	propagation delay LE to Q_n	– – –	17.6 6.6 4.4	– – –	19.2 7.2 4.8	ns	1.2 2.0 3.0	Fig.7
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n	– – –	18.4 6.9 4.6	– – –	20.0 7.5 5.0	ns	1.2 2.0 3.0	Fig.8
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n	– – –	18.8 7.0 4.7	– – –	20.2 7.6 5.1	ns	1.2 2.0 3.0	Fig.8
t_W	LE pulse width HIGH	3.0 2.0	– –	3.8 2.5	– –	ns	2.0 3.0	Fig.7
t_{su}	set-up time D_n to LE	2.0 0.8 0.5	– – –	2.2 0.9 0.6	– – –	ns	1.2 2.0 3.0	Fig.9
t_h	hold time D_n to LE	2.0 0.8 0.5	– – –	2.2 0.9 0.6	– – –	ns	1.2 2.0 3.0	Fig.9

AC WAVEFORMS

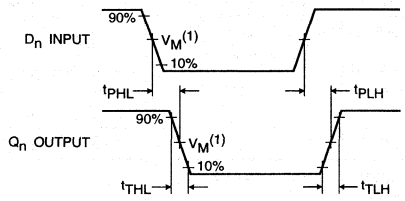


Fig.6 Waveforms showing the input (D_n) to output (Q_n) propagation delays and the output transition times.

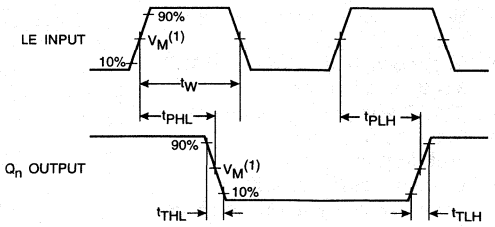


Fig.7 Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output (Q_n) propagation delays and the output transition times.

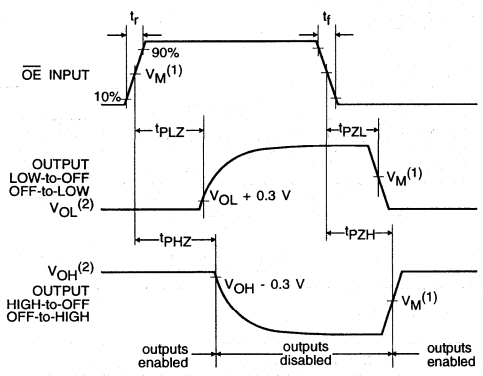


Fig.8 Waveforms showing the 3-state enable and disable times

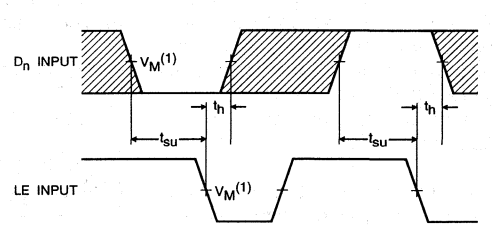


Fig.9 Waveforms showing the data set-up and hold times for the D_n input to the LE input.

Note to Fig.9:

The shaded areas indicate when the input is permitted to change for predictable output performance.

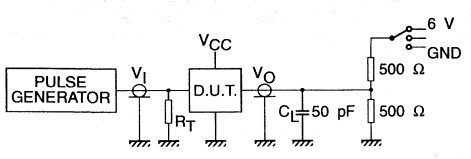


Fig.10 Test conditions: Load circuitry for enable / disable times, switch set to 6 V for t_{PLZ}/t_{PZL}, switch set to GND for t_{PHZ}/t_{PZH} otherwise do not connect.

Notes: (1) V_M = 0.6 V at V_{CC}= 1.2 V.
V_M = 1.0 V at V_{CC}= 2.0 V.
V_M = 1.5 V at V_{CC}= 3.0 V.

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-state output load.

Octal D-type flip-flop; positive edge-trigger; 3-state

74HL33374

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with the JEDEC 3.3 V ±0.3 V supply**
- **CMOS low power consumption**
- **Flow-through pin-out architecture**
- **Low inductance, multiple centre power and ground pins for minimum noise and ground bounce**
- **3-state outputs**
- **Direct interface with TTL levels**
- **5 V to 3.3 V level shifting**

DESCRIPTION

The 74HL33374 is an octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A clock (CP) input and an output enable ($\overline{OE}$) are common to all flip-flops.

The 8 flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition.

When $\overline{OE}$ is LOW, the contents of the 8 flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

The "374" is functionally identical to the "534", but has non-inverting outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 50 pF; V_{CC} = 3.3 V	3.2	ns
f_{max}	maximum clock frequency		350	MHz
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	28	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
74HL33374D	24	SO	plastic	SOT137A
74HL33374DB	24	SSOP	plastic	SOT340

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 9, 10, 11, 12	Q_0 to Q_7	data outputs
5, 6, 7, 8	GND	ground (0 V)
13	CP	clock input
23, 22, 21, 20, 17, 16, 15, 14	D_0 to D_7	data inputs
18, 19	V_{CC}	positive supply voltage
24	$\overline{OE}$	output enable input (active LOW)

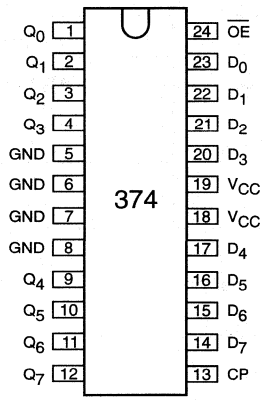


Fig.1 Pin configuration.

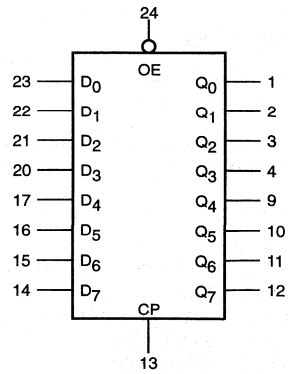


Fig.2 Logic symbol.

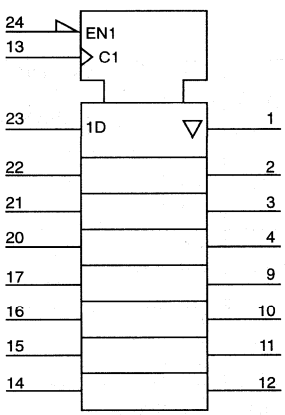


Fig3. IEC logic symbol.

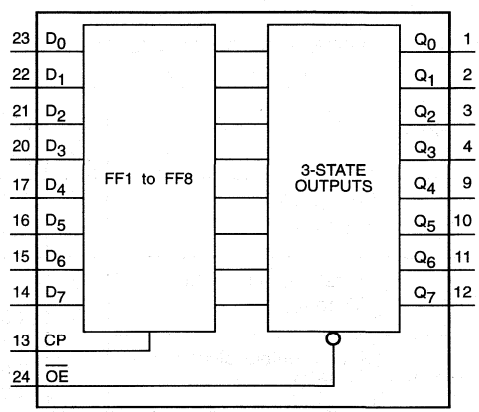


Fig.4 Functional diagram.

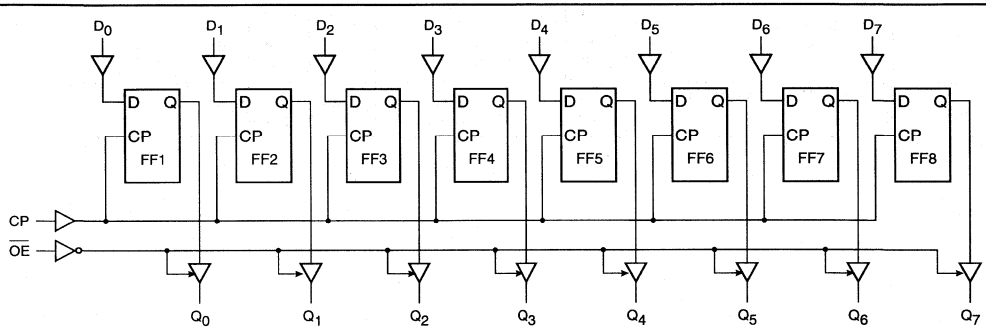


Fig.5 Logic diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS
	$\overline{OE}$	CP	D_n	Q_0 to Q_7
load and read register	L L	↑ ↑	l h	L H
load register and disable outputs	H H	↑ ↑	l h	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
Z = high impedance OFF-state
↑ = LOW-to-HIGH CP transition

DC CHARACTERISTICS FOR 74HL33374

For the DC characteristics see chapter "HLL family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74HL33374

GND = 0 V; $t_r = t_f$ = 2.0 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)				UNIT	TEST CONDITIONS	
		+25		−40 to +85			V_{CC} (V)	WAVEFORMS
		MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	– – –	17.2 6.4 4.3	– – –	18.9 7.0 4.8	ns	1.2 2.0 3.0	Fig.6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n	– – –	18.4 6.9 4.6	– – –	20.0 7.5 5.0	ns	1.2 2.0 3.0	Fig.7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n	– – –	18.8 7.0 4.7	– – –	20.2 7.6 5.1	ns	1.2 2.0 3.0	Fig.7
t_W	CP pulse width HIGH or LOW	3.0 2.0	– –	3.8 2.5	– –	ns	2.0 3.0	Fig.6
t_{su}	set-up time D_n to CP	2.0 0.8 0.5	– – –	2.2 0.9 0.6	– – –	ns	1.2 2.0 3.0	Fig.8
t_h	hold time D_n to CP	2.0 0.8 0.5	– – –	2.2 0.9 0.6	– – –	ns	1.2 2.0 3.0	Fig.8
f_{max}	maximum clock pulse frequency	166 250	– –	135 200	– –	MHz	2.0 3.0	Fig.6

AC WAVEFORMS

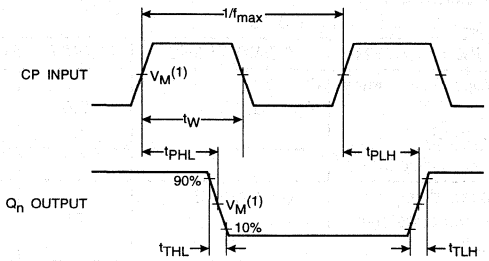


Fig.6 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency.

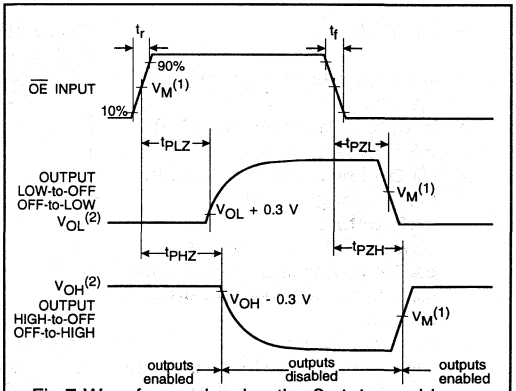


Fig.7 Waveforms showing the 3-state enable and disable times.

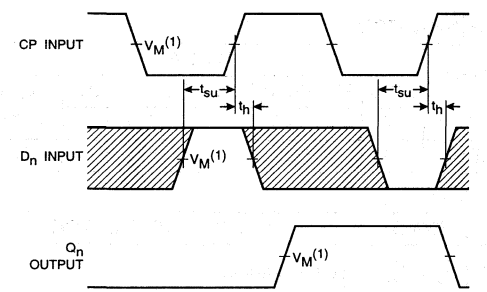


Fig.8 Waveforms showing the data set-up and hold times for the D_n input.

Note to Fig.8:

The shaded areas indicate when the input is permitted to change for predictable output performance.

Notes: (1) V_M = 0.6 V at V_{CC}= 1.2 V.
V_M = 1.0 V at V_{CC}= 2.0 V.
V_M = 1.5 V at V_{CC}= 3.0 V.

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-state output load.

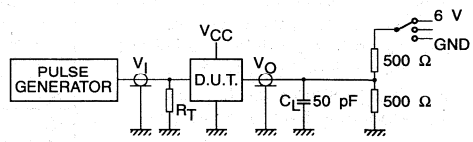


Fig.9 Test conditions: Load circuitry for enable / disable times, switch set to 6 V for t_{PLZ}/t_{PZL}, switch set to GND for t_{PHZ}/t_{PZH} otherwise do not connect.

Octal D-type transparent latch; 3-state; inverting

74HL33533

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with the JEDEC 3.3 V ±0.3 V supply**
- **CMOS low power consumption**
- **Flow-through pin-out architecture**
- **Low inductance, multiple centre power and ground pins for minimum noise and ground bounce**
- **3-state outputs**
- **Direct interface with TTL levels**
- **5 V to 3.3 V level shifting**

DESCRIPTION

The 74HL33533 is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. A latch enable (LE) input and an output enable ($\overline{OE}$) are common to all internal latches.

The "533" consists of eight D-type transparent latches with 3-state inverting outputs. When LE is HIGH, data at the D_n inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the eight latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

The "533" is functionally identical to the "373", but the "373" has non-inverted outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay D_n to $\overline{Q}_n$; LE to $\overline{Q}_n$	C_L = 50 pF V_{CC} = 3.3 V	3.0 3.0	ns
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	25	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
74HL33533D	24	SO	plastic	SOT137A
74HL33533DB	24	SSOP	plastic	SOT340

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 9, 10, 11, 12	$\overline{Q}_0$ to $\overline{Q}_7$	data outputs
5, 6, 7, 8	GND	ground (0 V)
13	LE	latch enable
23, 22, 21, 20, 17, 16, 15, 14	D_0 to D_7	data inputs
18, 19	V_{CC}	positive supply voltage
24	$\overline{OE}$	output enable input (active LOW)

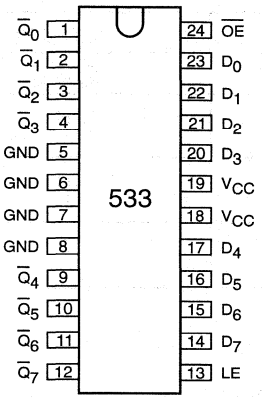


Fig.1 Pin configuration.

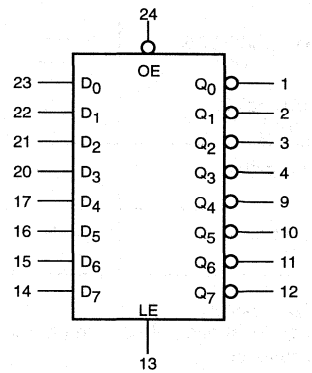


Fig.2 Logic symbol.

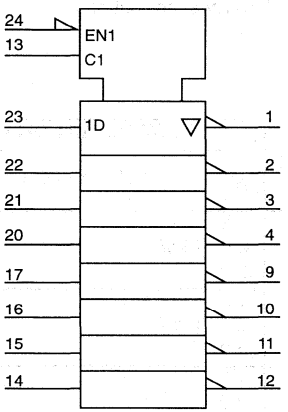


Fig.3 IEC logic symbol.

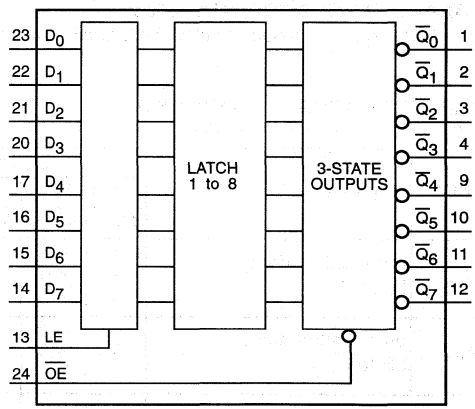


Fig.4 Functional diagram.

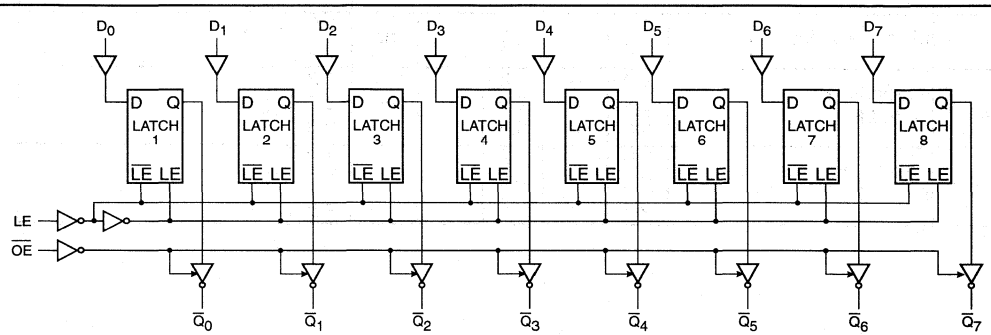


Fig.5 Logic diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS
	$\overline{OE}$	LE	D_n	$\overline{Q}_0$ to $\overline{Q}_7$
enable and read register (transparent mode)	L L	H H	L H	H L
latch and read register	L L	L L	l h	H L
latch register and disable outputs	H	X	X	Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
X = don't care
Z = high impedance OFF-state

DC CHARACTERISTICS FOR 74HL33533

For the DC characteristics see chapter "HLL family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74HL33533

GND = 0 V; $t_r = t_f$ = 2.0 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)				UNIT	TEST CONDITIONS	
		+25		−40 to +85			V_{CC} (V)	WAVEFORMS
		MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay D_n to $\overline{Q}_n$	– – –	16.0 6.0 4.0	– – –	17.6 6.6 4.4	ns	1.2 2.0 3.0	Fig.6
t_{PHL}/t_{PLH}	propagation delay LE to $\overline{Q}_n$	– – –	17.6 6.6 4.4	– – –	19.2 7.2 4.8	ns	1.2 2.0 3.0	Fig.7
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to $\overline{Q}_n$	– – –	18.4 6.9 4.6	– – –	20.0 7.5 5.0	ns	1.2 2.0 3.0	Fig.8
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to $\overline{Q}_n$	– – –	18.8 7.0 4.7	– – –	20.2 7.6 5.1	ns	1.2 2.0 3.0	Fig.8
t_W	LE pulse width HIGH	3.0 2.0	– –	3.8 2.5	– –	ns	2.0 3.0	Fig.7
t_{su}	set-up time D_n to LE	2.0 0.8 0.5	– – –	2.2 0.9 0.6	– – –	ns	1.2 2.0 3.0	Fig.9
t_h	hold time D_n to LE	2.0 0.8 0.5	– – –	2.2 0.9 0.6	– – –	ns	1.2 2.0 3.0	Fig.9

AC WAVEFORMS

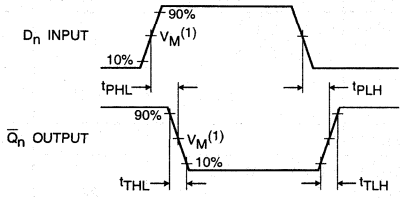


Fig.6 Waveforms showing the input (D_n) to output ($\overline{Q}_n$) propagation delays and the output transition times.

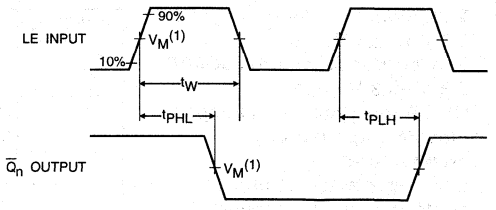


Fig.7 Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output ($\overline{Q}_n$) propagation delays and the output transition times.

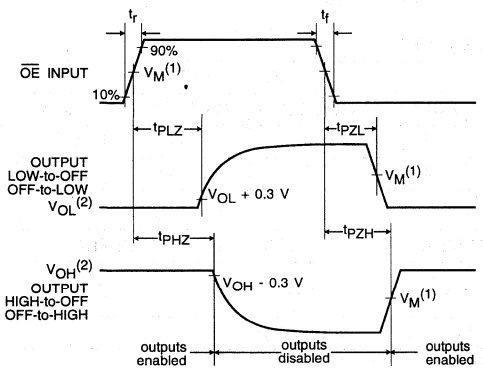


Fig.8 Waveforms showing the 3-state enable and disable times

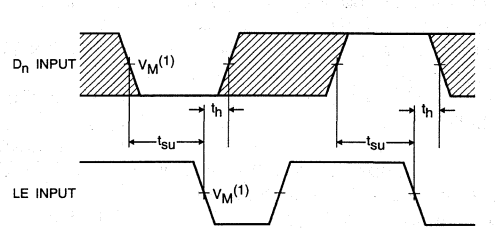


Fig.9 Waveforms showing the data set-up and hold times for the D_n input to the LE input.

Note to Fig.9:

The shaded areas indicate when the input is permitted to change for predictable output performance.

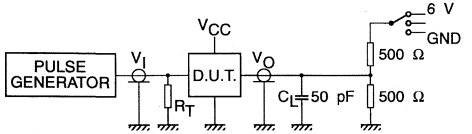


Fig.10 Test conditions: Load circuitry for enable / disable times, switch set to 6 V for t_{PLZ}/t_{PZL}, switch set to GND for t_{PHZ}/t_{PZH} otherwise do not connect.

Notes: (1) V_M = 0.6 V at V_{CC}= 1.2 V.
V_M = 1.0 V at V_{CC}= 2.0 V.
V_M = 1.5 V at V_{CC}= 3.0 V.

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-state output load.

Octal D-type flip-flop; positive edge-trigger; 3-state; inverting

74HL33534

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with the JEDEC 3.3 V ±0.3 V supply**
- **CMOS low power consumption**
- **Flow-through pin-out architecture**
- **Low inductance, multiple centre power and ground pins for minimum noise and ground bounce**
- **3-state inverting outputs**
- **Direct interface with TTL levels**
- **5 V to 3.3 V level shifting**

DESCRIPTION

The 74HL33534 is an octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A clock (CP) input and an output enable ($\overline{OE}$) are common to all flip-flops.

The 8 flip-flops will store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH CP transition.

When $\overline{OE}$ is LOW, the contents of the 8 flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

The "534" is functionally identical to the "374", but has inverting outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{Q}_n$	C_L = 50 pF; V_{CC} = 3.3 V	3.2	ns
f_{max}	maximum clock frequency		350	MHz
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	28	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
74HL33534D	24	SO	plastic	SOT137A
74HL33534DB	24	SSOP	plastic	SOT340

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 9, 10, 11, 12	$\overline{Q}_0$ to $\overline{Q}_7$	data outputs
5, 6, 7, 8	GND	ground (0 V)
13	CP	clock input
23, 22, 21, 20, 17, 16, 15, 14	D_0 to D_7	data inputs
18, 19	V_{CC}	positive supply voltage
24	$\overline{OE}$	output enable input (active LOW)

Octal D-type flip-flop; positive edge-trigger; 3-state; inverting

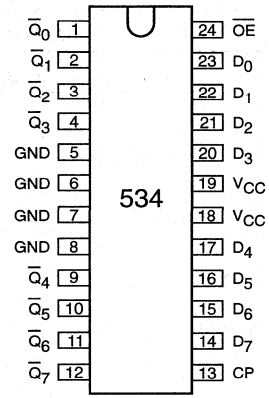


Fig.1 Pin configuration.

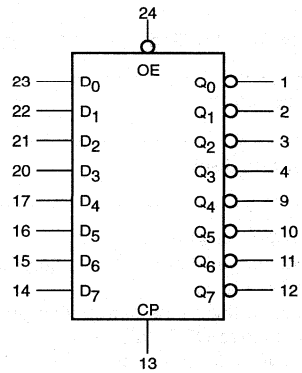


Fig.2 Logic symbol.

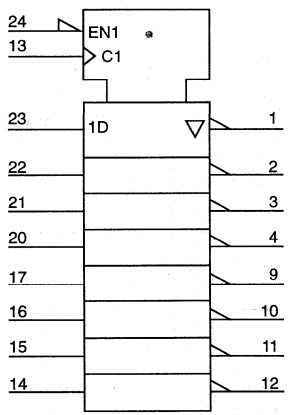


Fig.3 IEC logic symbol.

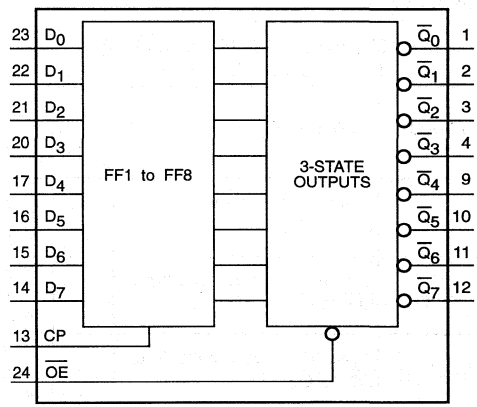


Fig.4 Functional diagram.

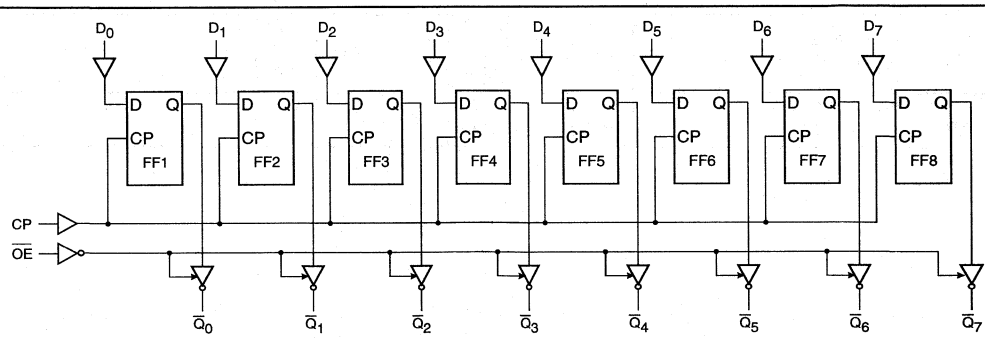


Fig.5 Logic diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS
	$\overline{OE}$	CP	D_n	$\overline{Q}_0$ to $\overline{Q}_7$
load and read register	L	↑	l	H
	L	↑	h	L
load register and disable outputs	H	↑	l	Z
	H	↑	h	Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
Z = high impedance OFF-state
↑ = LOW-to-HIGH CP transition

DC CHARACTERISTICS FOR 74HL33534

For the DC characteristics see chapter "HLL family characteristics", section "Family specifications".
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HL33534

GND = 0 V; $t_r = t_f$ = 2.0 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)				UNIT	TEST CONDITIONS	
		+25		−40 to +85			V_{CC} (V)	WAVEFORMS
		MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{Q}_n$	–	17.2	–	18.9	ns	1.2	Fig.6
		–	6.4	–	7.0		2.0	
		–	4.3	–	4.8		3.0	
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to $\overline{Q}_n$	–	18.4	–	20.0	ns	1.2	Fig.7
		–	6.9	–	7.5		2.0	
		–	4.6	–	5.0		3.0	
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to $\overline{Q}_n$	–	18.8	–	20.2	ns	1.2	Fig.7
		–	7.0	–	7.6		2.0	
		–	4.7	–	5.1		3.0	
t_W	CP pulse width HIGH or LOW	3.0	–	3.8	–	ns	2.0	Fig.6
		2.0	–	2.5	–		3.0	
t_{su}	set-up time D_n to CP	2.0	–	2.2	–	ns	1.2	Fig.8
		0.8	–	0.9	–		2.0	
		0.5	–	0.6	–		3.0	
t_h	hold time D_n to CP	2.0	–	2.2	–	ns	1.2	Fig.8
		0.8	–	0.9	–		2.0	
		0.5	–	0.6	–		3.0	
f_{max}	maximum clock pulse frequency	166	–	135	–	MHz	2.0	Fig.6
		250	–	200	–		3.0	

AC WAVEFORMS

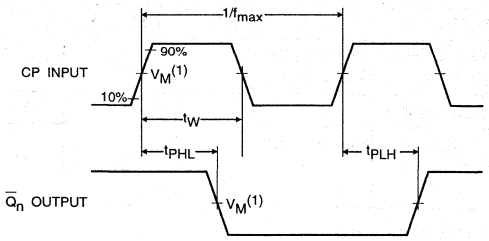


Fig.6 Waveforms showing the clock (CP) to output ($\overline{Q}_n$) propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency.

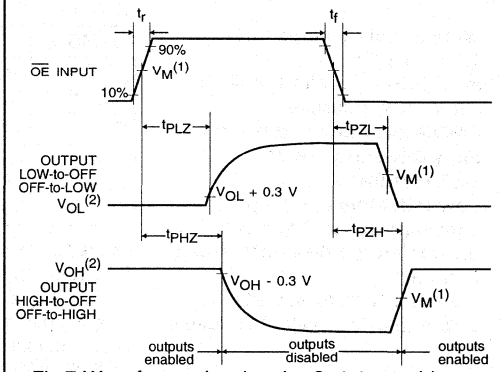


Fig.7 Waveforms showing the 3-state enable and disable times.

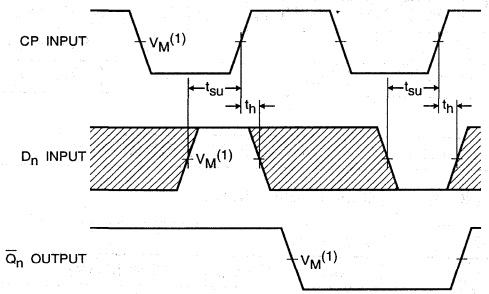


Fig.8 Waveforms showing the data set-up and hold times for the D_n input.

Note to Fig.8:

The shaded areas indicate when the input is permitted to change for predictable output performance.

Notes: (1) V_M = 0.6 V at V_{CC}= 1.2 V.
V_M = 1.0 V at V_{CC}= 2.0 V.
V_M = 1.5 V at V_{CC}= 3.0 V.

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-state output load.

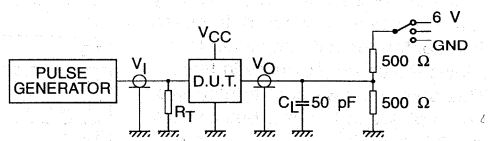


Fig.9 Test conditions: Load circuitry for enable / disable times, switch set to 6 V for t_{PLZ}/t_{PZL}, switch set to GND for t_{PHZ}/t_{PZH} otherwise do not connect.

Octal transceiver with dual enable; 3-state; inverting

74HL33620

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with the JEDEC 3.3 V ±0.3 V supply**
- **CMOS low power consumption**
- **Flow-through pin-out architecture**
- **Low inductance, multiple centre power and ground pins for minimum noise and ground bounce**
- **Inverting 3-state outputs**
- **Direct interface with TTL levels**

DESCRIPTION

The 74HL33620 is a high-performance, low-power, low-voltage, Si-gate CMOS device superior to most advanced CMOS compatible TTL families.

The 74HL33620 is an octal transceiver featuring inverting 3-state bus compatible outputs in both send and receive directions.

This octal bus transceiver is designed for asynchronous two-way communication between data buses. The control function implementation allows maximum flexibility in timing. This device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the enable inputs (OE_{AB}, $\overline{OE}_{BA}$). The enable inputs can be used to disable the device so that the buses are effectively isolated. The dual enable function configuration gives this transceiver the capability to store data by simultaneous enabling of OE_{AB} and $\overline{OE}_{BA}$. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance OFF-state, both sets of bus lines will remain at their last states.The 8-bit codes appearing on the two sets of buses will be complementary. The "620" is identical to the "623" but has inverting outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n	C_L = 50 pF V_{CC} = 3.3 V	2.2	ns
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	35	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
74HL33620D	24	SO	plastic	SOT137A
74HL33620DB	24	SSOP	plastic	SOT340

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 9, 10, 11, 12	A_0 to A_7	data inputs/outputs
5, 6, 7, 8	GND	ground (0 V)
13	$\overline{OE}_{BA}$	output enable input (active LOW)
14, 15, 16, 17, 20, 21, 22, 23	B_7 to B_0	data inputs/outputs
18, 19	V_{CC}	positive supply voltage
24	OE_{AB}	output enable input (active HIGH)

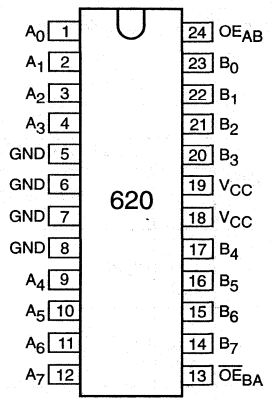


Fig.1 Pin configuration.

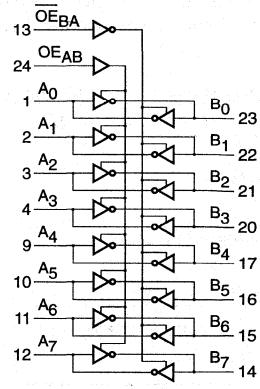


Fig.2 Logic symbol.

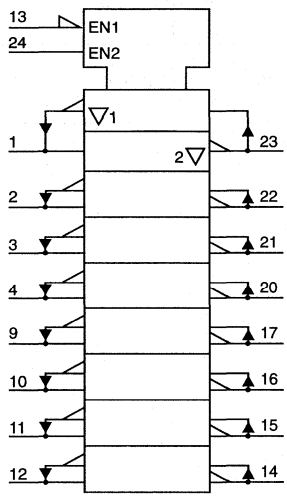


Fig.3 IEC logic symbol.

FUNCTION TABLE

ENABLE INPUTS		OPERATION
OE_{AB}	$\overline{OE}_{BA}$	
L	L	$\overline{B}$ data to A bus
H	H	$\overline{A}$ data to B bus
L	H	Z
H	L	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus

H = HIGH voltage level
L = LOW voltage level
Z = high impedance OFF-state

DC CHARACTERISTICS FOR 74HL33620

For the DC characteristics see chapter "HLL family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74HL33620

GND = 0 V; $t_r = t_f$ = 2.0 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)				UNIT	TEST CONDITIONS	
		+25		−40 to +85			V_{CC} (V)	WAVEFORMS
		MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n	– – –	14.0 5.3 3.5	– – –	16.0 6.0 4.0	ns	1.2 2.0 3.0	Fig.4
t_{PZH}/t_{PZL}	3-state output enable time OE_{AB} to B_n	– – –	18.4 6.9 4.6	– – –	21.2 7.9 5.3	ns	1.2 2.0 3.0	Fig.5, 6
t_{PHZ}/t_{PLZ}	3-state output disable time OE_{AB} to B_n	– – –	14.7 6.3 4.6	– – –	16.7 7.0 5.1	ns	1.2 2.0 3.0	Fig.5, 6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_{BA}$ to A_n	– – –	18.4 6.9 4.6	– – –	21.2 7.9 5.3	ns	1.2 2.0 3.0	Fig.5, 6
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_{BA}$ to A_n	– – –	15.0 6.4 4.7	– – –	17.1 7.2 5.2	ns	1.2 2.0 3.0	Fig.5, 6

AC WAVEFORMS

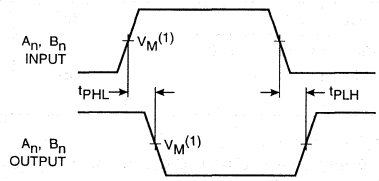


Fig. 4 Waveforms showing the input (A_n, B_n) to output (B_n, A_n) propagation delays and the output transition times.

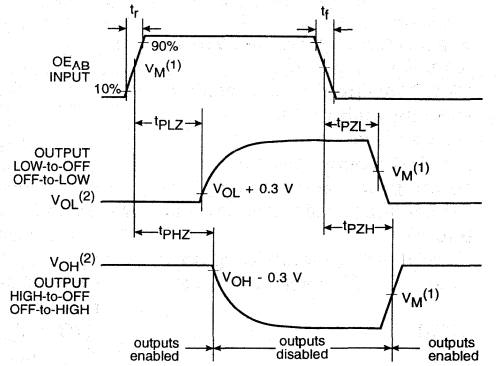


Fig.5 Waveforms showing the 3-state enable and disable times for OE_{AB} input.

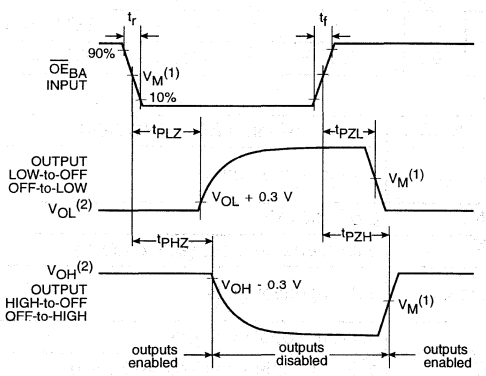


Fig.6 Waveforms showing the 3-state enable and disable times for $\overline{OE}_{BA}$ input.

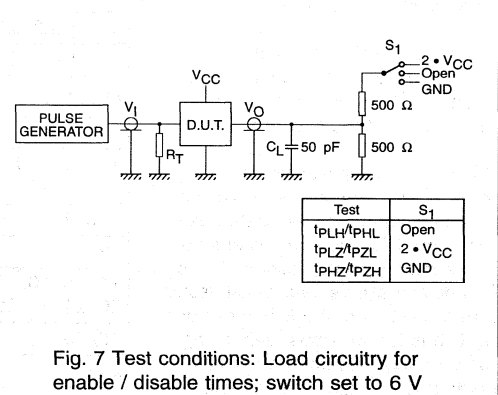


Fig. 7 Test conditions: Load circuitry for enable / disable times; switch set to 6 V for t_{PLZ}/t_{PZL}, switch set to GND for t_{PHZ}/t_{PZH} otherwise do not connect.

Notes: (1) V_M = 0.6 V at V_{CC}= 1.2 V.
V_M = 1.0 V at V_{CC}= 2.0 V.
V_M = 1.5 V at V_{CC}= 3.0 V.

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-state output load.

Octal transceiver with dual enable; 3-state | 74HL33623

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with the JEDEC 3.3 V ±0.3 V supply**
- **CMOS low power consumption**
- **Flow-through pin-out architecture**
- **Low inductance, multiple centre power and ground pins for minimum noise and ground bounce**
- **Non-inverting 3-state outputs**
- **Direct interface with TTL levels**

DESCRIPTION

The 74HL33623 is a high-performance, low-power, low-voltage, Si-gate CMOS device superior to most advanced CMOS compatible TTL families.

The 74HL33623 is an octal transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions.

This octal bus transceiver is designed for asynchronous two-way communication between data buses. The control function implementation allows maximum flexibility in timing. This device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the enable inputs (OE_{AB}, $\overline{OE}_{BA}$). The enable inputs can be used to disable the device so that the buses are effectively isolated. The dual enable function configuration gives this transceiver the capability to store data by simultaneous enabling of OE_{AB} and $\overline{OE}_{BA}$. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance OFF-state, both sets of bus lines will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical.
The '623' is identical to the '620' but has true (non-inverting) outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n	C_L = 50 pF V_{CC} = 3.3 V	2.2	ns
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	35	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
74HL33623D	24	SO	plastic	SOT137A
74HL33623DB	24	SSOP	plastic	SOT340

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 9, 10, 11, 12	A_0 to A_7	data inputs/outputs
5, 6, 7, 8	GND	ground (0 V)
13	$\overline{OE}_{BA}$	output enable input (active LOW)
14, 15, 16, 17, 20, 21, 22, 23	B_7 to B_0	data inputs/outputs
18, 19	V_{CC}	positive supply voltage
24	OE_{AB}	output enable input (active HIGH)

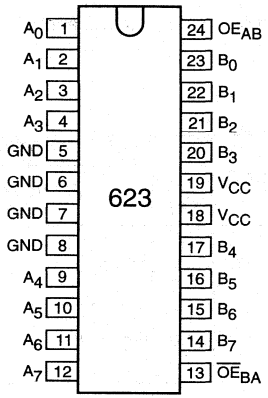


Fig.1 Pin configuration.

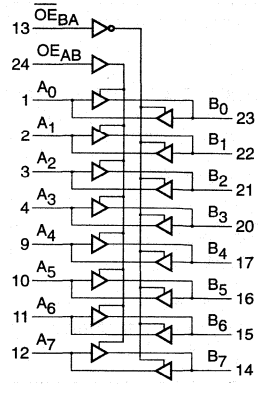


Fig.2 Logic symbol.

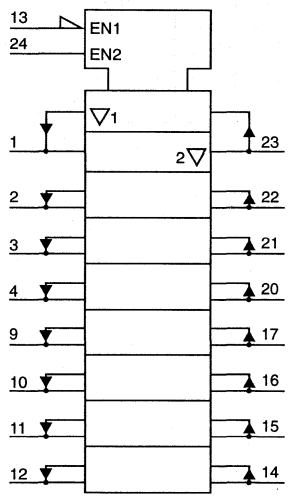


Fig.3 IEC logic symbol.

FUNCTION TABLE

ENABLE INPUTS		OPERATION
OE_{AB}	$\overline{OE}_{BA}$	
L	L	B data to A bus
H	H	A data to B bus
L	H	Z
H	L	B data to A bus, A data to B bus

H = HIGH voltage level
L = LOW voltage level
Z = high impedance OFF-state

DC CHARACTERISTICS FOR 74HL33623

For the DC characteristics see chapter "HLL family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74HL33623

GND = 0 V; $t_r = t_f$ = 2.0 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)				UNIT	TEST CONDITIONS	
		+25		−40 to +85			V_{CC} (V)	WAVEFORMS
		MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n	– – –	14.0 5.3 3.5	– – –	16.0 6.0 4.0	ns	1.2 2.0 3.0	Fig. 4
t_{PZH}/t_{PZL}	3-state output enable time OE_{AB} to B_n	– – –	18.4 6.9 4.6	– – –	21.2 7.9 5.3	ns	1.2 2.0 3.0	Fig. 5, 6
t_{PHZ}/t_{PLZ}	3-state output disable time OE_{AB} to B_n	– – –	14.7 6.3 4.6	– – –	16.7 7.0 5.1	ns	1.2 2.0 3.0	Fig. 5, 6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_{BA}$ to A_n	– – –	18.4 6.9 4.6	– – –	21.2 7.9 5.3	ns	1.2 2.0 3.0	Fig. 5, 6
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_{BA}$ to A_n	– – –	15.0 6.4 4.7	– – –	17.0 7.2 5.2	ns	1.2 2.0 3.0	Fig. 5, 6

AC WAVEFORMS

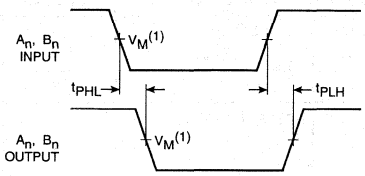


Fig. 4 Waveforms showing the input (A_n, B_n) to output (B_n, A_n) propagation delays and the output transition times.

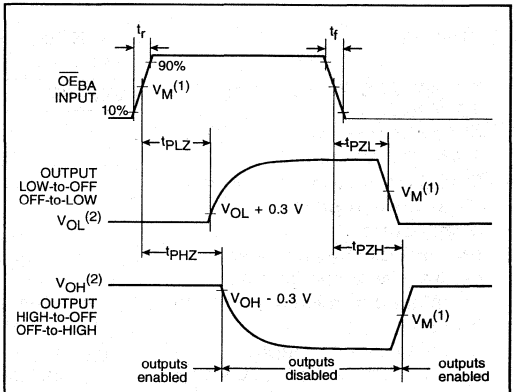


Fig.5 Waveforms showing the 3-state enable and disable times for $\overline{OE}_{BA}$ input.

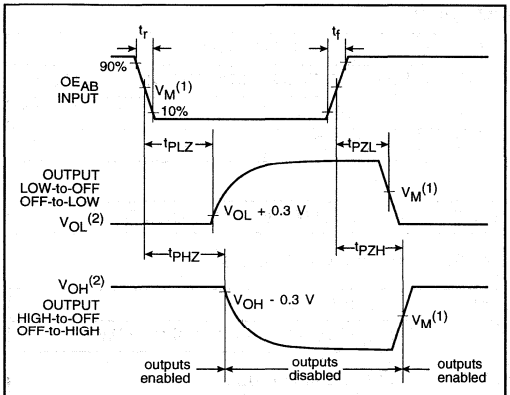


Fig.6 Waveforms showing the 3-state enable and disable times for OE_{AB} input.

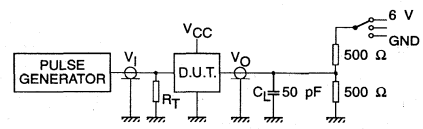


Fig.7 Test conditions: Load circuitry for enable / disable times; switch set to 6 V for t_{PLZ}/t_{PZL}, switch set to GND for t_{PHZ}/t_{PZH} otherwise do not connect.

Notes: (1) V_M = 0.6 V at V_{CC}= 1.2 V.
V_M = 1.0 V at V_{CC}= 2.0 V.
V_M = 1.5 V at V_{CC}= 3.0 V.

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-state output load.

Octal transceiver with direction pin; 3-state; inverting

74HL33640

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with the JEDEC 3.3 V ±0.3 V supply**
- **CMOS low power consumption**
- **Flow-through pin-out architecture**
- **Low inductance, multiple centre power and ground pins for minimum noise and ground bounce**
- **Inverting 3-state outputs**
- **Direct interface with TTL levels**

DESCRIPTION

The 74HL33640 is a high-performance, low-power, low-voltage, Si-gate CMOS device superior to most advanced CMOS compatible TTL families.

The 74HL33640 is an octal transceiver featuring inverting 3-state bus compatible outputs in both send and receive directions. The "640" features an output enable ($\overline{OE}$) input for easy cascading and a send/receive (DIR) input for direction control. $\overline{OE}$ controls the outputs so that the buses are effectively isolated.
The "640" is identical to the "245" but has inverting outputs.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUT	
$\overline{OE}$	DIR	A_n	B_n
L	L	A = $\overline{B}$	inputs
L	H	inputs	B = $\overline{A}$
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n	C_L = 50 pF V_{CC} = 3.3 V	2.2	ns
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	35	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
74HL33640D	24	SO	plastic	SOT137A
74HL33640DB	24	SSOP	plastic	SOT340

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 9, 10, 11, 12	A_0 to A_7	data inputs/outputs
5, 6, 7, 8	GND	ground (0 V)
13	$\overline{OE}$	output enable input (active LOW)
14, 15, 16, 17, 20, 21, 22, 23	B_7 to B_0	data inputs/outputs
18, 19	V_{CC}	positive supply voltage
24	DIR	direction control

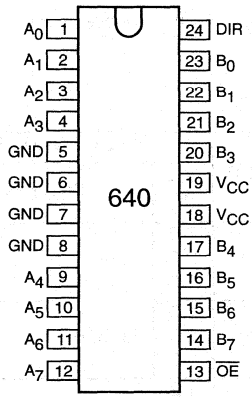


Fig.1 Pin configuration.

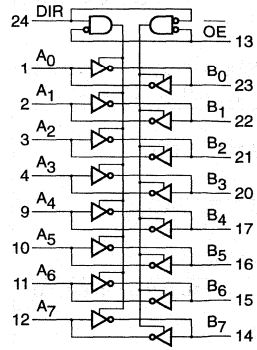


Fig.2 Logic symbol.

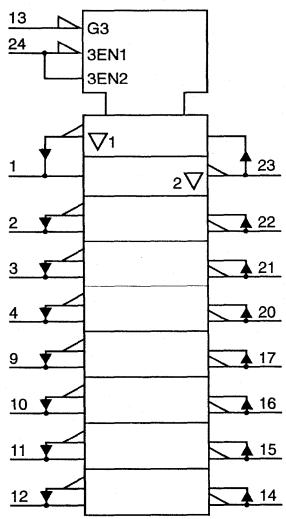


Fig.3 IEC logic symbol.

DC CHARACTERISTICS FOR 74HL33640

For the DC characteristics see chapter "HLL family characteristics", section "Family specifications".
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HL33640

GND = 0 V; $t_r = t_f$ = 2.0 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)				UNIT	TEST CONDITIONS	
		+25		−40 to +85			V_{CC} (V)	WAVEFORMS
		MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay	–	14.0	–	16.0	ns	1.2	Fig. 4
	A_n to B_n;	–	5.3	–	6.0		2.0	
	B_n to A_n	–	3.5	–	4.0		3.0	
t_{PZH}/t_{PZL}	3-state output enable time	–	17.8	–	20.7	ns	1.2	Fig. 5, 6
	$\overline{OE}$ to A_n;	–	7.5	–	8.5		2.0	
	$\overline{OE}$ to B_n	–	5.4	–	6.1		3.0	
t_{PHZ}/t_{PLZ}	3-state output disable time	–	15.0	–	16.7	ns	1.2	Fig. 5, 6
	$\overline{OE}$ to A_n;	–	6.4	–	7.0		2.0	
	$\overline{OE}$ to B_n	–	4.7	–	5.1		3.0	

AC WAVEFORMS

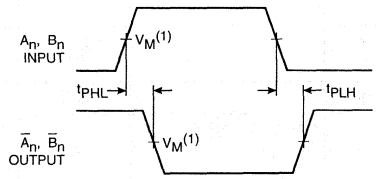


Fig. 4 Waveforms showing the input (A_n, B_n) to output (B_n, A_n) propagation delays and the output transition times.

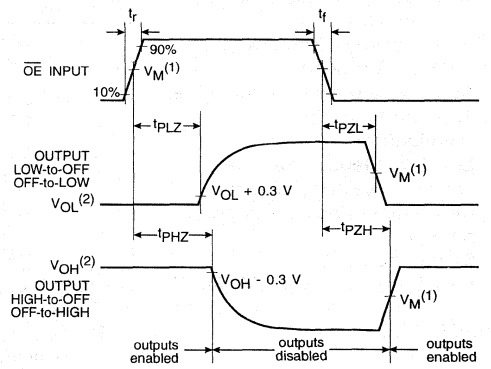


Fig.5 Waveforms showing the 3-state enable and disable times.

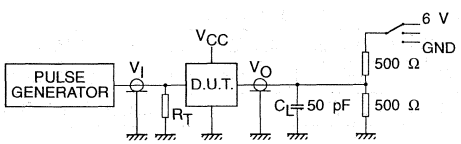


Fig. 6 Test conditions: Load circuitry for enable / disable times; switch set to 6 V for t_{PLZ}/t_{PZL}, switch set to GND for t_{PHZ}/t_{PZH} otherwise do not connect.

Notes: (1) V_M = 0.6 V at V_{CC}= 1.2 V.
V_M = 1.0 V at V_{CC}= 2.0 V.
V_M = 1.5 V at V_{CC}= 3.0 V.

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-state output load.

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with the JEDEC 3.3 V ±0.3 V supply**
- **CMOS low power consumption**
- **Flow-through pin-out architecture**
- **Low inductance, multiple centre power and ground pins for minimum noise and ground bounce**
- **3-state outputs**
- **Direct interface with TTL levels**

DESCRIPTION

The 74HL33646 consist of 8 non-inverting bus transceiver circuits with 3-state outputs, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the internal registers. Data on the 'A' or 'B' bus will be clocked in the internal registers, as the appropiate clock (CP_{AB} or CP_{BA}) goes to a HIGH logic level. Output enable ($\overline{OE}$) and direction (DIR) inputs are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the 'A' or 'B' register, or in both.The select source inputs (S_{AB} and S_{BA}) can multiplex stored and real-time (transparent mode) data. The direction (DIR) input determines which bus will receive data when $\overline{OE}$ is active (LOW). In the isolation mode ($\overline{OE}$ = HIGH), 'A' data may be stored in the 'B' register and/or 'B' data may be stored in the 'A' register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, 'A' or 'B' may be driven at a time.

The '646' is functionally identical to the '648', but has non-inverting data paths.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to B_n, A_n	C_L = 50 pF V_{CC} = 3.3 V	3.2	ns
f_{max}	maximum clock frequency		350	MHz
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	50	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PACKAGE	MATERIAL	CODE
74HL33646D	28	SO	plastic	SO28/SOT136A
74HL33646DB	28	SSOP	plastic	SSOP28/SOT341

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	output enable input (active LOW)
2, 3, 4, 5, 10, 11, 12, 13	A_0 to A_7	'A' data inputs/outputs
6, 7, 8, 9	GND	ground (0 V)
14	DIR	direction control input
15	S_{BA}	select 'B' to 'A' source input
16	CP_{BA}	'B' to 'A' clock input (Low-to-High, edge-triggered)
26, 25, 24, 23, 20, 19, 18, 17	B_0 to B_7	'B' data inputs/outputs
21, 22	V_{CC}	positive supply voltage
27	S_{AB}	select 'A' to 'B' source input
28	CP_{AB}	'A' to 'B' clock input (Low-to-High, edge-triggered)

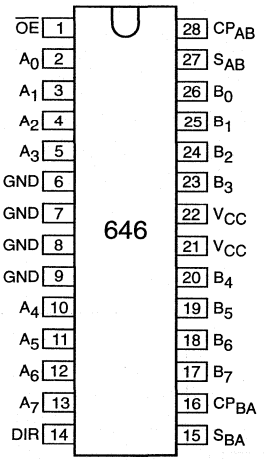


Fig.1 Pin configuration.

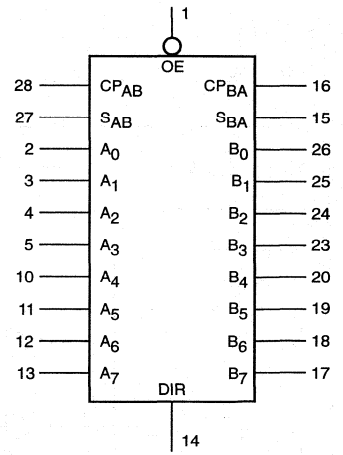


Fig.2 Logic symbol.

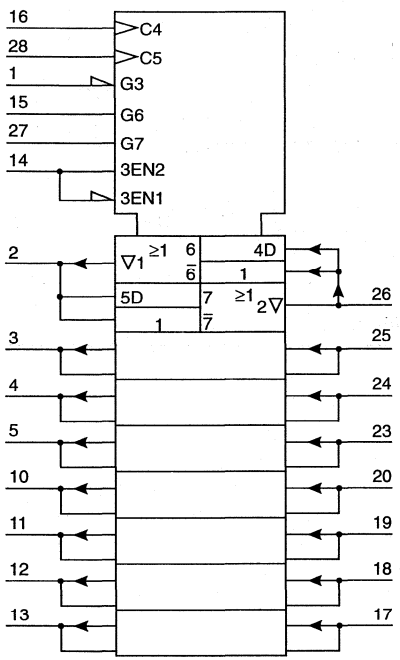


Fig3. IEC logic symbol.

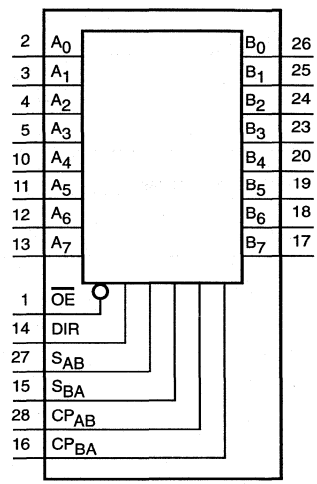


Fig.4 Functional diagram.

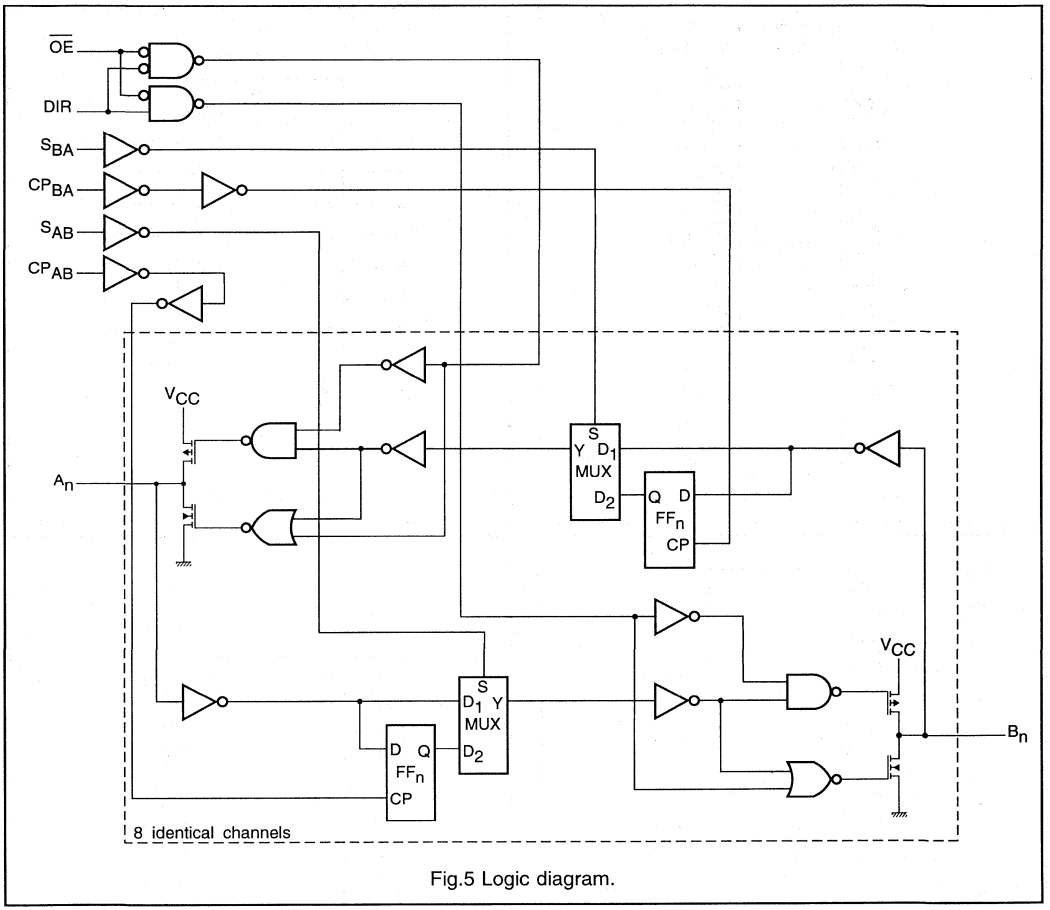


Fig.5 Logic diagram.

FUNCTION TABLE

INPUTS						DATA I/O *		FUNCTION
$\overline{OE}$	DIR	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	A_0 to A_7	B_0 to B_7	
X X	X X	↑ X	X ↑	X X	X X	input un*	un* input	store A, B unspecified* store B, A unspecified*
H H	X X	↑ H or L	↑ H or L	X X	X X	input	input	store A and B data, isolation hold storage
L L	L L	X X	X H or L	X X	L H	output	input	real-time B data to A bus stored B data to A bus
L L	H H	X H or L	X X	L H	X X	input	output	real-time A data to B bus stored A data to B bus

* The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

un = unspecified
H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH level transition

DC CHARACTERISTICS FOR 74HL33646

For the DC characteristics see chapter "HLL family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74HL33646

GND = 0 V; $t_r = t_f$ = 2.0 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)				UNIT	TEST CONDITIONS	
		+25		-40 to +85			V_{CC} (V)	WAVEFORMS
		MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to B_n, A_n	–	19.2	–	22.0	ns	1.2	Fig.6
		–	7.2	–	8.3		2.0	
		–	4.8	–	5.5		3.0	
t_{PHL}/t_{PLH}	propagation delay CP_{AB}, CP_{BA} to B_n, A_n	–	23.2	–	26.8	ns	1.2	Fig.7
		–	8.7	–	10.1		2.0	
		–	5.8	–	6.7		3.0	
t_{PHL}/t_{PLH}	propagation delay S_{AB}, S_{BA} to B_n, A_n	–	24.4	–	28.0	ns	1.2	Fig.8
		–	9.2	–	10.5		2.0	
		–	6.1	–	7.0		3.0	
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to A_n, B_n	–	24.4	–	28.0	ns	1.2	Fig.9
		–	9.2	–	10.5		2.0	
		–	6.1	–	7.0		3.0	
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to A_n, B_n	–	19.5	–	22.3	ns	1.2	Fig.9
		–	8.1	–	9.1		2.0	
		–	5.8	–	6.5		3.0	
t_{PZH}/t_{PZL}	3-state output enable time DIR to A_n, B_n	–	26.0	–	30.0	ns	1.2	Fig.11
		–	9.8	–	11.3		2.0	
		–	6.5	–	7.5		3.0	
t_{PHZ}/t_{PLZ}	3-state output disable time DIR to A_n, B_n	–	20.3	–	23.1	ns	1.2	Fig.11
		–	8.4	–	9.5		2.0	
		–	6.0	–	6.7		3.0	
t_W	clock pulse width HIGH or LOW CP_{AB} or CP_{BA}	3.0	–	3.7	–	ns	2.0	Figs 6 and 8
		2.0	–	2.5	–		3.0	
t_{su}	set-up time A_n, B_n to CP_{AB}, CP_{BA}	–	–	–	–	ns	1.2	Fig.7
		–	–	–	–		2.0	
		1.0	–	1.0	–		3.0	
t_h	hold time A_n, B_n to CP_{AB}, CP_{BA}	–	–	–	–	ns	1.2	Fig.7
		–	–	–	–		2.0	
		1.0	–	1.0	–		3.0	
f_{max}	maximum clock pulse frequency	150	–	100	–	ns	2.0	Fig.7
		200	–	150	–		3.0	

AC WAVEFORMS

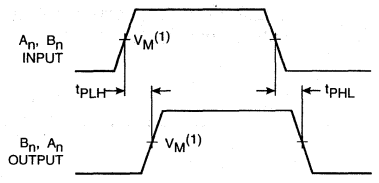


Fig.6 Waveforms showing the input A_n, B_n to output B_n, A_n propagation delays and the output transition times.

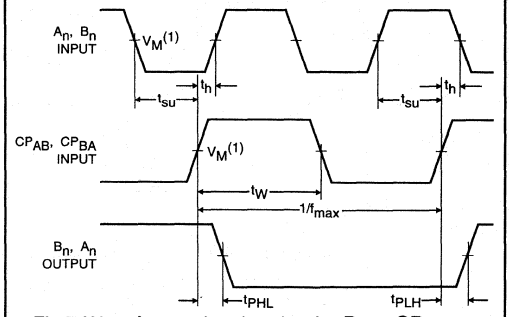


Fig.7 Waveforms showing the A_n, B_n to CP_{AB}, CP_{BA} set-up and hold times, clock CP_{AB}, CP_{BA} pulse width, maximum clock pulse frequency and the CP_{AB}, CP_{BA} to output B_n, A_n propagation delays.

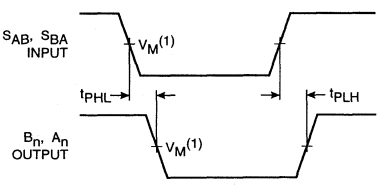


Fig.8 Waveforms showing the input S_{AB}, S_{BA} to output B_n, A_n propagation delay times and output transition times.

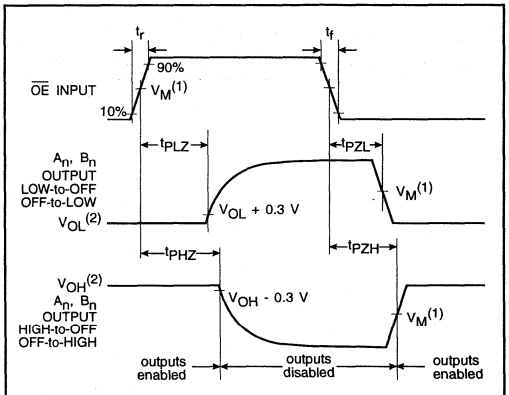


Fig.9 Waveforms showing the input $\overline{OE}$ to output A_n, B_n 3-state enable and disable times.

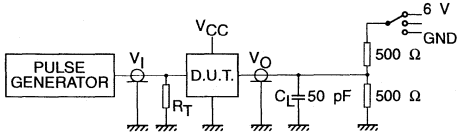


Fig.10 Test conditions: Load circuitry for enable / disable times, switch set to 6 V for t_{PLZ}/t_{PZL}, switch set to GND for t_{PHZ}/t_{PZH} otherwise do not connect.

Notes: (1) V_M = 0.6 V at V_{CC}= 1.2 V.
V_M = 1.0 V at V_{CC}= 2.0 V.
V_M = 1.5 V at V_{CC}= 3.0 V.

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-state output load.

AC WAVEFORMS *(Continued)*

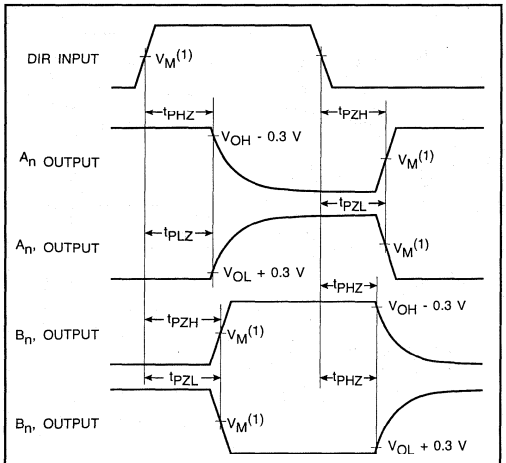


Fig.11 Waveforms showing the input DIR to output A_n, B_n 3-state enable and disable times.

Notes: (1) V_M = 0.6 V at V_{CC}= 1.2 V.
V_M = 1.0 V at V_{CC}= 2.0 V.
V_M = 1.5 V at V_{CC}= 3.0 V.

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-state output load.

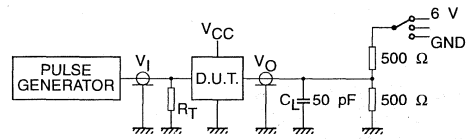
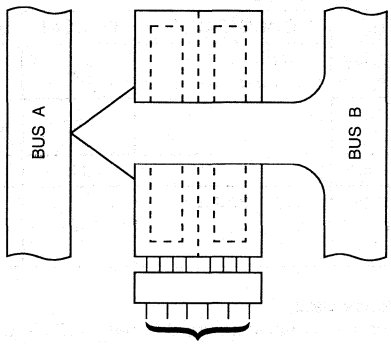


Fig.11 Test conditions: Load circuitry for enable / disable times, switch set to 6 V for t_{PLZ}/t_{PZL}, switch set to GND for t_{PHZ}/t_{PZH} otherwise do not connect.

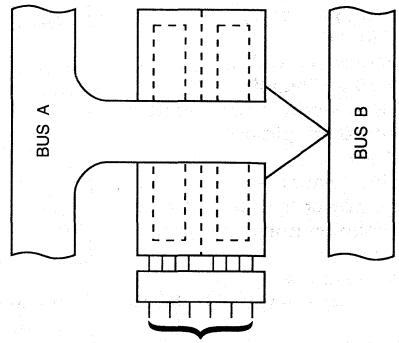
APPLICATION INFORMATION

Real-time transfer; bus B to bus A



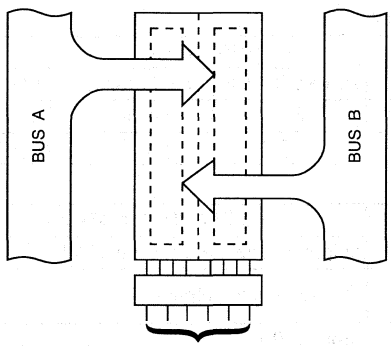
(1) $\overline{OE}$	(14) DIR	(28) CP_{AB}	(16) CP_{BA}	(27) S_{AB}	(15) S_{BA}
L	L	X	X	X	L

Real-time transfer; bus A to bus B



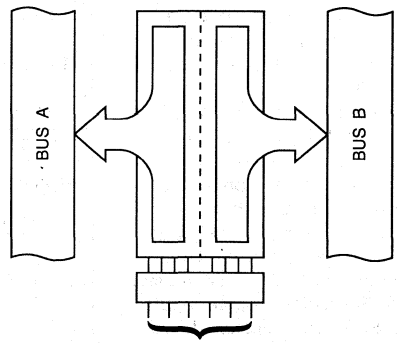
(1) $\overline{OE}$	(14) DIR	(28) CP_{AB}	(16) CP_{BA}	(27) S_{AB}	(15) S_{BA}
L	H	X	X	L	X

Storage from A, B or A and B



(1) $\overline{OE}$	(14) DIR	(28) CP_{AB}	(16) CP_{BA}	(27) S_{AB}	(15) S_{BA}
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

Transfer storage data to A or B



(1) $\overline{OE}$	(14) DIR	(28) CP_{AB}	(16) CP_{BA}	(27) S_{AB}	(15) S_{BA}
L	L	X	H or L	X	H
L	H	H or L	X	H	X

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with the JEDEC 3.3 V ±0.3 V supply**
- **CMOS low power consumption**
- **Flow-through pin-out architecture**
- **Low inductance, multiple centre power and ground pins for minimum noise and ground bounce**
- **3-state outputs**
- **Direct interface with TTL levels**

DESCRIPTION

The 74HL33648 consist of 8 inverting bus transceiver circuits with 3-state outputs, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the internal registers. Data on the 'A' or 'B' bus will be clocked in the internal registers, as the appropiate clock (CP_{AB} or CP_{BA}) goes to a HIGH logic level. Output enable ($\overline{OE}$) and direction (DIR) inputs are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the 'A' or 'B' register, or in both.The select source inputs (S_{AB} and S_{BA}) can multiplex stored and real-time (transparent mode) data. The direction (DIR) input determines which bus will receive data when $\overline{OE}$ is active (LOW). In the isolation mode ($\overline{OE}$ = HIGH), '$\overline{A}$' data may be stored in the 'B' register and/or '$\overline{B}$' data may be stored in the 'A' register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, 'A' or 'B' may be driven at a time.

The '648' is functionally identical to the '646', but has inverting data paths.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to B_n, A_n	C_L = 50 pF V_{CC} = 3.3 V	3.4	ns
f_{max}	maximum clock frequency		350	MHz
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	50	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
74HL33648D	28	SO	plastic	SOT136A
74HL33648DB	28	SSOP	plastic	SOT341

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	output enable input (active LOW)
2, 3, 4, 5, 10, 11, 12, 13	$\overline{A}_0$ to $\overline{A}_7$	'$\overline{A}$' data inputs/outputs
6, 7, 8, 9	GND	ground (0 V)
14	DIR	direction control input
15	S_{BA}	select 'B' to 'A' source input
16	CP_{BA}	'B' to 'A' clock input (Low-to-High, edge-triggered)
26, 25, 24, 23, 20, 19, 18, 17	$\overline{B}_0$ to $\overline{B}_7$	'$\overline{B}$' data inputs/outputs
21, 22	V_{CC}	positive supply voltage
27	S_{AB}	select 'A' to 'B' source input
28	CP_{AB}	'A' to 'B' clock input (Low-to-High, edge-triggered)

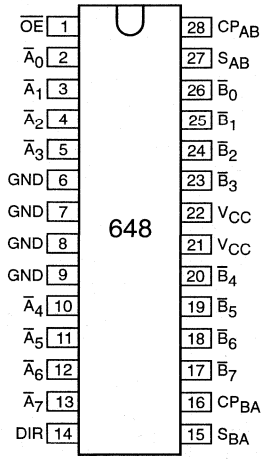


Fig.1 Pin configuration.

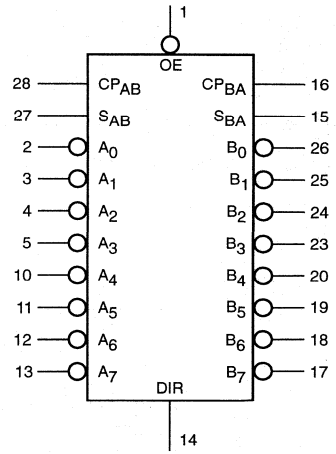


Fig.2 Logic symbol.

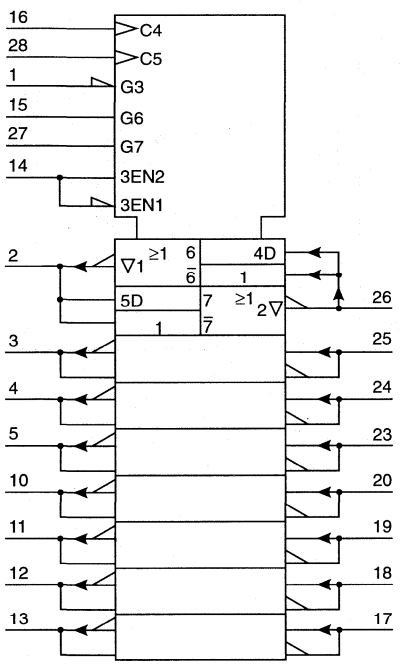


Fig.3 IEC logic symbol.

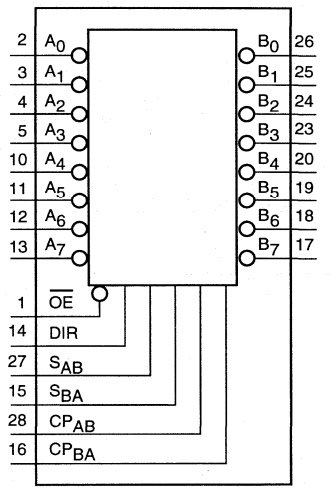


Fig.4 Functional diagram.

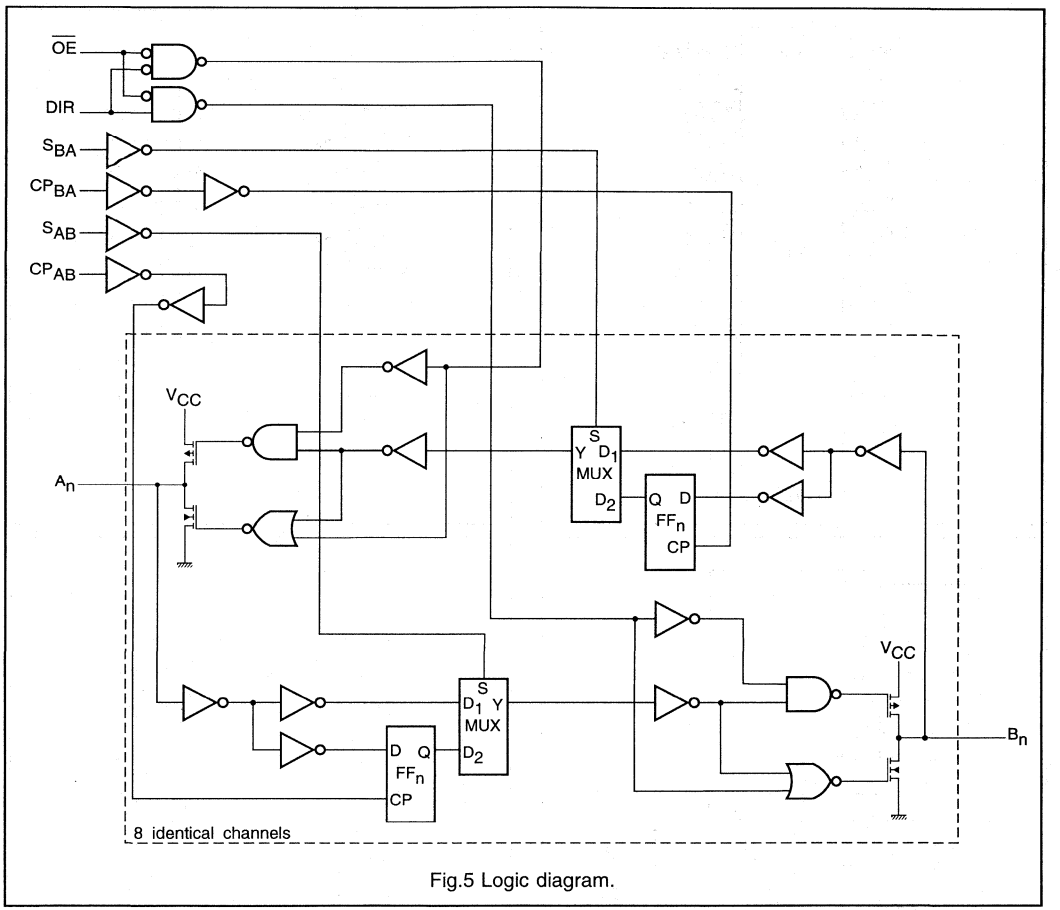


Fig.5 Logic diagram.

FUNCTION TABLE

INPUTS						DATA I/O *		FUNCTION
$\overline{OE}$	DIR	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	$\overline{A}_0$ to $\overline{A}_7$	$\overline{B}_0$ to $\overline{B}_7$	
X X	X X	↑ X	X ↑	X X	X X	input un*	un* input	store A, B unspecified* store B, A unspecified*
H H	X X	↑ H or L	↑ H or L	X X	X X	input	input	store A and B data, isolation hold storage
L L	L L	X X	X H or L	X X	L H	output	input	real-time $\overline{B}$ data to A bus stored $\overline{B}$ data to A bus
L L	H H	X H or L	X X	L H	X X	input	output	real-time $\overline{A}$ data to B bus stored $\overline{A}$ data to B bus

* The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

un = unspecified
H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH level transition

DC CHARACTERISTICS FOR 74HL33648

For the DC characteristics see chapter "HLL family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74HL33648

GND = 0 V; $t_r = t_f$ = 2.0 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)				UNIT	TEST CONDITIONS	
		+25		−40 to +85			V_{CC} (V)	WAVEFORMS
		MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to $\overline{B}_n$, $\overline{A}_n$	–	19.5	–	22.4	ns	1.2	Fig.6
		–	7.3	–	8.4		2.0	
		–	4.9	–	5.6		3.0	
t_{PHL}/t_{PLH}	propagation delay CP_{AB}, CP_{BA} to $\overline{B}_n$, $\overline{A}_n$	–	23.2	–	26.8	ns	1.2	Fig.7
		–	8.7	–	10.1		2.0	
		–	5.8	–	6.7		3.0	
t_{PHL}/t_{PLH}	propagation delay S_{AB}, S_{BA} to $\overline{B}_n$, $\overline{A}_n$	–	24.4	–	28.0	ns	1.2	Fig.8
		–	9.2	–	10.5		2.0	
		–	6.1	–	7.0		3.0	
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to $\overline{A}_n$, $\overline{B}_n$	–	24.4	–	28.0	ns	1.2	Fig.9
		–	9.2	–	10.5		2.0	
		–	6.1	–	7.0		3.0	
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to $\overline{A}_n$, $\overline{B}_n$	–	19.5	–	22.3	ns	1.2	Fig.9
		–	8.1	–	9.1		2.0	
		–	5.8	–	6.5		3.0	
t_{PZH}/t_{PZL}	3-state output enable time DIR to $\overline{A}_n$, $\overline{B}_n$	–	26.0	–	30.0	ns	1.2	Fig.10
		–	9.8	–	11.3		2.0	
		–	6.5	–	7.5		3.0	
t_{PHZ}/t_{PLZ}	3-state output disable time DIR to $\overline{A}_n$, $\overline{B}_n$	–	20.3	–	23.1	ns	1.2	Fig.10
		–	8.4	–	9.5		2.0	
		–	6.0	–	6.7		3.0	
t_W	clock pulse width HIGH or LOW CP_{AB} or CP_{BA}	3.0	–	3.7	–	ns	2.0	Figs 6 and 8
		2.0	–	2.5	–		3.0	
t_{su}	set-up time A_n, B_n to CP_{AB}, CP_{BA}	–	–	–	–	ns	1.2	Fig.7
		–	–	–	–		2.0	
		1.0	–	1.0	–		3.0	
t_h	hold time A_n, B_n to CP_{AB}, CP_{BA}	–	–	–	–	ns	1.2	Fig.7
		–	–	–	–		2.0	
		1.0	–	1.0	–		3.0	
f_{max}	maximum clock pulse frequency	150	–	100	–	ns	2.0	Fig.7
		200	–	150	–		3.0	

AC WAVEFORMS

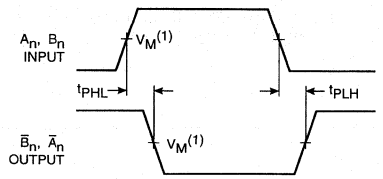


Fig.6 Waveforms showing the input A_n, B_n to output B_n, A_n propagation delays and the output transition times.

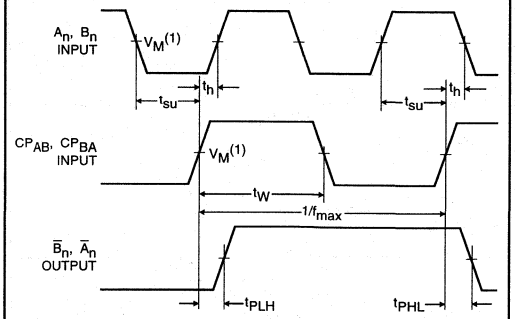


Fig.7 Waveforms showing the A_n, B_n to CP_{AB}, CP_{BA} set-up and hold times, clock CP_{AB}, CP_{BA} pulse width, maximum clock pulse frequency and the CP_{AB}, CP_{BA} to output B_n, A_n propagation delays.

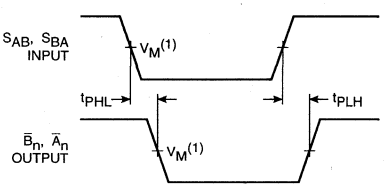


Fig.8 Waveforms showing the input S_{AB}, S_{BA} to output B_n, A_n propagation delay times and output transition times.

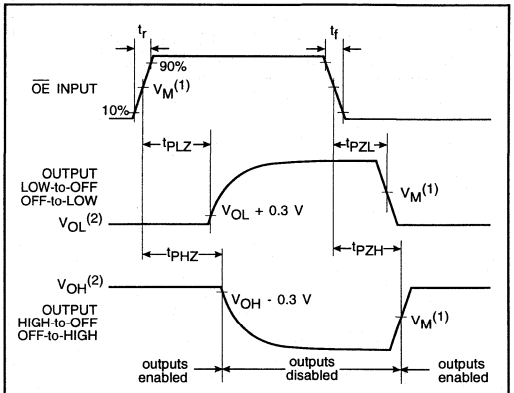


Fig.9 Waveforms showing the input $\overline{OE}$ to output A_n, B_n 3-state enable and disable times.

Notes: (1) V_M = 0.6 V at V_{CC}= 1.2 V.
V_M = 1.0 V at V_{CC}= 2.0 V.
V_M = 1.5 V at V_{CC}= 3.0 V.

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-state output load.

AC WAVEFORMS *(Continued)*

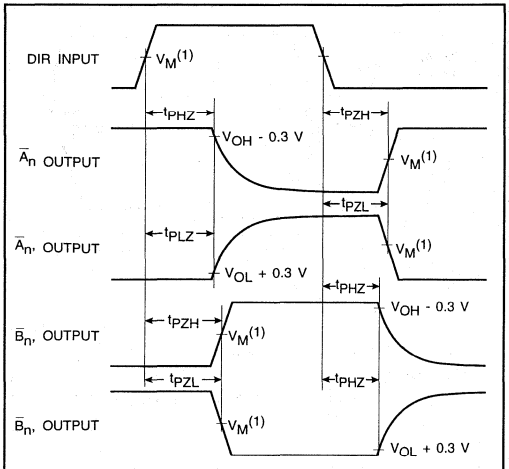


Fig.10 Waveforms showing the input DIR to output A_n, B_n 3-state enable and disable times.

Notes: (1) V_M = 0.6 V at V_{CC}= 1.2 V.
V_M = 1.0 V at V_{CC}= 2.0 V.
V_M = 1.5 V at V_{CC}= 3.0 V.

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-state output load.

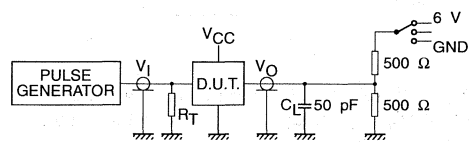
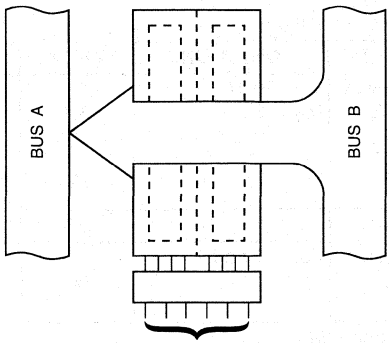


Fig.11 Test conditions: Load circuitry for enable / disable times, switch set to 6 V for t_{PLZ}/t_{PZL}, switch set to GND for t_{PHZ}/t_{PZH} otherwise do not connect.

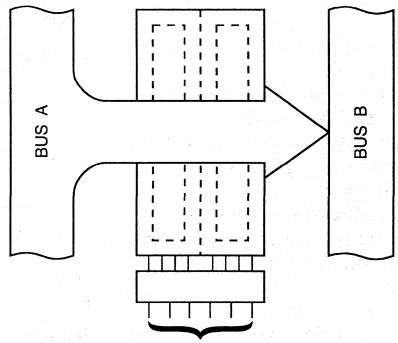
APPLICATION INFORMATION

Real-time transfer; bus B to bus A



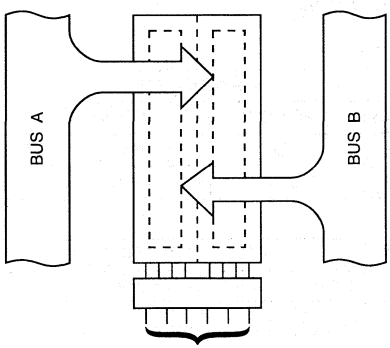
(1) $\overline{OE}$	(14) DIR	(28) CP_{AB}	(16) CP_{BA}	(27) S_{AB}	(15) S_{BA}
L	L	X	X	X	L

Real-time transfer; bus A to bus B



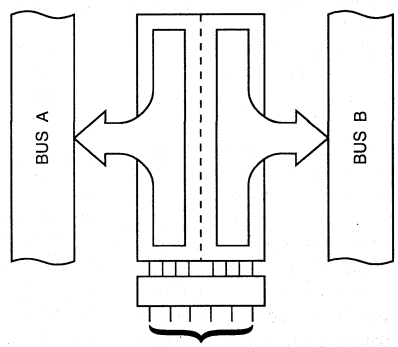
(1) $\overline{OE}$	(14) DIR	(28) CP_{AB}	(16) CP_{BA}	(27) S_{AB}	(15) S_{BA}
L	H	X	X	L	X

Storage from A, B or A and B



(1) $\overline{OE}$	(14) DIR	(28) CP_{AB}	(16) CP_{BA}	(27) S_{AB}	(15) S_{BA}
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

Transfer storage data to A or B



(1) $\overline{OE}$	(14) DIR	(28) CP_{AB}	(16) CP_{BA}	(27) S_{AB}	(15) S_{BA}
L	L	X	H or L	X	H
L	H	H or L	X	H	X

Octal transceiver/register with dual enable; 3-state; inverting

74HL33651

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with the JEDEC 3.3 V ±0.3 V supply**
- **CMOS low power consumption**
- **Flow-through pin-out architecture**
- **Low inductance, multiple centre power and ground pins for minimum noise and ground bounce**
- **3-state outputs**
- **Direct interface with TTL levels**

DESCRIPTION

The 74HL33651 consist of 8 inverting bus transceiver circuits with 3-state outputs, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Data on the "A" or "B" or both buses, will be stored in the internal registers, at the appropiate clock inputs (CP_{AB} or CP_{BA}) regardless of the select inputs (S_{AB} and S_{BA}) or output enable (OE_{AB} and $\overline{OE}_{BA}$) control inputs. Depending on the select inputs S_{AB} and S_{BA} data can directly go from input to output (real time mode) or data can be controlled by the clock (storage mode), this is when the OE_n inputs this operating mode permits. The output enable inputs OE_{AB} and $\overline{OE}_{BA}$ determine the operation mode of the transceiver. When OE_{AB} is LOW, no data transmission from A_n to B_n is possible and when $\overline{OE}_{BA}$ is HIGH, there is no data transmission from B_n to A_n possible. When S_{AB} and S_{BA} are in the real time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OE_{AB} and $\overline{OE}_{BA}$. In this configuration each output reinforces its input.

The '651' is functionally identical to the '652', but has inverting data paths.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to B_n, A_n	C_L = 50 pF V_{CC} = 3.3 V	3.4	ns
f_{max}	maximum clock frequency		350	MHz
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	50	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
74HL33651D	28	SO	plastic	SOT136A
74HL33651DB	28	SSOP	plastic	SOT341

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	OE_{AB}	output enable A to B input
2, 3, 4, 5, 10, 11, 12, 13	$\overline{A}_0$ to $\overline{A}_7$	'A' data inputs/outputs
6, 7, 8, 9	GND	ground (0 V)
14	$\overline{OE}_{BA}$	output enable B to A input (active LOW)
15	S_{BA}	select 'B' to 'A' source input
16	CP_{BA}	'B' to 'A' clock input (Low-to-High, edge-triggered)
26, 25, 24, 23, 20, 19, 18, 17	$\overline{B}_0$ to $\overline{B}_7$	'B' data inputs/outputs
21, 22	V_{CC}	positive supply voltage
27	S_{AB}	select 'A' to 'B' source input
28	CP_{AB}	'A' to 'B' clock input (Low-to-High, edge-triggered)

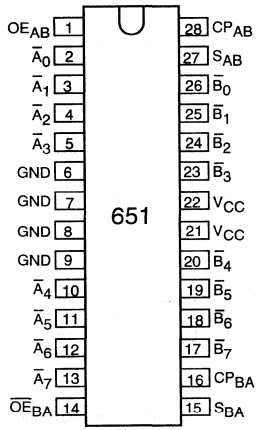


Fig.1 Pin configuration.

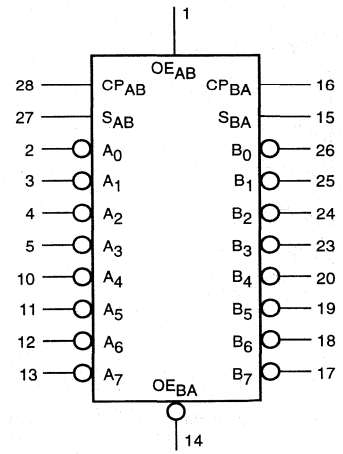


Fig.2 Logic symbol.

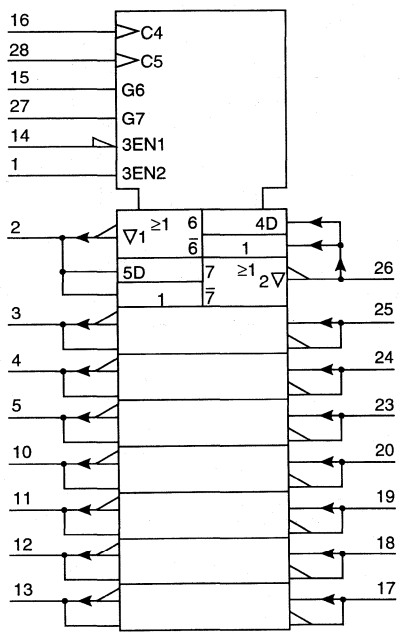


Fig3. IEC logic symbol.

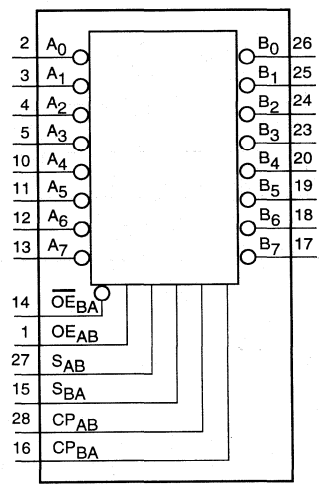


Fig.4 Functional diagram.

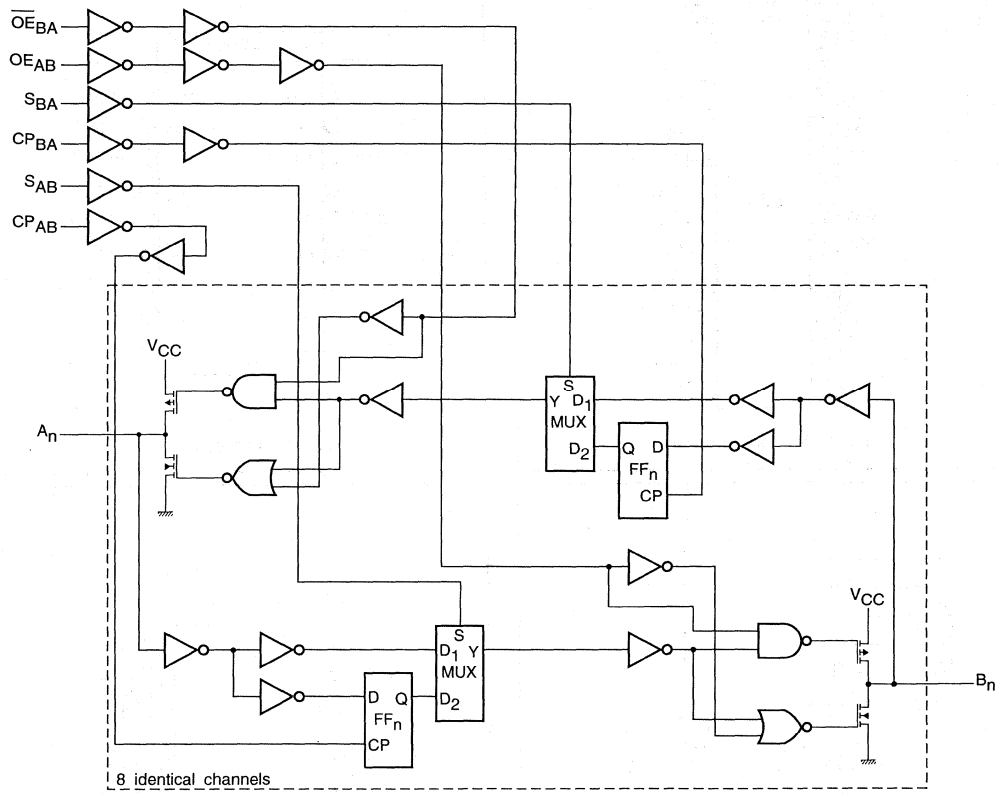


Fig.5 Logic diagram.

FUNCTION TABLE

INPUTS						DATA I/O *		FUNCTION
OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	$\overline{A}_0$ to $\overline{A}_7$	$\overline{B}_0$ to $\overline{B}_7$	
L L	H H	H or L ↑	H or L ↑	X X	X X	input	input	isolation store $\overline{A}$ and $\overline{B}$ data
X H	H H	↑ ↑	H or L ↑	X L	X X	input input	un* output	store A, hold B store A in both registers
L L	X L	H or L ↑	↑ ↑	X X	X L	un* output	input input	hold A, store B store B in both registers
L L	L L	X X	X H or L	X X	L H	output	input	real time $\overline{B}$ data to A bus stored $\overline{B}$ data to A bus
H H	H H	X H or L	X X	L H	X X	input	output	real-time $\overline{A}$ data to B bus stored $\overline{A}$ data to B bus
H	L	H or L	H or L	H	H	output	output	stored $\overline{A}$ data to B bus and stored $\overline{B}$ data to A bus

* The data output functions may be enabled or disabled by various signals at the OE_{AB} and $\overline{OE}_{BA}$ inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

un = unspecified
H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH level transition

DC CHARACTERISTICS FOR 74HL33651

For the DC characteristics see chapter "HLL family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74HL33651

GND = 0 V; $t_r = t_f$ = 2.0 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)				UNIT	TEST CONDITIONS	
		+25		−40 to +85			V_{CC} (V)	WAVEFORMS
		MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay $\overline{A}_n$, $\overline{B}_n$ to $\overline{B}_n$, $\overline{A}_n$	–	19.5	–	22.4	ns	1.2	Fig.6
		–	7.3	–	8.4		2.0	
		–	4.9	–	5.6		3.0	
t_{PHL}/t_{PLH}	propagation delay CP_{AB}, CP_{BA} to $\overline{B}_n$, $\overline{A}_n$	–	23.2	–	26.8	ns	1.2	Fig.7
		–	8.7	–	10.1		2.0	
		–	5.8	–	6.7		3.0	
t_{PHL}/t_{PLH}	propagation delay S_{AB}, S_{BA} to $\overline{B}_n$, $\overline{A}_n$	–	24.4	–	28.0	ns	1.2	Fig.8
		–	9.2	–	10.5		2.0	
		–	6.1	–	7.0		3.0	
t_{PZH}/t_{PZL}	3-state output enable time OE_{AB} to $\overline{B}_n$	–	22.0	–	25.2	ns	1.2	Fig.9
		–	8.3	–	7.8		2.0	
		–	5.5	–	6.3		3.0	
t_{PHZ}/t_{PLZ}	3-state output disable time OE_{AB} to $\overline{B}_n$	–	17.5	–	20.2	ns	1.2	Fig.9
		–	7.3	–	8.4		2.0	
		–	5.3	–	6.0		3.0	
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_{BA}$ to $\overline{A}_n$	–	22.0	–	25.2	ns	1.2	Fig.9
		–	8.3	–	9.5		2.0	
		–	5.5	–	6.3		3.0	
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_{BA}$ to $\overline{A}_n$	–	17.5	–	20.3	ns	1.2	Fig.9
		–	7.4	–	8.4		2.0	
		–	5.3	–	6.0		3.0	
t_W	clock pulse width HIGH or LOW CP_{AB} or CP_{BA}	3.0	–	3.7	–	ns	2.0	Figs 6 and 8
		2.0	–	2.5	–		3.0	
t_{su}	set-up time $\overline{A}_n$, $\overline{B}_n$ to CP_{AB}, CP_{BA}	–	–	–	–	ns	1.2	Fig.7
		–	–	–	–		2.0	
		1.0	–	1.0	–		3.0	
t_h	hold time $\overline{A}_n$, $\overline{B}_n$ to CP_{AB}, CP_{BA}	–	–	–	–	ns	1.2	Fig.7
		–	–	–	–		2.0	
		1.0	–	1.0	–		3.0	
f_{max}	maximum clock pulse frequency	150	–	100	–	MHz	2.0	Fig.7
		200	–	150	–		3.0	

AC WAVEFORMS

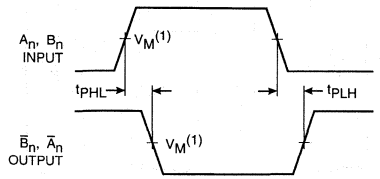


Fig.6 Waveforms showing the input A_n, B_n to output B_n, A_n propagation delays and the output transition times.

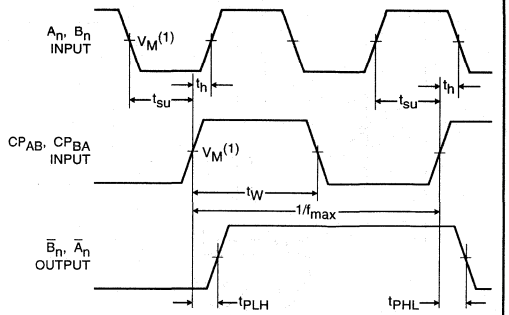


Fig.7 Waveforms showing the A_n, B_n to CP_{AB}, CP_{BA} set-up and hold times, clock CP_{AB}, CP_{BA} pulse width, maximum clock pulse frequency and the CP_{AB}, CP_{BA} to output B_n, A_n propagation delays.

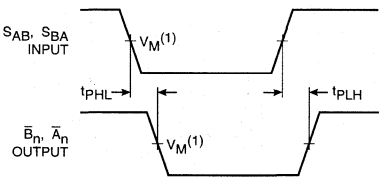


Fig.8 Waveforms showing the input S_{AB}, S_{BA} to output B_n, A_n propagation delay times and output transition times.

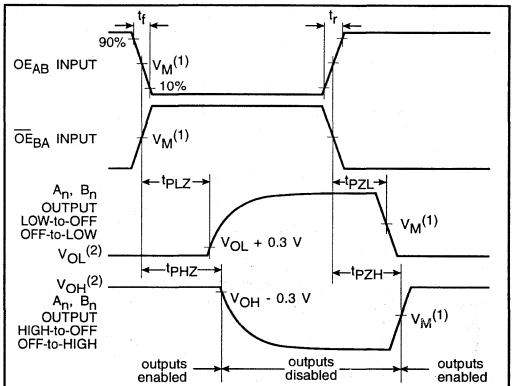


Fig.9 Waveforms showing the OE inputs (OE_{AB}, $\overline{OE}_{BA}$) to outputs A_n, B_n enable and disable times and the input rise and fall times.

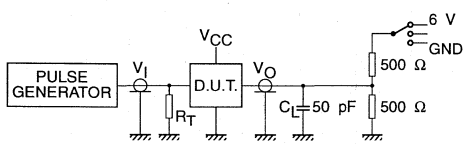


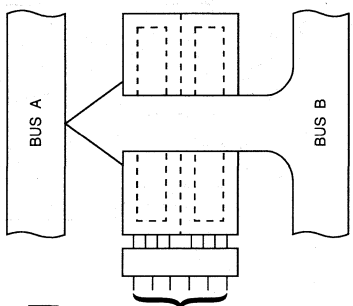
Fig.10 Test conditions: Load circuitry for enable / disable times, switch set to 6 V for t_{PLZ}/t_{PZL}, switch set to GND for t_{PHZ}/t_{PZH} otherwise do not connect.

Notes: (1) V_M = 0.6 V at V_{CC}= 1.2 V.
V_M = 1.0 V at V_{CC}= 2.0 V.
V_M = 1.5 V at V_{CC}= 3.0 V.

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-state output load.

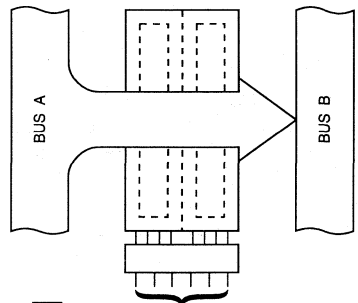
APPLICATION INFORMATION

Real-time transfer; bus B to bus A



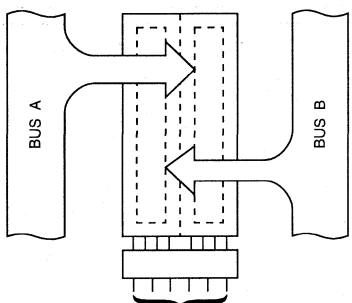
OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
L	L	X	X	X	L

Real-time transfer; bus A to bus B



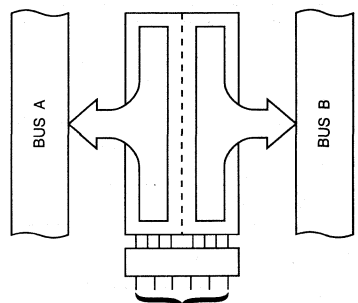
OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
H	H	X	X	L	X

Store A, B or A and B in one register



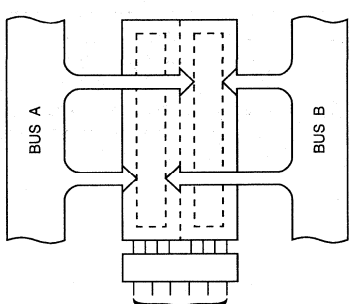
OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

Transfer A stored data to B bus or B stored data to A bus or both at the same time



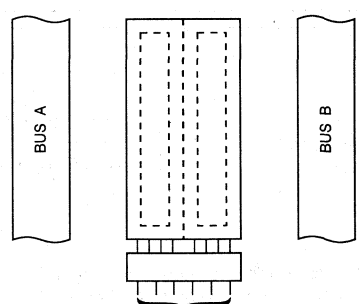
OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
H	H	H or L	X	H	X
L	L	X	H or L	X	H
H	L	H or L	H or L	H	H

Store bus A in both registers or store bus B in both registers



OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
H	H	↑	↑	L	X
L	L	↑	↑	X	L

Isolation



OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
L	H	H or L	H or L	X	X

Octal transceiver/register with dual enable; 3-state 74HL33652

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with the JEDEC 3.3 V ±0.3 V supply**
- **CMOS low power consumption**
- **Flow-through pin-out architecture**
- **Low inductance, multiple centre power and ground pins for minimum noise and ground bounce**
- **3-state outputs**
- **Direct interface with TTL levels**

DESCRIPTION

The 74HL33652 consist of 8 non-inverting bus transceiver circuits with 3-state outputs, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Data on the 'A' or 'B' or both buses, will be stored in the internal registers, at the appropiate clock inputs (CP_{AB} or CP_{BA}) regardless of the select inputs (S_{AB} and S_{BA}) or output enable (OE_{AB} and $\overline{OE}_{BA}$) control inputs. Depending on the select inputs S_{AB} and S_{BA} data can directly go from input to output (real time mode) or data can be controlled by the clock (storage mode), this is when the OE_n inputs this operating mode permits. The output enable inputs OE_{AB} and $\overline{OE}_{BA}$ determine the operation mode of the transceiver. When OE_{AB} is LOW, no data transmission from A_n to B_n is possible and when $\overline{OE}_{BA}$ is HIGH, there is no data transmission from B_n to A_n possible. When S_{AB} and S_{BA} are in the real time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OE_{AB} and $\overline{OE}_{BA}$. In this configuration each output reinforces its input.

The '652' is functionally identical to the '651', but has non-inverting data paths.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to B_n, A_n	C_L = 50 pF V_{CC} = 3.3 V	3.2	ns
f_{max}	maximum clock frequency		350	MHz
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	50	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74HL33652D	28	SO	plastic	SO28/SOT136A
74HL33652DB	28	SSOP	plastic	SSOP28/SOT341

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	OE_{AB}	output enable A to B input
2, 3, 4, 5, 10, 11, 12, 13	A_0 to A_7	'A' data inputs/outputs
6, 7, 8, 9	GND	ground (0 V)
14	$\overline{OE}_{BA}$	output enable B to A input (active LOW)
15	S_{BA}	select 'B' to 'A' source input
16	CP_{BA}	'B' to 'A' clock input (Low-to-High, edge-triggered)
26, 25, 24, 23, 20, 19, 18, 17	B_0 to B_7	'B' data inputs/outputs
21, 22	V_{CC}	positive supply voltage
27	S_{AB}	select 'A' to 'B' source input
28	CP_{AB}	'A' to 'B' clock input (Low-to-High, edge-triggered)

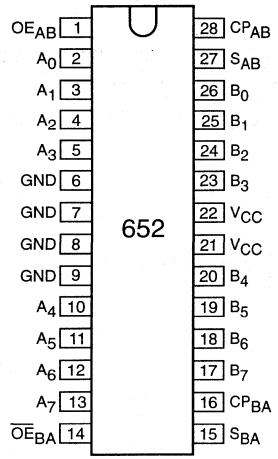


Fig.1 Pin configuration.

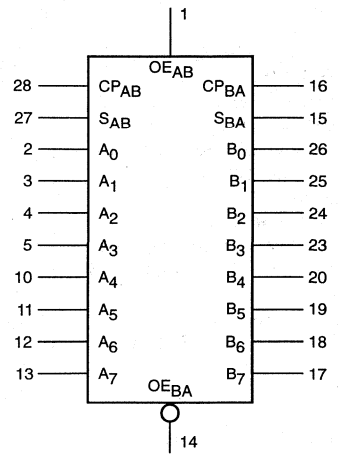


Fig.2 Logic symbol.

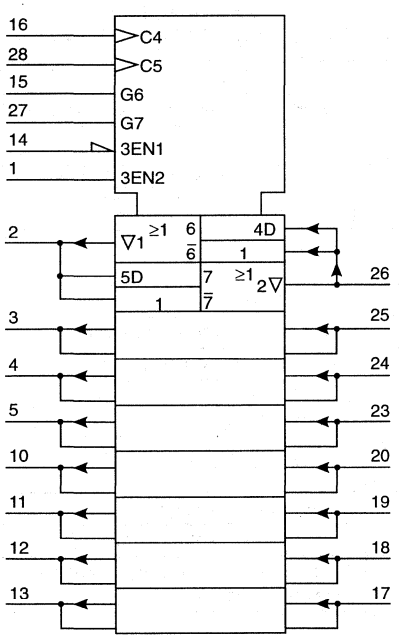


Fig3. IEC logic symbol.

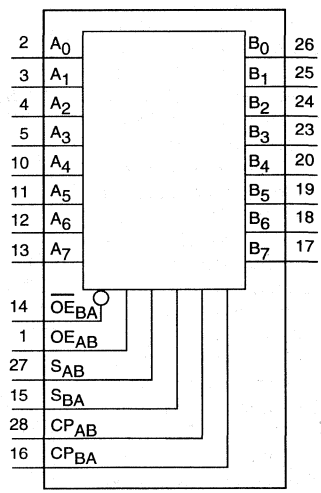


Fig.4 Functional diagram.

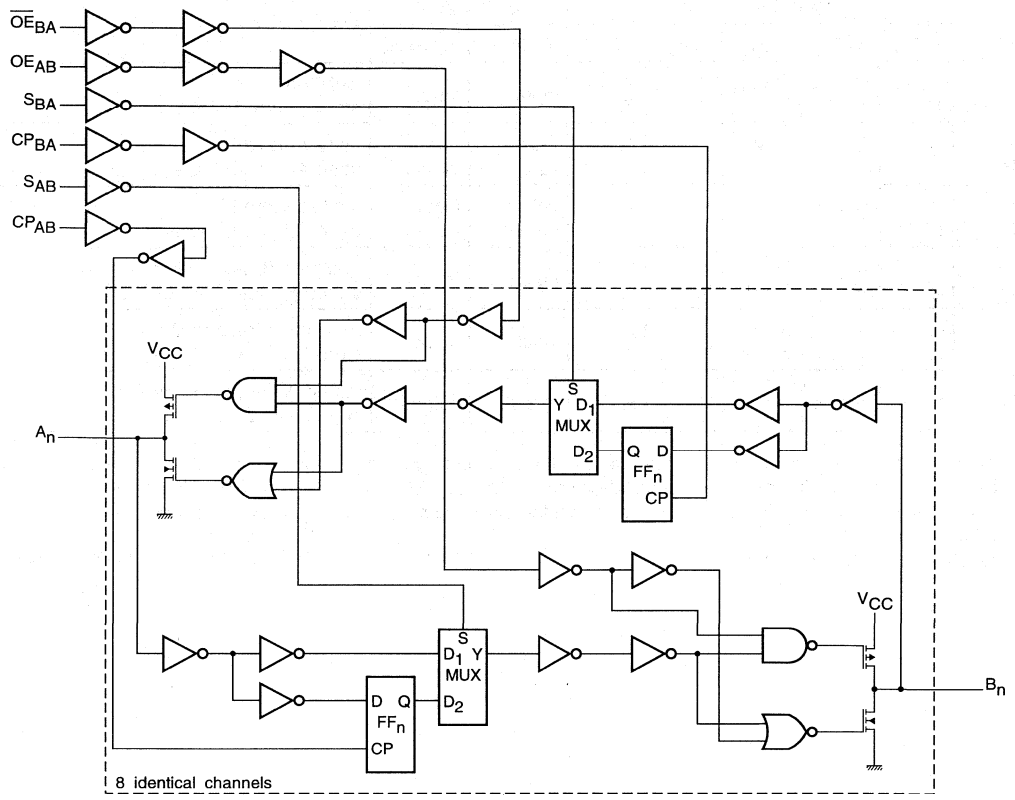


Fig.5 Logic diagram.

FUNCTION TABLE

INPUTS						DATA I/O *		FUNCTION
OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	A_0 to A_7	B_0 to B_7	
L L	H H	H or L ↑	H or L ↑	X X	X X	input	input	isolation store A and B data
X H	H H	↑ ↑	H or L ↑	X L	X X	input input	un* output	store A, hold B store A in both registers
L L	X L	H or L ↑	↑ ↑	X X	X L	un* output	input input	hold A, store B store B in both registers
L L	L L	X X	X H or L	X X	L H	output	input	real time B data to A bus stored B data to A bus
H H	H H	X H or L	X X	L H	X X	input	output	real-time A data to B bus stored A data to B bus
H	L	H or L	H or L	H	H	output	output	stored A data to B bus and stored B data to A bus

* The data output functions may be enabled or disabled by various signals at the OE_{AB} and $\overline{OE}_{BA}$ inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

un = unspecified
H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH level transition

DC CHARACTERISTICS FOR 74HL33652

For the DC characteristics see chapter "HLL family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74HL33652

GND = 0 V; $t_r = t_f$ = 2.0 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)				UNIT	TEST CONDITIONS	
		+25		−40 to +85			V_{CC} (V)	WAVEFORMS
		MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to B_n, A_n	–	19.2	–	22.0	ns	1.2	Fig.6
		–	7.2	–	8.3		2.0	
		–	4.8	–	5.5		3.0	
t_{PHL}/t_{PLH}	propagation delay CP_{AB}, CP_{BA} to B_n, A_n	–	23.2	–	26.8	ns	1.2	Fig.7
		–	8.7	–	10.1		2.0	
		–	5.8	–	6.7		3.0	
t_{PHL}/t_{PLH}	propagation delay S_{AB}, S_{BA} to B_n, A_n	–	24.4	–	28.0	ns	1.2	Fig.8
		–	9.2	–	10.5		2.0	
		–	6.1	–	7.0		3.0	
t_{PZH}/t_{PZL}	3-state output enable time OE_{AB} to B_n	–	22.0	–	25.2	ns	1.2	Fig.9
		–	8.3	–	7.8		2.0	
		–	5.5	–	6.3		3.0	
t_{PHZ}/t_{PLZ}	3-state output disable time OE_{AB} to B_n	–	17.5	–	20.2	ns	1.2	Fig.9
		–	7.3	–	8.4		2.0	
		–	5.3	–	6.0		3.0	
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_{BA}$ to A_n	–	22.0	–	25.2	ns	1.2	Fig.9
		–	8.3	–	9.5		2.0	
		–	5.5	–	6.3		3.0	
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_{BA}$ to A_n	–	17.5	–	20.3	ns	1.2	Fig.9
		–	7.4	–	8.4		2.0	
		–	5.3	–	6.0		3.0	
t_W	clock pulse width HIGH or LOW CP_{AB} or CP_{BA}	3.0	–	3.7	–	ns	2.0	Figs 6 and 8
		2.0	–	2.5	–		3.0	
t_{su}	set-up time A_n, B_n to CP_{AB}, CP_{BA}	–	–	–	–	ns	1.2	Fig.7
		–	–	–	–		2.0	
		1.0	–	1.0	–		3.0	
t_h	hold time A_n, B_n to CP_{AB}, CP_{BA}	–	–	–	–	ns	1.2	Fig.7
		–	–	–	–		2.0	
		1.0	–	1.0	–		3.0	
f_{max}	maximum clock pulse frequency	150	–	100	–	MHz	2.0	Fig.7
		200	–	150	–		3.0	

AC WAVEFORMS

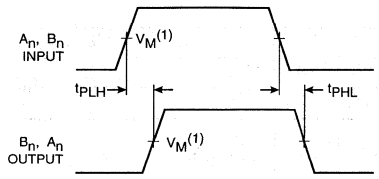


Fig.6 Waveforms showing the input A_n, B_n to output B_n, A_n propagation delays and the output transition times.

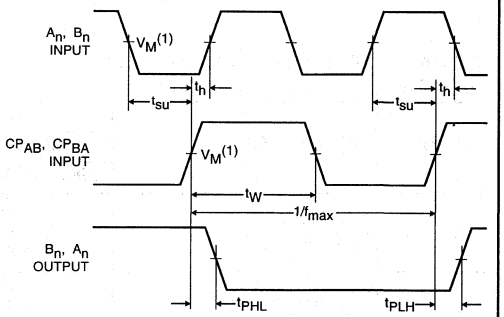


Fig.7 Waveforms showing the A_n, B_n to CP_{AB}, CP_{BA} set-up and hold times, clock CP_{AB}, CP_{BA} pulse width, maximum clock pulse frequency and the CP_{AB}, CP_{BA} to output B_n, A_n propagation delays.

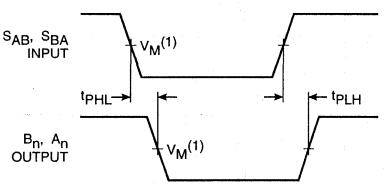


Fig.8 Waveforms showing the input S_{AB}, S_{BA} to output B_n, A_n propagation delay times and output transition times.

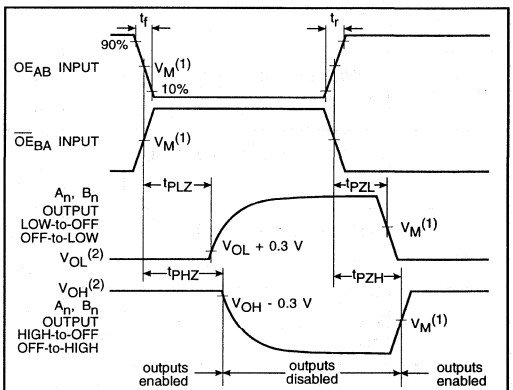


Fig.9 Waveforms showing the OE inputs (OE_{AB}, $\overline{OE}_{BA}$) to outputs A_n, B_n enable and disable times and the input rise and fall times.

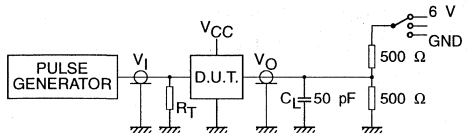


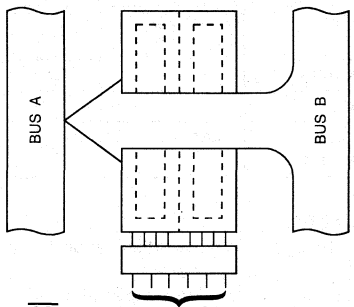
Fig.10 Test conditions: Load circuitry for enable / disable times, switch set to 6 V for t_{PLZ}/t_{PZL}, switch set to GND for t_{PHZ}/t_{PZH} otherwise do not connect.

Notes: (1) V_M = 0.6 V at V_{CC}= 1.2 V.
V_M = 1.0 V at V_{CC}= 2.0 V.
V_M = 1.5 V at V_{CC}= 3.0 V.

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-state output load.

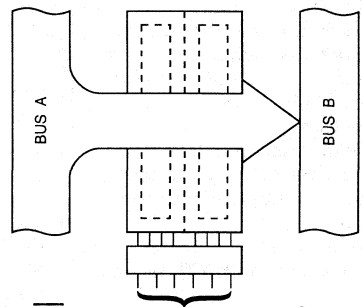
APPLICATION INFORMATION

Real-time transfer; bus B to bus A



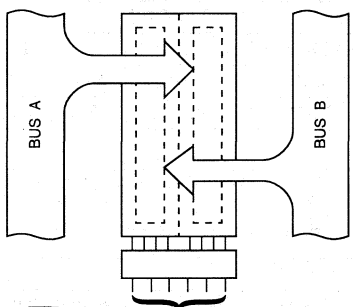
OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
L	L	X	X	X	L

Real-time transfer; bus A to bus B



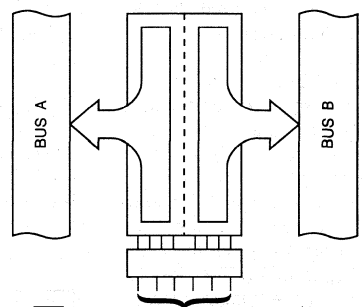
OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
H	H	X	X	L	X

Store A, B or A and B in one register



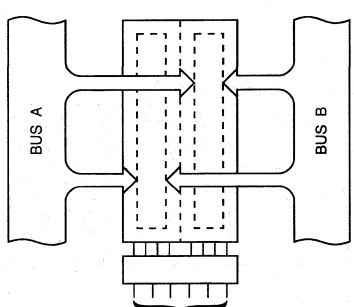
OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

Transfer A stored data to B bus or B stored data to A bus or both at the same time



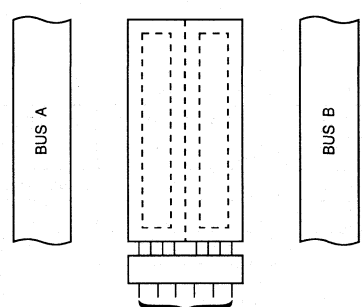
OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
H	H	H or L	X	H	X
L	L	X	H or L	X	H
H	L	H or L	H or L	H	H

Store bus A in both registers or store bus B in both registers



OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
H	H	↑	↑	L	X
L	L	↑	↑	X	L

Isolation



OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
L	H	H or L	H or L	X	X

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with the JEDEC 3.3 V ±0.3 V supply**
- **CMOS low power consumption**
- **Flow-through pin-out architecture**
- **Low inductance, multiple centre power and ground pins for minimum noise and ground bounce**
- **3-state outputs**
- **Direct interface with TTL levels**

DESCRIPTION

The 74HL33952 is a high-performance, low-power, low-voltage, Si-gate CMOS device superior to most advanced CMOS compatible TTL families.

The 74HL33952 is an octal non-inverting registered transceiver. Two 8-bit back to back registers store data flowing in both directions between two bi-directional busses. Data applied to the inputs is entered and stored on the rising edge of the clock (CP_{nn}) provided that the clock enable ($\overline{CE}_{nn}$) is LOW. The data is then present at the 3-state output buffers, but is only accessible when the output enable input ($\overline{OE}_{nn}$) is LOW. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.
The '952' is identical to the '953' but has non-inverting outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay CP_{nn} to A_n, B_n	C_L = 50 pF; V_{CC} = 3.3 V	3.2	ns
f_{max}	maximum clock frequency		350	MHz
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	35	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74HL33952D	28	SO	plastic	SO28/SOT136A
74HL33952DB	28	SSOP	plastic	SSOP28/SOT341

PINNING

PIN	SYMBOL	NAME AND FUNCTION
12, 11, 10, 5, 4, 3, 2, 1	B_0 to B_7	B data inputs/outputs
6, 7, 8, 9	GND	ground (0 V)
13, 18	$\overline{OE}_{AB}$, $\overline{OE}_{BA}$	output enable inputs (active LOW)
14, 17	CP_{AB}, CP_{BA}	clock inputs
15, 16	$\overline{CE}_{AB}$, $\overline{CE}_{BA}$	clock enable inputs
19, 20, 23, 24, 25, 26, 27, 28	A_0 to A_7	A data inputs/outputs
21, 22	V_{CC}	positive supply voltage

FUNCTION TABLE for register A_n or B_n

INPUTS			INTERNAL Q	OPERATING MODE
A_n or B_n	CP_{nn}	$\overline{CE}_{nn}$		
X	X	H	NC	Hold data
L	↑	L	L	Load data
H	↑	L	H	Load data

H = HIGH voltage level
L = LOW voltage level
↑ = Low-to-High transition

FUNCTION TABLE for output enable

INPUTS	INTERNAL Q	A_n or B_n OUTPUTS	OPERATING MODE
$\overline{OE}_{nn}$			
H	X	Z	disable outputs
L	L	L	enable outputs
L	H	H	enable outputs

NC = no change
X = don't care
Z = high impedance OFF-state

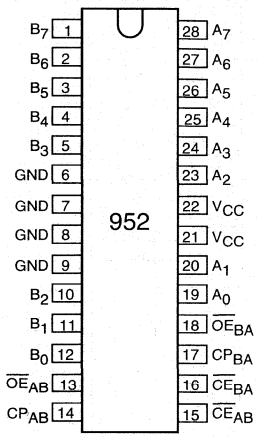


Fig.1 Pin configuration.

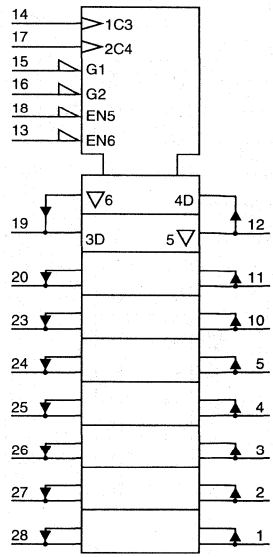


Fig.2 IEC logic symbol.

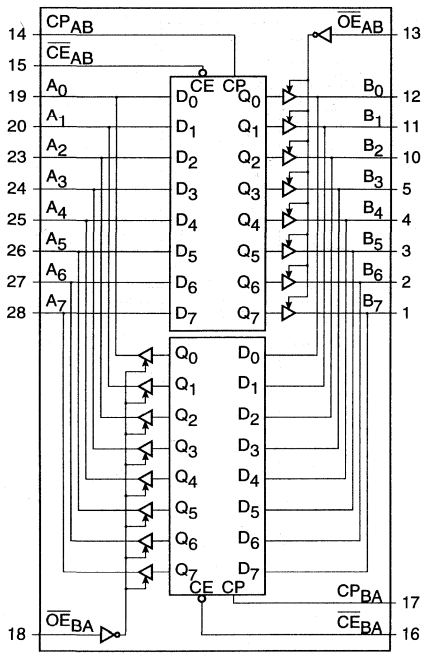


Fig.3 Logic symbol.

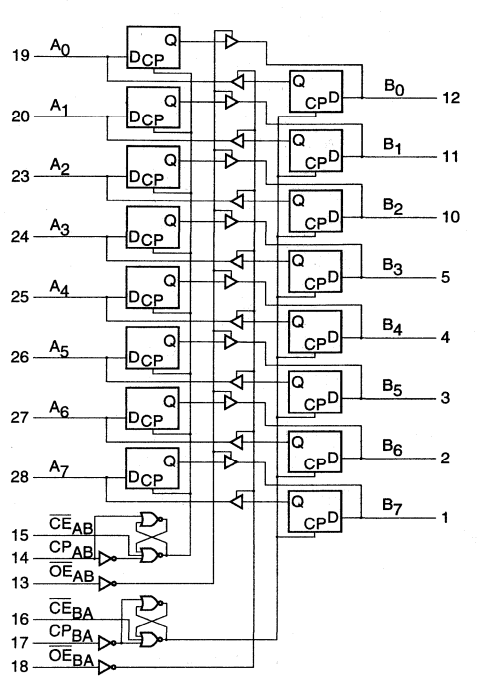


Fig.4 Functional diagram.

DC CHARACTERISTICS FOR 74HL33952

For the DC characteristics see chapter "HLL family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74HL33952

GND = 0 V; $t_r = t_f$ = 2.0 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)				UNIT	TEST CONDITIONS	
		+25		−40 to +85			V_{CC} (V)	WAVEFORMS
		MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay CP_{BA}, CP_{AB} to A_n, B_n	–	60	–	70	ns	1.2	Fig. 5
		–	8.9	–	11		2.0	
		–	5.9	–	6.8		3.0	
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_{BA}$, $\overline{OE}_{AB}$ to A_n, B_n	–	23	–	27	ns	1.2	Fig. 7
		–	8.6	–	9.9		2.0	
		–	5.7	–	6.6		3.0	
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_{BA}$, $\overline{OE}_{AB}$ to A_n, B_n	–	19	–	21	ns	1.2	Fig. 7
		–	7.7	–	8.6		2.0	
		–	5.9	–	6.6		3.0	
t_W	CP_{AB}, CP_{BA} pulse width, HIGH or LOW	2.0	–	2.4	–	ns	2.0	Fig. 5
		1.3	–	1.6	–		3.0	
t_{su}	set-up time, HIGH or LOW A_n, B_n to CP_{AB}, CP_{BA}	−0.8	–	−0.9	–	ns	2.0	Fig. 6
		−0.5	–	−0.6	–		3.0	
t_{su}	set-up time, HIGH or LOW $\overline{CE}_{AB}$, $\overline{CE}_{BA}$ to CP_{AB}, CP_{BA}	2.3	–	2.3	–	ns	2.0	Fig. 6
		1.3	–	1.5	–		3.0	
t_h	hold time A_n, B_n to CP_{AB}, CP_{BA}	0.9	–	1.1	–	ns	2.0	Fig. 6
		0.6	–	0.7	–		3.0	
t_h	hold time $\overline{CE}_{AB}$, $\overline{CE}_{BA}$ to CP_{AB}, CP_{BA}	1.7	–	2.0	–	ns	2.0	Fig. 6
		1.1	–	1.3	–		3.0	
f_{max}	maximum clock pulse frequency	166	–	140	–	MHz	2.0	Fig. 5
		250	–	200	–		3.0	

AC WAVEFORMS

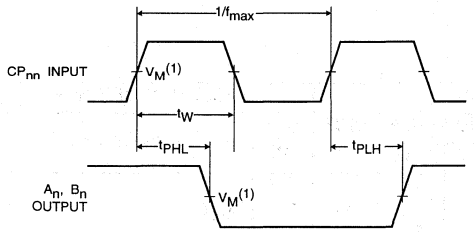


Fig. 5 Waveforms showing the clock input (CP_{BA}, CP_{AB}) to output (B_n, A_n) propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency.

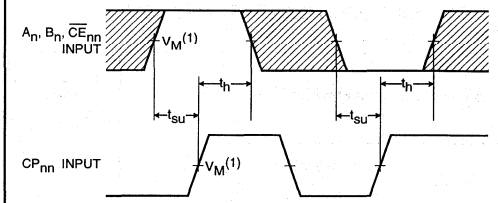


Fig.6 Waveforms showing the set-up and hold times for the A_n, B_n and $\overline{CE}_{nn}$ inputs.

Note to Fig.6

The shaded areas indicate when the input is permitted to change for predictable output performance.

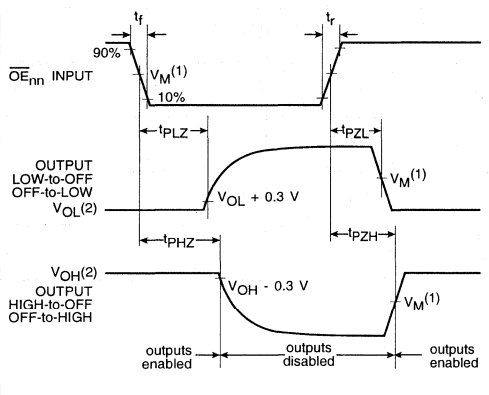


Fig.7 Waveforms showing the 3-state enable and disable times.

Notes: (1) V_M = 0.6 V at V_{CC}= 1.2 V.
V_M = 1.0 V at V_{CC}= 2.0 V.
V_M = 1.5 V at V_{CC}= 3.0 V.

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-state output load.

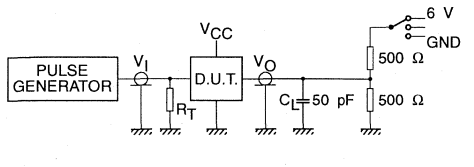


Fig.8 Test conditions: Load circuitry for enable / disable times, switch set to 6 V for t_{PLZ}/t_{PZL}, switch set to GND for t_{PHZ}/t_{PZH} otherwise do not connect.

Octal registered transceiver; 3-state; inverting — 74HL33953

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with the JEDEC 3.3 V ±0.3 V supply**
- **CMOS low power consumption**
- **Flow-through pin-out architecture**
- **Low inductance, multiple centre power and ground pins for minimum noise and ground bounce**
- **3-state outputs**
- **Direct interface with TTL levels**

DESCRIPTION

The 74HL33953 is a high-performance, low-power, low-voltage, Si-gate CMOS device superior to most advanced CMOS compatible TTL families.

The 74HL33953 is an octal inverting registered transceiver. Two 8-bit back to back registers store data flowing in both directions between two bi-directional busses. Data applied to the inputs is entered and stored on the rising edge of the clock (CP_{nn}) provided that the clock enable ($\overline{CE}_{nn}$) is LOW. The data is then present at the 3-state output buffers, but is only accessible when the output enable input ($\overline{OE}_{nn}$) is LOW. Data flow from A inputs to $\overline{B}$ outputs is the same as for B inputs to $\overline{A}$ outputs.
The '953' is identical to the '952' but has inverting outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay CP_{nn} to $\overline{A}_n$, $\overline{B}_n$	C_L = 50 pF; V_{CC} = 3.3 V	3.2	ns
f_{max}	maximum clock frequency		350	MHz
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	35	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74HL33953D	28	SO	plastic	SO28/SOT136A
74HL33953DB	28	SSOP	plastic	SSOP28/SOT341

PINNING

PIN	SYMBOL	NAME AND FUNCTION
12, 11, 10, 5, 4, 3, 2, 1	$\overline{B}_0$ to $\overline{B}_7$	B data inputs/outputs
6, 7, 8, 9	GND	ground (0 V)
13, 18	$\overline{OE}_{AB}$, $\overline{OE}_{BA}$	output enable inputs (active LOW)
14, 17	CP_{AB}, CP_{BA}	clock inputs
15, 16	$\overline{CE}_{AB}$, $\overline{CE}_{BA}$	clock enable inputs
19, 20, 23, 24, 25, 26, 27, 28	$\overline{A}_0$ to $\overline{A}_7$	A data inputs/outputs
21, 22	V_{CC}	positive supply voltage

FUNCTION TABLE for register A_n or B_n

INPUTS			INTERNAL Q	OPERATING MODE
A_n or B_n	CP_{nn}	$\overline{CE}_{nn}$		
X	X	H	NC	Hold data
L	↑	L	L	Load data
H	↑	L	H	Load data

H = HIGH voltage level
L = LOW voltage level
↑ = Low-to-High transition

FUNCTION TABLE for output enable

INPUTS	INTERNAL Q	$\overline{A}_n$ or $\overline{B}_n$ OUTPUTS	OPERATING MODE
$\overline{OE}_{nn}$			
H	X	Z	disable outputs
L	L	H	enable outputs
L	H	L	enable outputs

NC = no change
X = don't care
Z = high impedance OFF-state

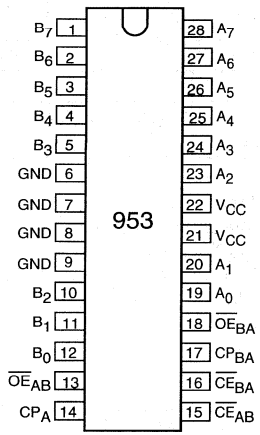


Fig.1 Pin configuration.

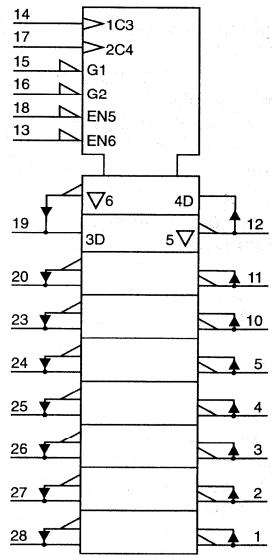


Fig.2 IEC logic symbol.

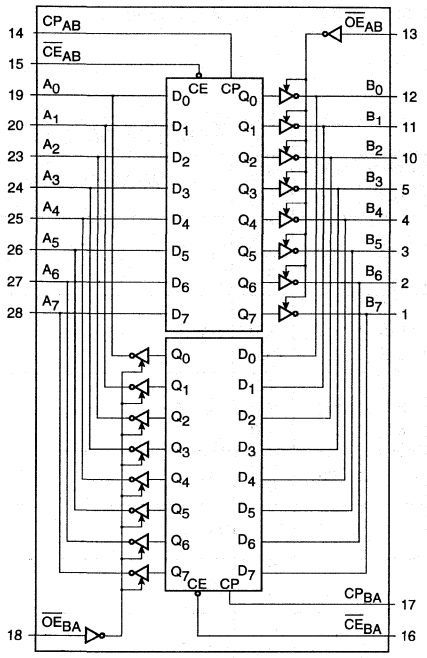


Fig.3 Logic symbol.

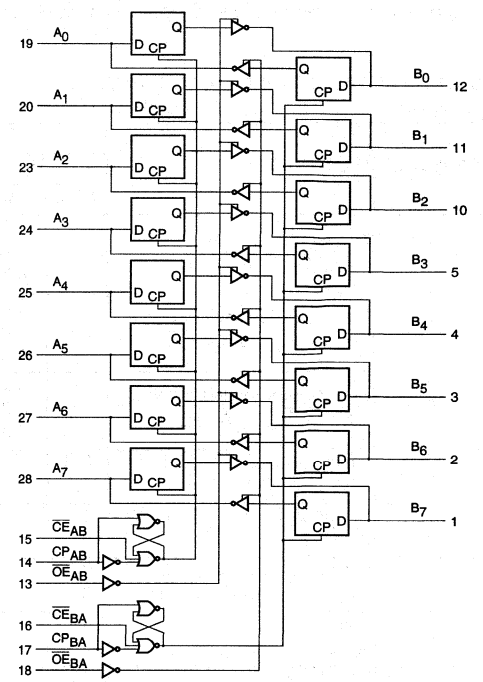


Fig.4 Functional diagram.

DC CHARACTERISTICS FOR 74HL33953

For the DC characteristics see chapter "HLL family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74HL33953

GND = 0 V; $t_r = t_f$ = 2.0 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)				UNIT	TEST CONDITIONS	
		+25		−40 to +85			V_{CC} (V)	WAVEFORMS
		MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay CP_{BA}, CP_{AB} to $\overline{A}_n$, $\overline{B}_n$	–	24	–	30	ns	1.2	Fig. 5
		–	7.8	–	9.8		2.0	
		–	4.7	–	5.9		3.0	
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_{BA}$, $\overline{OE}_{AB}$ to $\overline{A}_n$, $\overline{B}_n$	–	21	–	27	ns	1.2	Fig. 7
		–	7.0	–	8.8		2.0	
		–	4.2	–	5.3		3.0	
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_{BA}$, $\overline{OE}_{AB}$ to $\overline{A}_n$, $\overline{B}_n$	–	13	–	16	ns	1.2	Fig. 7
		–	5.2	–	6.1		2.0	
		–	3.6	–	4.2		3.0	
t_W	CP_{AB}, CP_{BA} pulse width, HIGH or LOW	2.0	–	2.3	–	ns	2.0	Fig. 5
		1.3	–	1.6	–		3.0	
t_{su}	set-up time, HIGH or LOW $\overline{A}_n$, $\overline{B}_n$ to CP_{AB}, CP_{BA}	1.1	–	1.3	–	ns	2.0	Fig. 6
		0.7	–	0.9	–		3.0	
t_{su}	set-up time, HIGH or LOW $\overline{CE}_{AB}$, $\overline{CE}_{BA}$ to CP_{AB}, CP_{BA}	0.3	–	0.3	–	ns	2.0	Fig. 6
		0.2	–	0.3	–		3.0	
t_h	hold time $\overline{A}_n$, $\overline{B}_n$ to CP_{AB}, CP_{BA}	−0.3	–	−0.3	–	ns	2.0	Fig. 6
		−0.3	–	−0.3	–		3.0	
t_h	hold time $\overline{CE}_{AB}$, $\overline{CE}_{BA}$ to CP_{AB}, CP_{BA}	0.0	–	0.0	–	ns	2.0	Fig. 6
		0.0	–	0.0	–		3.0	
f_{max}	maximum clock pulse frequency	166	–	140	–	MHz	2.0	Fig. 5
		250	–	200	–		3.0	

AC WAVEFORMS

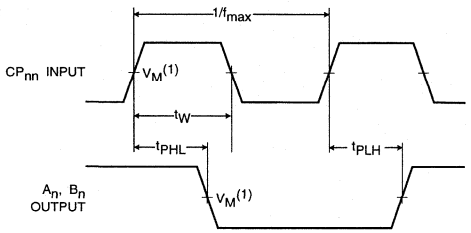


Fig. 5 Waveforms showing the clock input (CP_{BA}, CP_{AB}) to output ($\overline{B}_n$, $\overline{A}_n$) propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency.

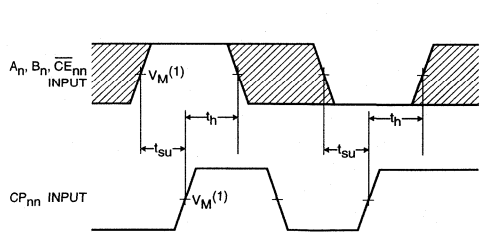


Fig.6 Waveforms showing the set-up and hold times for the A_n, B_n and $\overline{CE}_{nn}$ inputs.

Note to Fig.6

The shaded areas indicate when the input is permitted to change for predictable output performance.

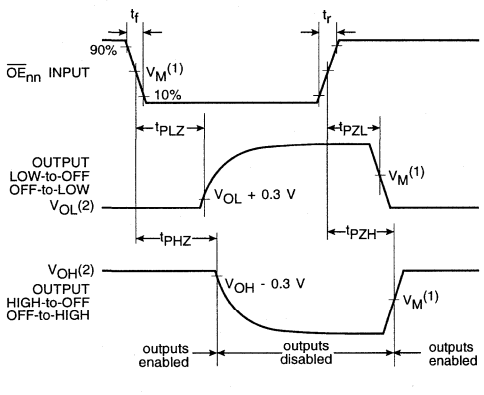


Fig.7 Waveforms showing the 3-state enable and disable times.

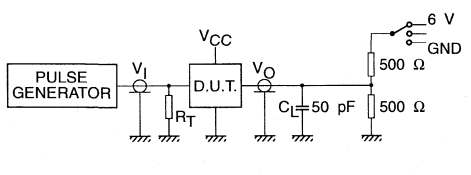


Fig.8 Test conditions: Load circuitry for enable / disable times, switch set to 6 V for t_{PLZ}/t_{PZL}, switch set to GND for t_{PHZ}/t_{PZH} otherwise do not connect.

Notes: (1) V_M = 0.6 V at V_{CC}= 1.2 V.
V_M = 1.0 V at V_{CC}= 2.0 V.
V_M = 1.5 V at V_{CC}= 3.0 V.

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-state output load.

DEVICE DATA

ALVC

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no.8-1A**
- **CMOS low power consumption**
- **Multibyte™ flow-through standard pin-out architecture**
- **Low inductance multiple power and ground pins for minimum noise and ground bounce**
- **Direct interface with TTL levels**
- **All data inputs have bushold**
- **Output drive capability 50 Ω transmission lines @ 85 °C**

DESCRIPTION

The 74ALVC16240 is a high-performance, low-power, low-voltage, Si-gate CMOS device superior to most advanced CMOS compatible TTL families.

The 74ALVC16240 is a 16-bit inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state. The "16240" is identical to the "16244" but has inverting outputs.

FUNCTION TABLE

INPUTS		OUTPUT
$n\overline{OE}$	nA_n	nY_n
L	L	H
L	H	L
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	C_L = 50 pF; V_{CC} = 3.3 V	2.1	ns
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	30	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC16240DL	48	SSOP48	plastic	SSOP48/SOT370
74ALVC16240DGG	48	TSSOP48	plastic	TSSOP48/SOT362

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	'1' output enable input (active LOW)
2, 3, 5, 6	$1Y_0$ to $1Y_3$	'1Y' data outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	ground (0 V)
7, 18, 31, 42	V_{CC}	positive supply voltage
8, 9, 11, 12	$2Y_0$ to $2Y_3$	'2Y' data outputs
13, 14, 16, 17	$3Y_0$ to $3Y_3$	'3Y' data outputs
19, 20, 22, 23	$4Y_0$ to $4Y_3$	'4Y' data outputs
24	$4\overline{OE}$	'4' output enable input (active LOW)
25	$3\overline{OE}$	'3' output enable input (active LOW)
30, 29, 27, 26	$4A_0$ to $4A_3$	'4A' data inputs
36, 35, 33, 32	$3A_0$ to $3A_3$	'3A' data inputs
41, 40, 38, 37	$2A_0$ to $2A_3$	'2A' data inputs
47, 46, 44, 43	$1A_0$ to $1A_3$	'1A' data inputs
48	$2\overline{OE}$	'2' output enable input (active LOW)

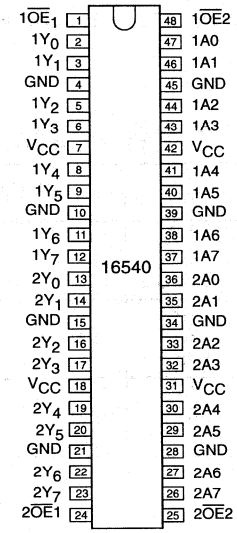


Fig.1 Pin configuration.

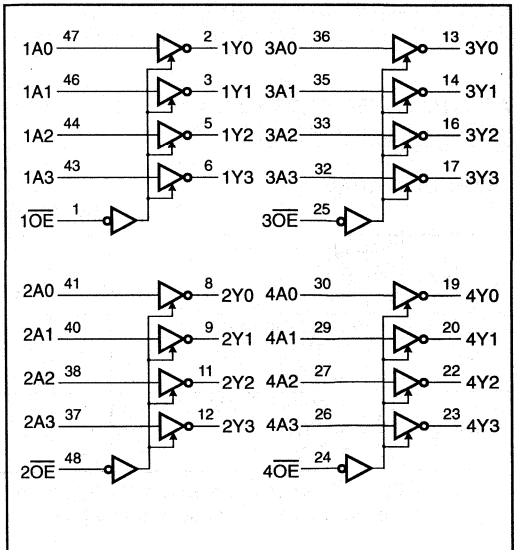


Fig.2 Logic symbol.

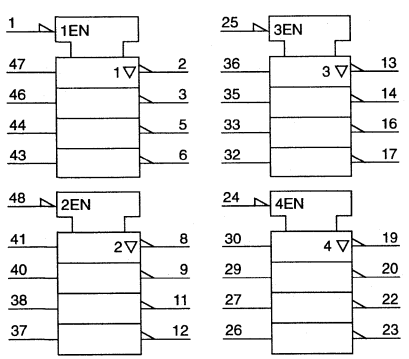


Fig.3 IEC logic symbol.

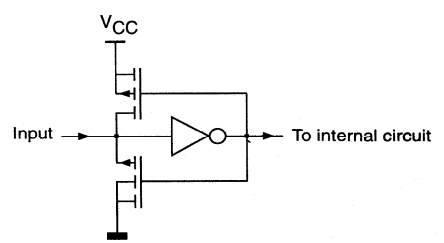


Fig.4 Bushold circuit.

DC CHARACTERISTICS FOR 74ALVC16240

For the DC characteristics see chapter "ALVC16 family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74ALVC16240

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C) −40 to +85			UNIT	TEST CONDITIONS	
		MIN.	TYP.	MAX.		V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay	–	–	16.0	ns	1.2	Fig. 5
	$1A_n$ to $1Y_n$;	–	–	4.5		2.7	
	$2A_n$ to $2Y_n$	–	2.1*	3.9		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time	–	–	–	ns	1.2	Fig. 6
	$1\overline{OE}$ to $1Y_n$;	–	–	5.5		2.7	
	$2\overline{OE}$ to $2Y_n$	–	–	4.7		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time	–	–	–	ns	1.2	Fig. 6
	$1\overline{OE}$ to $1Y_n$;	–	–	5.5		2.7	
	$2\overline{OE}$ to $2Y_n$	–	–	5.0		3.0 to 3.6	

Notes: All typical values are measured at T_{amb} = 25 °C.
* Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

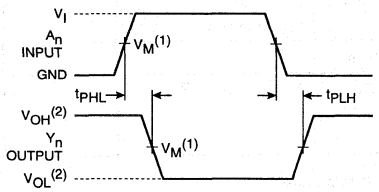


Fig.5 Waveforms showing the input (A_n) to output (Y_n) propagation delay times.

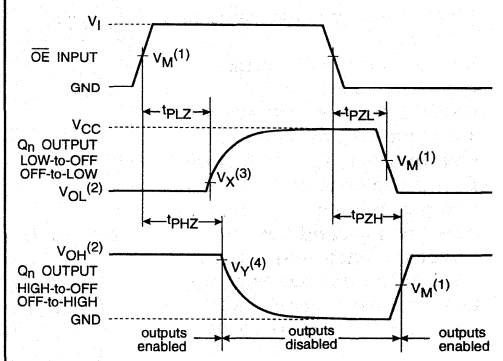
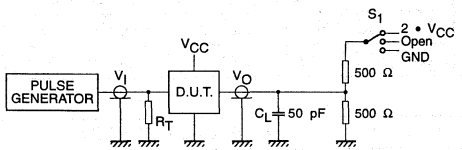


Fig.6 Waveforms showing the 3-state enable and disable times.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.7 Load circuitry for switching times.

Notes:

(1) V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
$V_M = 0.5 \cdot V_{CC}$ at V_{CC} < 2.7 V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

(3) $V_X = V_{OL}$ + 0.3 V at $V_{CC} \geq$ 2.7 V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at V_{CC} < 2.7 V

(4) $V_Y = V_{OH}$ – 0.3 V at $V_{CC} \geq$ 2.7 V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at V_{CC} < 2.7 V

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no.8-1A**
- **CMOS low power consumption**
- **Multibyte™ flow-through standard pin-out architecture**
- **Low inductance multiple power and ground pins for minimum noise and ground bounce**
- **Direct interface with TTL levels**
- **All data inputs have bushold**
- **Output drive capability 50 Ω transmission lines @ 85 °C**

DESCRIPTION

The 74ALVC16241 is a high-performance, low-power, low-voltage, Si-gate CMOS device superior to most advanced CMOS compatible TTL families.

The 74ALVC16241 is a 16-bit buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs nOE and nOE. Smitt-trigger action at all inputs makes the circuit highly tolerant for slower input rise and fall times

FUNCTION TABLE

INPUTS		OUTPUT
$n\overline{OE}$	$1A_n$, $4A_n$	$1Y_n$, $4Y_n$
L	H	H
L	L	L
H	X	Z

INPUTS		OUTPUT
nOE	$2A_n$, $3A_n$	$2Y_n$, $3Y_n$
H	H	H
H	L	L
L	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA_n to nY_n	C_L = 50 pF V_{CC} = 3.3 V	2.1	ns
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	30	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC16241DL	48	SSOP48	plastic	SSOP48/SOT370
74ALVC16241DGG	48	TSSOP48	plastic	TSSOP48/SOT362

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	'1' output enable input (active LOW)
2, 3, 5, 6	$1Y_0$ to $1Y_3$	'1Y' data outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	ground (0 V)
7, 18, 31, 42	V_{CC}	positive supply voltage
8, 9, 11, 12	$2Y_0$ to $2Y_3$	'2Y' data outputs
13, 14, 16, 17	$3Y_0$ to $3Y_3$	'3Y' data outputs
19, 20, 22, 23	$4Y_0$ to $4Y_3$	'4Y' data outputs
24	$4\overline{OE}$	'4' output enable input (active LOW)
25	3OE	'3' output enable input (active LOW)
30, 29, 27, 26	$4A_0$ to $4A_3$	'4A' data inputs
36, 35, 33, 32	$3A_0$ to $3A_3$	'3A' data inputs
41, 40, 38, 37	$2A_0$ to $2A_3$	'2A' data inputs
47, 46, 44, 43	$1A_0$ to $1A_3$	'1A' data inputs
48	2OE	'2' output enable input (active LOW)

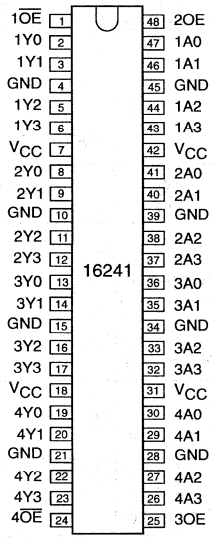


Fig.1 Pin configuration.

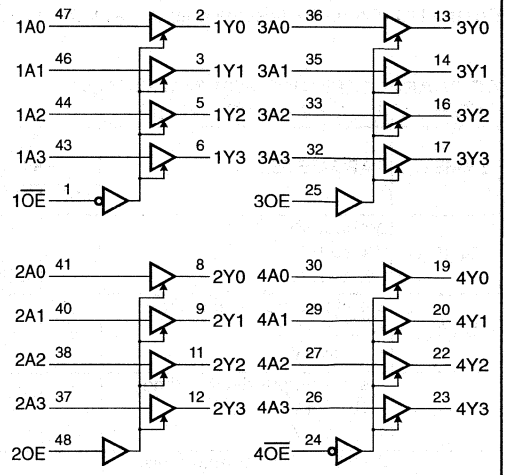


Fig.2 Logic symbol.

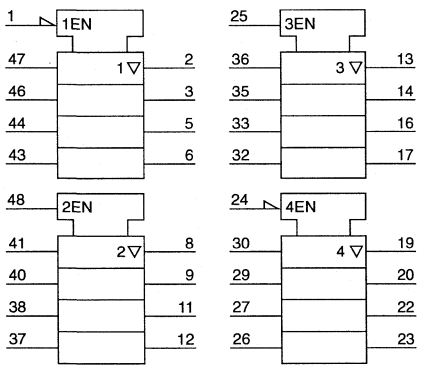


Fig.3 IEC logic symbol.

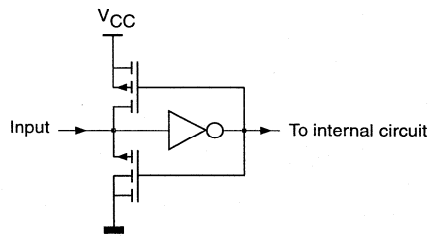


Fig.4 Bushold circuit.

DC CHARACTERISTICS FOR 74ALVC16241

For the DC characteristics see chapter "ALVC16 family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74ALVC16241

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C) −40 to +85			UNIT	TEST CONDITIONS	
		MIN.	TYP.	MAX.		V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay nA_n to nY_n; nA_n to nY_n	– – –	– – 2.3*	– 4.5 3.6	ns	1.2 2.7 3.0 to 3.6	Fig. 5
t_{PZH}/t_{PZL}	3-state output enable time $1\overline{OE}$ to $1Y_n$; $4\overline{OE}$ to $4Y_n$	– – –	– – –	– 5.5 4.7	ns	1.2 2.7 3.0 to 3.6	Fig. 6
t_{PHZ}/t_{PLZ}	3-state output disable time $1\overline{OE}$ to $1Y_n$; $4\overline{OE}$ to $4Y_n$	– – –	– – –	– 6.0 5.0	ns	1.2 2.7 3.0 to 3.6	Fig. 6, 8
t_{PZH}/t_{PZL}	3-state output enable time 2OE to $2Y_n$; 3OE to $3Y_n$	– – –	– – –	– 5.5 4.7	ns	1.2 2.7 3.0 to 3.6	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time 2OE to $2Y_n$; 3OE to $3Y_n$	– – –	– – –	– 6.0 5.0	ns	1.2 2.7 3.0 to 3.6	Fig. 7

Notes: All typical values are measured at T_{amb} = 25 °C.
* Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

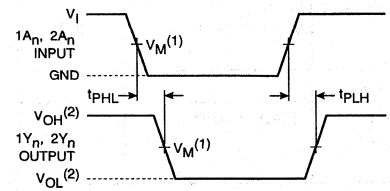


Fig.5 Waveforms showing the input (nA_n) to output (nY_n) propagation delay times.

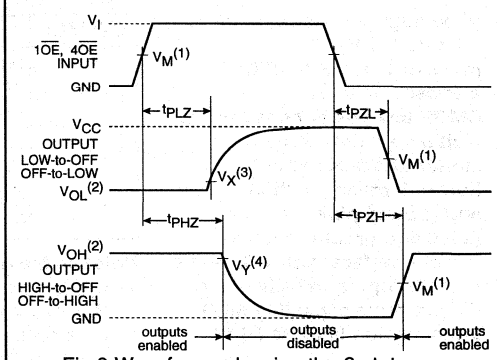


Fig.6 Waveforms showing the 3-state enable and disable times for the input ($1\overline{OE}$, $4\overline{OE}$).

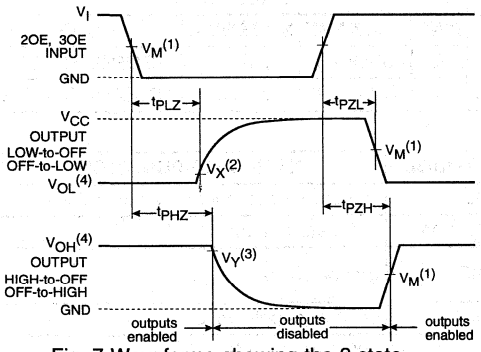
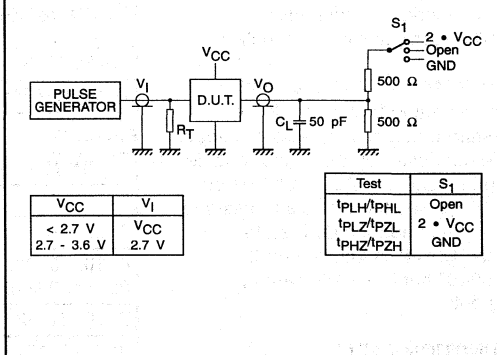


Fig. 7 Waveforms showing the 3-state enable and disable times for the input (2OE, 3OE).



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \cdot V_{CC}$
t_{PHZ}/t_{PZH}	GND

Fig.8 Load circuitry for switching times.

Notes:

(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no.8-1A**
- **CMOS low power consumption**
- **Multibyte™ flow-through standard pin-out architecture**
- **Low inductance multiple power and ground pins for minimum noise and ground bounce**
- **Direct interface with TTL levels**
- **All data inputs have bushold**
- **Output drive capability 50 Ω transmission lines @ 85 °C**

DESCRIPTION

The 74ALVC16244 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74ALVC16244 is a 16-bit non-inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state. The "16244" is identical to the "16240" but has non-inverting outputs.

FUNCTION TABLE

INPUTS		OUTPUT
$n\overline{OE}$	nA_n	nY_n
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	C_L = 15 pF; V_{CC} = 3.3 V	2.1	ns
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	30	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC16244DL	48	SSOP48	plastic	SSOP48/SOT370
74ALVC16244DGG	48	TSSOP48	plastic	TSSOP48/SOT362

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	'1' output enable input (active LOW)
2, 3, 5, 6	$1Y_0$ to $1Y_3$	'1Y' data outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	ground (0 V)
7, 18, 31, 42	V_{CC}	positive supply voltage
8, 9, 11, 12	$2Y_0$ to $2Y_3$	'2Y' data outputs
13, 14, 16, 17	$3Y_0$ to $3Y_3$	'3Y' data outputs
19, 20, 22, 23	$4Y_0$ to $4Y_3$	'4Y' data outputs
24	$4\overline{OE}$	'4' output enable input (active LOW)
25	$3\overline{OE}$	'3' output enable input (active LOW)
30, 29, 27, 26	$4A_0$ to $4A_3$	'4A' data inputs
36, 35, 33, 32	$3A_0$ to $3A_3$	'3A' data inputs
41, 40, 38, 37	$2A_0$ to $2A_3$	'2A' data inputs
47, 46, 44, 43	$1A_0$ to $1A_3$	'1A' data inputs
48	$2\overline{OE}$	'2' output enable input (active LOW)

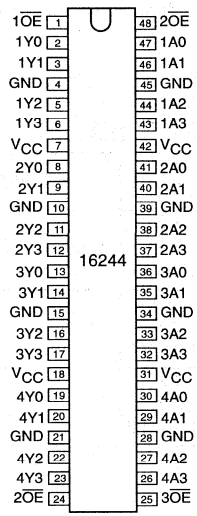


Fig.1 Pin configuration.

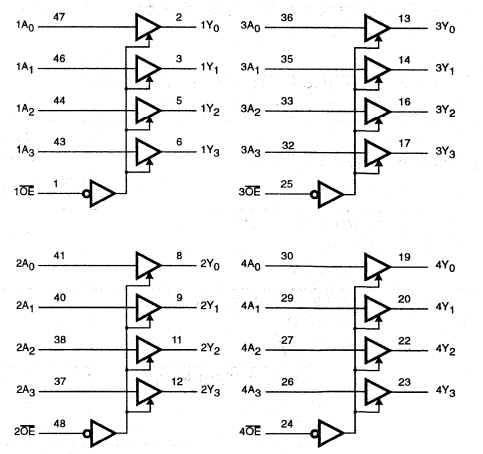


Fig.2 Logic symbol.

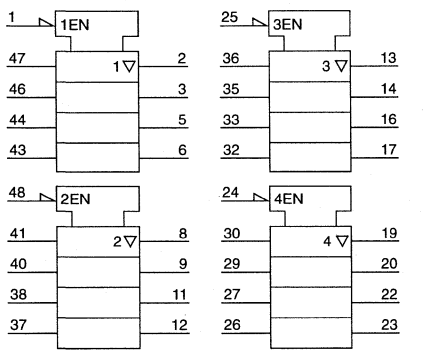


Fig.3 IEC logic symbol.

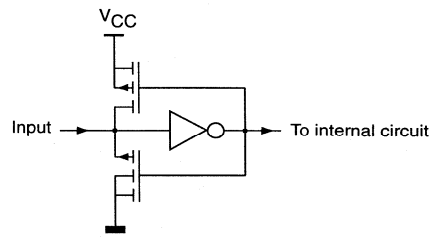


Fig.4 Bushold circuit.

DC CHARACTERISTICS FOR 74ALVC244

For the DC characteristics see chapter "ALVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74ALVC244

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C) −40 to +85			UNIT	TEST CONDITIONS	
		MIN.	TYP.	MAX.		V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	– – –	– – 2.3*	– 4.0 3.6	ns	1.2 2.7 3.0 to 3.6	Fig. 5
t_{PZH}/t_{PZL}	3-state output enable time $1\overline{OE}$ to $1Y_n$; $2\overline{OE}$ to $2Y_n$	– – –	– – –	– 5.5 4.7	ns	1.2 2.7 3.0 to 3.6	Figs 6
t_{PHZ}/t_{PLZ}	3-state output disable time $1\overline{OE}$ to $1Y_n$; $2\overline{OE}$ to $2Y_n$	– – –	– – –	– 6.0 5.0	ns	1.2 2.7 3.0 to 3.6	Figs 6

Notes: All typical values are measured at T_{amb} = 25 °C.

* Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

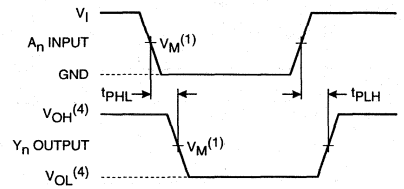


Fig.5 Waveforms showing the input (A_n) to output (Y_n) propagation delay times.

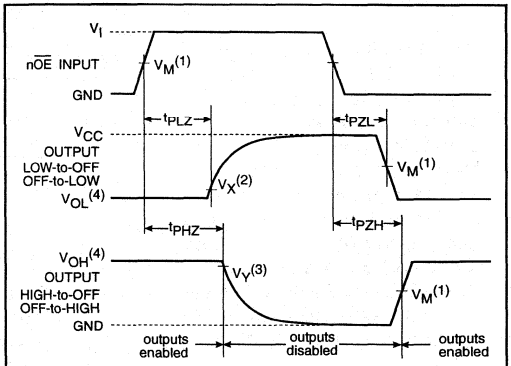
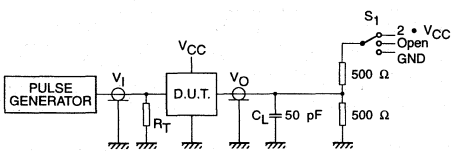


Fig.6 Waveforms showing the 3-state enable and disable times.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.7 Load circuitry for switching times.

Notes:

(1) $V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
$V_M = 1.5$ V at $V_{CC} \geq 2.7$ V

(2) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(3) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no.8-1A**
- **CMOS low power consumption**
- **Multibyte™ flow-through standard pin-out architecture**
- **Low inductance multiple power and ground pins for minimum noise and ground bounce**
- **Direct interface with TTL levels**
- **All data inputs have bushold**
- **Integrated 30Ω termination resistor**

DESCRIPTION

The 74ALVC16244-1 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74ALVC16244-1 is a 16-bit non-inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state. The ALVC16244-1 is designed with 30 Ω series resistors in both HIGH and LOW output states.

FUNCTION TABLE

INPUTS		OUTPUT
$n\overline{OE}$	nA_n	nY_n
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	C_L = 15 pF; V_{CC} = 3.3 V	2.1	ns
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	30	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC16244-1DL	48	SSOP48	plastic	SSOP48/SOT370
74ALVC16244-1DGG	48	TSSOP48	plastic	TSSOP48/SOT362

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	'1' output enable input (active LOW)
2, 3, 5, 6	$1Y_0$ to $1Y_3$	'1Y' data outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	ground (0 V)
7, 18, 31, 42	V_{CC}	positive supply voltage
8, 9, 11, 12	$2Y_0$ to $2Y_3$	'2Y' data outputs
13, 14, 16, 17	$3Y_0$ to $3Y_3$	'3Y' data outputs
19, 20, 22, 23	$4Y_0$ to $4Y_3$	'4Y' data outputs
24	$4\overline{OE}$	'4' output enable input (active LOW)
25	$3\overline{OE}$	'3' output enable input (active LOW)
30, 29, 27, 26	$4A_0$ to $4A_3$	'4A' data inputs
36, 35, 33, 32	$3A_0$ to $3A_3$	'3A' data inputs
41, 40, 38, 37	$2A_0$ to $2A_3$	'2A' data inputs
47, 46, 44, 43	$1A_0$ to $1A_3$	'1A' data inputs
48	$2\overline{OE}$	'2' output enable input (active LOW)

16-bit 30 Ω termintaed buffer/line driver; 3-state

74ALVC16244-1

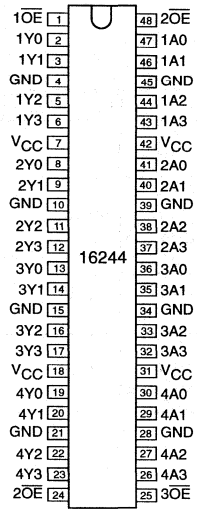


Fig.1 Pin configuration.

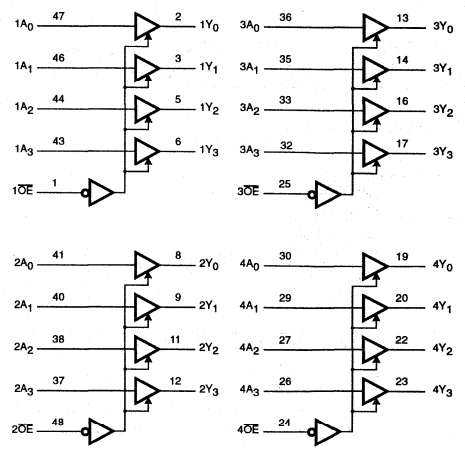


Fig.2 Logic symbol.

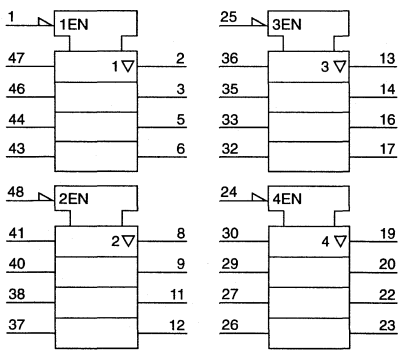


Fig.3 IEC logic symbol.

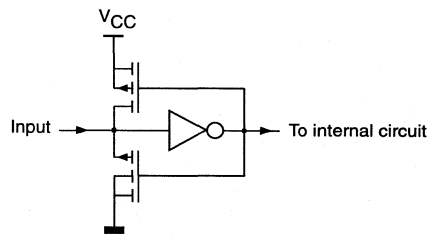


Fig.4 Bushold circuit.

DC CHARACTERISTICS FOR 74ALVC244-1

For the DC characteristics see chapter "ALVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74ALVC244-1

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C) −40 to +85			UNIT	TEST CONDITIONS	
		MIN.	TYP.	MAX.		V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	– – –	16 – 2.3*	– 4.0 3.6	ns	1.2 2.7 3.0 to 3.6	Fig. 5
t_{PZH}/t_{PZL}	3-state output enable time $1\overline{OE}$ to $1Y_n$; $2\overline{OE}$ to $2Y_n$	– – –	– – –	– 5.0 4.7	ns	1.2 2.7 3.0 to 3.6	Fig. 6
t_{PHZ}/t_{PLZ}	3-state output disable time $1\overline{OE}$ to $1Y_n$; $2\overline{OE}$ to $2Y_n$	– – –	– – –	– 5.2 5.0	ns	1.2 2.7 3.0 to 3.6	Fig. 6

Notes: All typical values are measured at T_{amb} = 25 °C.
* Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

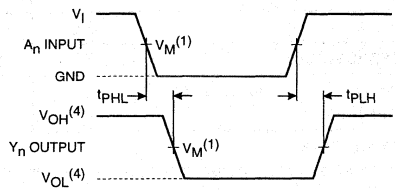


Fig.4 Waveforms showing the input (A_n) to output (Y_n) propagation delay times.

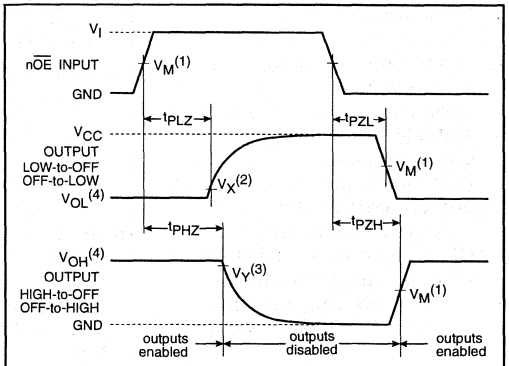
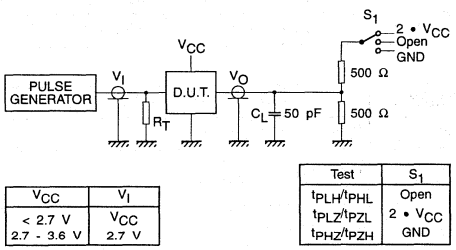


Fig.5 Waveforms showing the 3-state enable and disable times.



V_{CC}	V_I
< 2.7 V 2.7 - 3.6 V	V_{CC} 2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.6 Load circuitry for switching times.

Notes:

(1) $V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
$V_M = 1.5$ V at $V_{CC} \geq 2.7$ V

(2) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(3) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no.8-1A**
- **CMOS low power consumption**
- **Multibyte™ flow-through standard pin-out architecture**
- **Low inductance multiple power and ground pins for minimum noise and ground bounce**
- **Direct interface with TTL levels**
- **All data inputs have bushold**
- **Output drive capability 50 Ω transmission lines @ 85 °C**

DESCRIPTION

The ALVC16245 is a high-performance, low-power, low-voltage, Si-gate CMOS device superior to most advanced CMOS compatible TTL families.

The ALVC16245 is a 16-bit transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The '16245' features two output enable ($n\overline{OE}$) inputs for easy cascading and two send/receive (nDIR) inputs for direction control. $n\overline{OE}$ controls the outputs so that the buses are effectively isolated.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUT	
$n\overline{OE}$	nDIR	nA_n	nB_n
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n	C_L = 50 pF V_{CC} = 3.3 V	2.2	ns
C_I	input capacitance		3.0	pF
$C_{I/O}$	input/output capacitance		10	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	30	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC16245DL	48	SSOP48	plastic	SSOP48/SOT370
74ALVC16245DGG	48	TSSOP48	plastic	TSSOP48/SOT362

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	1DIR	'1' direction control
2, 3, 5, 6, 8, 9, 11, 12	$1B_0$ to $1B_7$	'1B' data inputs/outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	ground (0 V)
7, 18, 31, 42	V_{CC}	positive supply voltage
13, 14, 16, 17, 19, 20, 22, 23	$2B_0$ to $2B_7$	'2B' data inputs/outputs
24	2DIR	'2' direction control
25	$2\overline{OE}$	'2' output enable input (active LOW)
36, 35, 33, 32, 30, 29, 27, 26	$2A_0$ to $2A_7$	'2A' data inputs/outputs
47, 46, 44, 43, 41, 40, 38, 37	$1A_0$ to $1A_7$	'1A' data inputs/outputs
48	$1\overline{OE}$	'1' output enable input (active LOW)

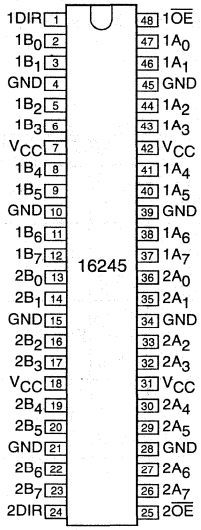


Fig.1 Pin configuration.

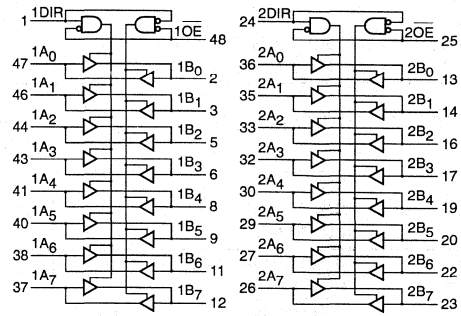


Fig.2 Logic symbol.

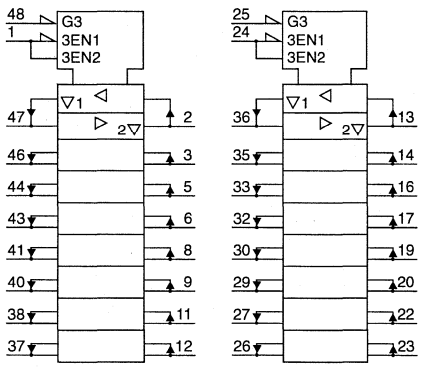


Fig.3 IEC logic symbol.

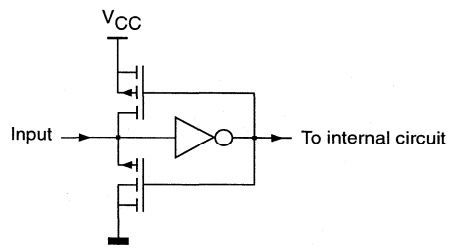


Fig.4 Bushold circuit.

DC CHARACTERISTICS FOR ALVC16245

For the DC characteristics see chapter "ALVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR ALVC16245

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C) −40 to +85			UNIT	TEST CONDITIONS	
		MIN.	TYP.	MAX.		V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay nA_n to nB_n; nB_n to nA_n	– – –	– – 2.3*	– 4.5 3.6	ns	1.2 2.7 3.0 to 3.6	Fig.5
t_{PZH}/t_{PZL}	3-state output enable time $n\overline{OE}$ to nA_n; $n\overline{OE}$ to nB_n	– – –	– – –	– 5.5 4.7	ns	1.2 2.7 3.0 to 3.6	Fig. 6
t_{PHZ}/t_{PLZ}	3-state output disable time $n\overline{OE}$ to nA_n; $n\overline{OE}$ to nB_n	– – –	– – –	– 5.5 5.0	ns	1.2 2.7 3.0 to 3.6	Fig. 6

Notes: All typical values are measured at T_{amb} = 25 °C.
* Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

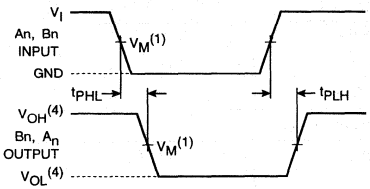


Fig. 5 Waveforms showing the input (nA_n, nB_n) to output (nB_n, nA_n) propagation delay times.

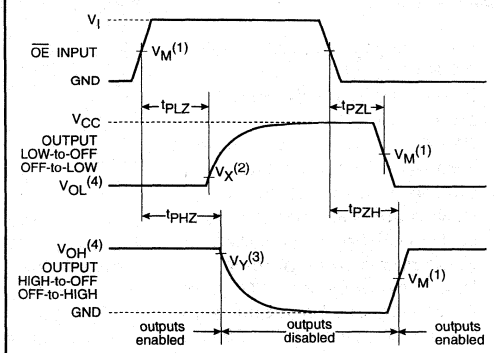
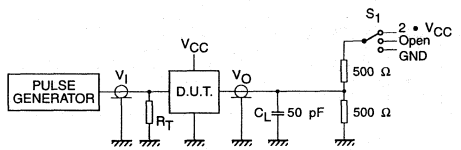


Fig.6 Waveforms showing the 3-state enable and disable times.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig. 7 Load circuitry for switching times.

Notes:

(1) $V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
$V_M = 1.5$ V at $V_{CC} \geq 2.7$ V

(2) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(3) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

16-bit 30 Ω terminated bus transceiver with direction pin; 3-state

74ALVC16245-1

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no.8-1A**
- **CMOS low power consumption**
- **Multibyte™ flow-through standard pin-out architecture**
- **Low inductance multiple power and ground pins for minimum noise and ground bounce**
- **Direct interface with TTL levels**
- **All data inputs have bushold**
- **Output drive capability 50 Ω transmission lines @ 85 °C**

DESCRIPTION

The ALVC16245-1 is a high-performance, low-power, low-voltage, Si-gate CMOS device superior to most advanced CMOS compatible TTL families.

The ALVC16245-1 is a 16-bit transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The '16245-1' features two output enable ($n\overline{OE}$) inputs for easy cascading and two send/receive (nDIR) inputs for direction control. $n\overline{OE}$ controls the outputs so that the buses are effectively isolated.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUT	
$n\overline{OE}$	nDIR	nA_n	nB_n
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n	C_L = 50 pF V_{CC} = 3.3 V	2.2	ns
C_I	input capacitance		3.0	pF
$C_{I/O}$	input/output capacitance		10	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	30	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC16245-1DL	48	SSOP48	plastic	SSOP48/SOT370
74ALVC16245-1DGG	48	TSSOP48	plastic	TSSOP48/SOT362

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	1DIR	'1' direction control
2, 3, 5, 6, 8, 9, 11, 12	$1B_0$ to $1B_7$	'1B' data inputs/outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	ground (0 V)
7, 18, 31, 42	V_{CC}	positive supply voltage
13, 14, 16, 17, 19, 20, 22, 23	$2B_0$ to $2B_7$	'2B' data inputs/outputs
24	2DIR	'2' direction control
25	$2\overline{OE}$	'2' output enable input (active LOW)
36, 35, 33, 32, 30, 29, 27, 26	$2A_0$ to $2A_7$	'2A' data inputs/outputs
47, 46, 44, 43, 41, 40, 38, 37	$1A_0$ to $1A_7$	'1A' data inputs/outputs
48	$1\overline{OE}$	'1' output enable input (active LOW)

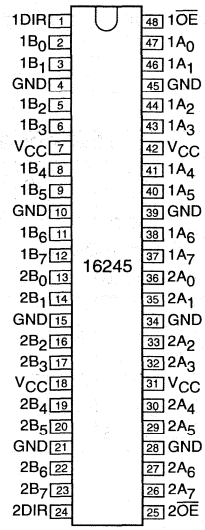


Fig.1 Pin configuration.

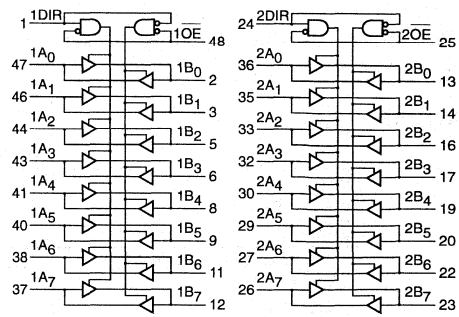


Fig.2 Logic symbol.

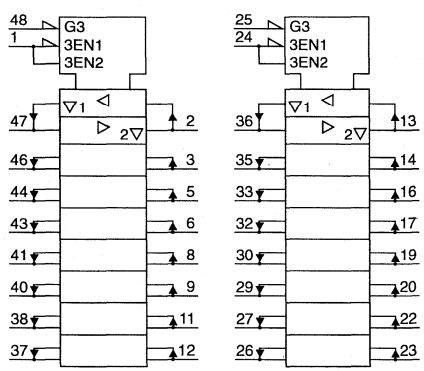


Fig.3 IEC logic symbol.

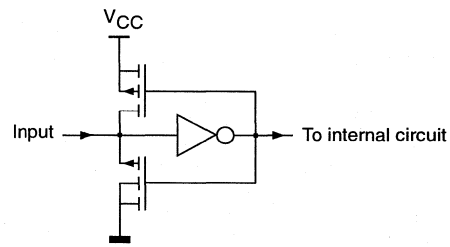


Fig.4 Bushold circuit.

DC CHARACTERISTICS FOR ALVC16245-1

For the DC characteristics see chapter "ALVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR ALVC16245-1

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C) −40 to +85			UNIT	TEST CONDITIONS	
		MIN.	TYP.	MAX.		V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay nA_n to nB_n; nB_n to nA_n	– – –	16.0 – 2.3*	– 4.0 3.6	ns	1.2 2.7 3.0 to 3.6	Fig.5
t_{PZH}/t_{PZL}	3-state output enable time $n\overline{OE}$ to nA_n; $n\overline{OE}$ to nB_n	– – –	– – –	– 5.0 4.7	ns	1.2 2.7 3.0 to 3.6	Fig. 6
t_{PHZ}/t_{PLZ}	3-state output disable time $n\overline{OE}$ to nA_n; $n\overline{OE}$ to nB_n	– – –	– – –	– 5.2 5.0	ns	1.2 2.7 3.0 to 3.6	Fig. 6

Noths: All typical values are measured at T_{amb} = 25 °C.
* Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

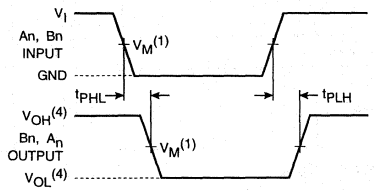


Fig. 5 Waveforms showing the input (nA_n, nB_n) to output (nB_n, nA_n) propagation delay times.

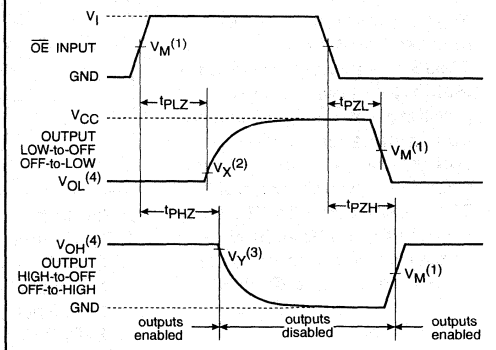
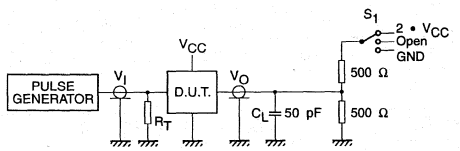


Fig.6 Waveforms showing the 3-state enable and disable times.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig. 7 Load circuitry for switching times.

Notes:

(1) $V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
$V_M = 1.5$ V at $V_{CC} \geq 2.7$ V

(2) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(3) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

16-bit D-type transparent latch; 3-state — 74ALVC16373

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no.8-1A**
- **CMOS low power consumption**
- **Multibyte™ flow-through standard pin-out architecture**
- **Low inductance multiple power and ground pins for minimum noise and ground bounce**
- **Direct interface with TTL levels**
- **All data inputs have bushold**
- **Output drive capability 50 Ω transmission lines @ 85 °C**

DESCRIPTION

The 74ALVC16373 is a 16-bit D-type transparent latch featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. One latch enable (LE) input and one output enable ($\overline{OE}$) are provided for each octal.

The "16373" consists of 2 sections of eight D-type transparent latches with 3-state true outputs. When LE is HIGH, data at the D_n inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the eight latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n; LE to Q_n	C_L = 50 pF; V_{CC} = 3.3 V	3.0 3.0	ns
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	25	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC16373DL	48	SSOP48	plastic	SSOP48/SOT370
74ALVC16373DGG	48	TSSOP48	plastic	TSSOP48/SOT362

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	'1' output enable input (active LOW)
2, 3, 5, 6, 8, 9, 11, 12	$1Q_0$ to $1Q_7$	'1Q' data inputs/outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	ground (0 V)
7, 18, 31, 42	V_{CC}	positive supply voltage
13, 14, 16, 17, 19, 20, 22, 23	$2Q_0$ to $2Q_7$	'2Q' data inputs/outputs
24	$2\overline{OE}$	'2' output enable input (active LOW)
25	2LE	'2' latch enable
36, 35, 33, 32, 30, 29, 27, 26	$2D_0$ to $2D_7$	'2D' data inputs
47, 46, 44, 43, 41, 40, 38, 37	$1D_0$ to $1D_7$	'1D' data inputs
48	1LE	'1' latch enable

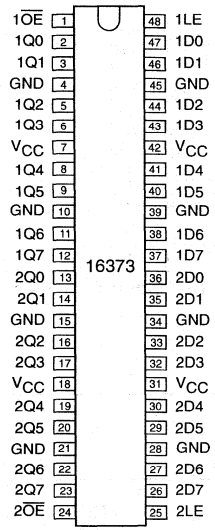


Fig.1 Pin configuration.

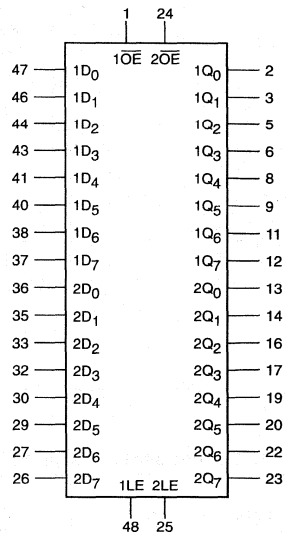


Fig.2 Logic symbol.

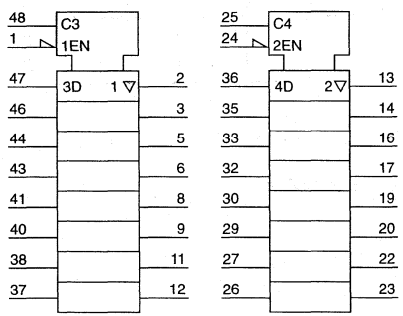


Fig.3 IEC logic symbol.

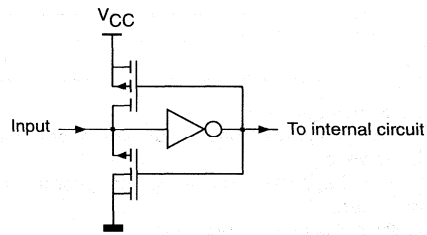


Fig.4 Bushold circuit.

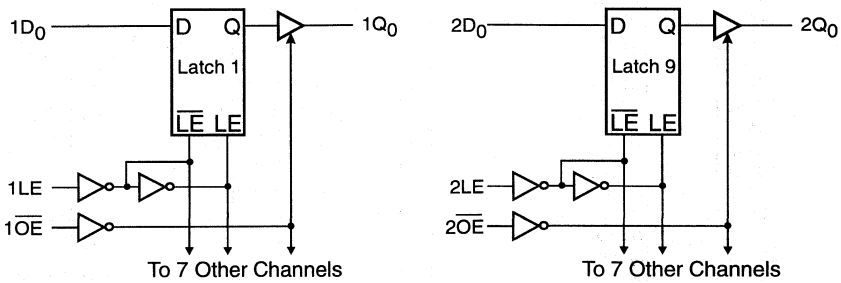


Fig. 5 Logic diagram.

FUNCTION TABLE (per section of eight bits)

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$\overline{OE}$	LE	D_n		Q_0 to Q_7
enable and read register (transparent mode)	L L	H H	L H	L H	L H
latch and read register	L L	L L	l h	L H	L H
latch register and disable outputs	H H	L L	l h	L H	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
X = don't care
Z = high impedance OFF-state

DC CHARACTERISTICS FOR 74ALVC16373

For the DC characteristics see chapter "ALVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74ALVC16373

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		−40 to +85				V_{CC} (V)	WAVEFORMS
		MIN.		MAX.			
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n	–	–	17.6	ns	1.2	Fig. 6
		–	–	4.8		2.7	
		–	3.0*	4.4		3.0 to 3.6	
t_{PHL}/t_{PLH}	propagation delay LE to Q_n	–	–	–	ns	1.2	Fig. 7
		–	–	5.3		2.7	
		–	3.0*	4.8		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n	–	–	–	ns	1.2	Fig. 8
		–	–	5.5		2.7	
		–	–	5.0		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n	–	–	–	ns	1.2	Fig. 8
		–	–	5.6		2.7	
		–	–	5.1		3.0 to 3.6	
t_w	LE pulse width HIGH	2.7	–	–	ns	2.7	Fig. 7
		2.5	–	–		3.0 to 3.6	
t_{su}	set-up time D_n to LE	2.2	–	–	ns	1.2	Fig. 9
		0.7	–	–		2.7	
		0.6	–	–		3.0 to 3.6	
t_h	hold time D_n to LE	2.2	–	–	ns	1.2	Fig. 9
		0.7	–	–		2.7	
		0.6	–	–		3.0 to 3.6	

Notes: All typical values are measured at T_{amb} = 25 °C.
* Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

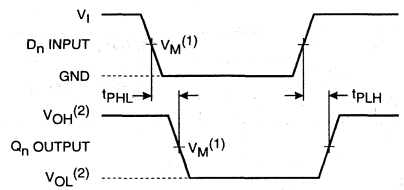


Fig.6 Waveforms showing the input (D_n) to output (Q_n) propagation delays.

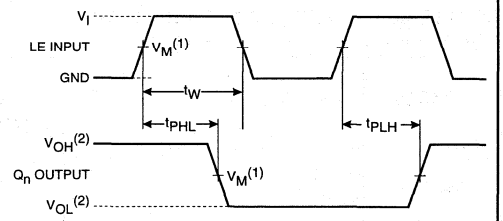


Fig.7 Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output (Q_n) propagation delays.

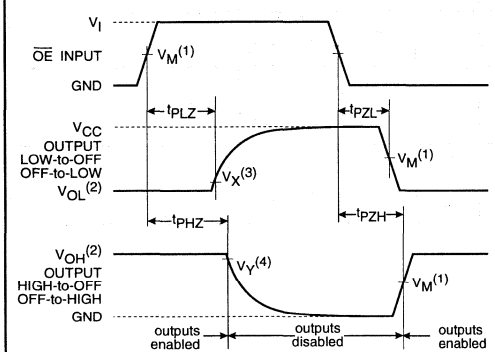


Fig.8 Waveforms showing the 3-state enable and disable times.

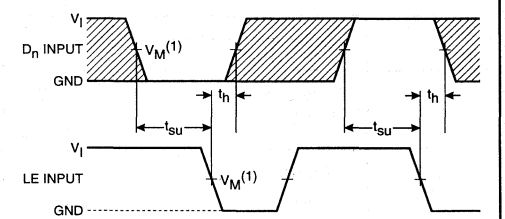
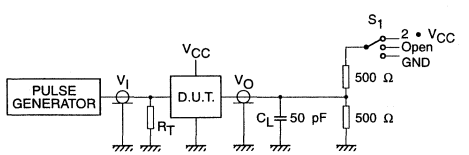


Fig.9 Waveforms showing the data set-up and hold times for the D_n input to the LE input.

Note to Fig.9:

The shaded areas indicate when the input is permitted to change for predictable output performance.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.10 Load circuitry for switching times.

Notes:

(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

16-bit edge triggered D-type flip-flop; 3-state 74ALVC16374

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no.8-1A**
- **CMOS low power consumption**
- **Multibyte™ flow-through standard pin-out architecture**
- **Low inductance multiple power and ground pins for minimum noise and ground bounce**
- **Direct interface with TTL levels**
- **All data inputs have bushold**
- **Output drive capability 50 Ω transmission lines @ 85 °C**

DESCRIPTION

The 74ALVC16374 is a 16-bit edge-triggered flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A clock (CP) input and an output enable ($\overline{OE}$) are provided for each octal.

The flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition.

When $\overline{OE}$ is LOW, the contents of the flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 50 pF; V_{CC} = 3.3 V	3.2	ns
f_{max}	maximum clock frequency		350	MHz
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	28	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC16374DL	48	SSOP48	plastic	SSOP48/SOT370
74ALVC16374DGG	48	TSSOP48	plastic	TSSOP48/SOT362

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	'1' output enable input (active LOW)
2, 3, 5, 6, 8, 9, 11, 12	$1Q_0$ to $1Q_7$	'1Q' data inputs/outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	ground (0 V)
7, 18, 31, 42	V_{CC}	positive supply voltage
13, 14, 16, 17, 19, 20, 22, 23	$2Q_0$ to $2Q_7$	'2Q' data inputs/outputs
24	$2\overline{OE}$	'1' output enable input (active LOW)
25	2CP	'2' clock input
36, 35, 33, 32, 30, 29, 27, 26	$2D_0$ to $2D_7$	'2D' data inputs
47, 46, 44, 43, 41, 40, 38, 37	$1D_0$ to $1D_7$	'1D' data inputs
48	1CP	'1' clock input

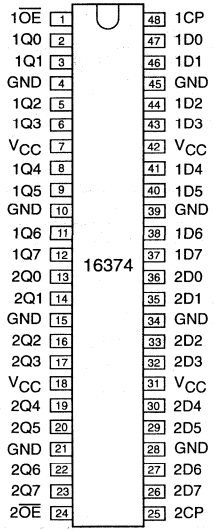


Fig.1 Pin configuration.

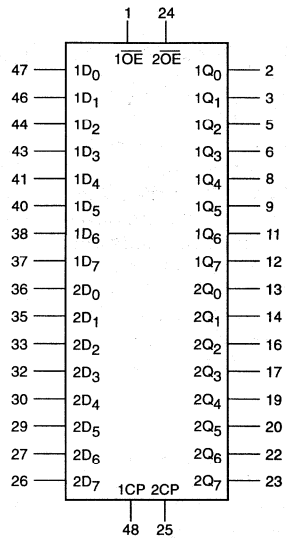


Fig.2 Logic symbol.

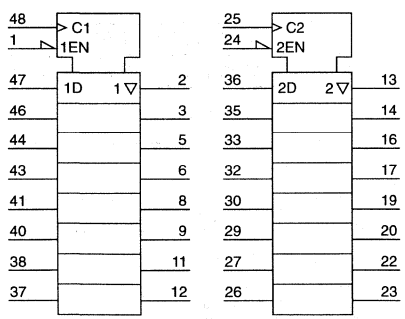


Fig.3 IEC logic symbol.

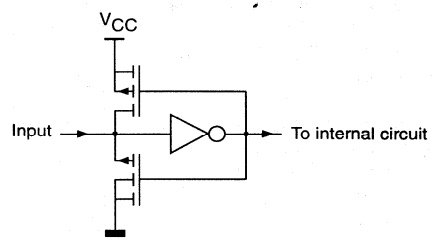


Fig.4 Bushold circuit.

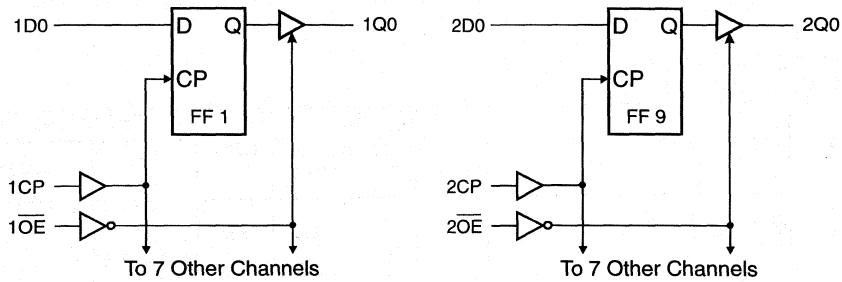


Fig.5 Logic diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	CP	D_n		Q_0 to Q_7
load and read register	L L	↑ ↑	l h	L H	L H
load register and disable outputs	H H	↑ ↑	l h	L H	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
Z = high impedance OFF-state
↑ = LOW-to-HIGH CP transition

DC CHARACTERISTICS FOR 74ALVC16374

For the DC characteristics see chapter "ALVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74ALVC16374

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		−40 to +85				V_{CC} (V)	WAVEFORMS
		MIN.		MAX.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	– – –	– – 3.0*	– 5.3 4.8	ns	1.2 2.7 3.0 to 3.6	Fig.5
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n	– – –	– – –	– 5.5 5.0	ns	1.2 2.7 3.0 to 3.6	Fig.6
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n	– – –	– – –	– 5.6 5.1	ns	1.2 2.7 3.0 to 3.6	Fig.6
t_W	CP pulse width HIGH or LOW	2.8 2.5	– –	– –	ns	2.7 3.0 to 3.6	Fig.5
t_{su}	set–up time D_n to CP	2.2 0.7 0.6	– – –	– – –	ns	1.2 2.7 3.0 to 3.6	Fig.7
t_h	hold time D_n to CP	2.2 0.7 0.6	– – –	– – –	ns	1.2 2.7 3.0 to 3.6	Fig.7
f_{max}	maximum clock pulse frequency	– 200	– –	– –	MHz	2.7 3.0 to 3.6	Fig.5

Notes: All typical values are measured at T_{amb} = 25 °C.
* Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

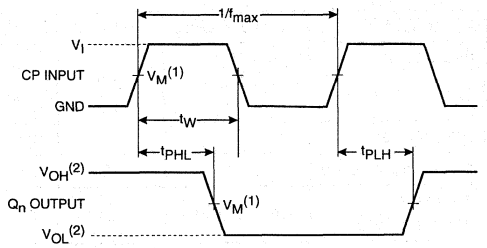


Fig.6 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width and the maximum clock pulse frequency.

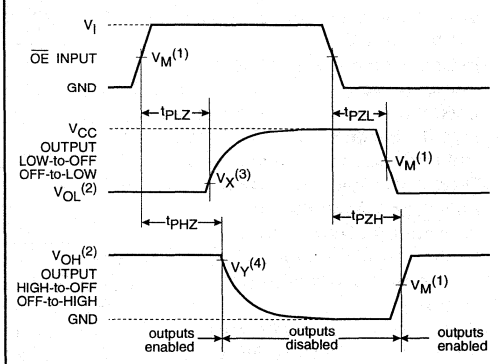


Fig.7 Waveforms showing the 3-state enable and disable times.

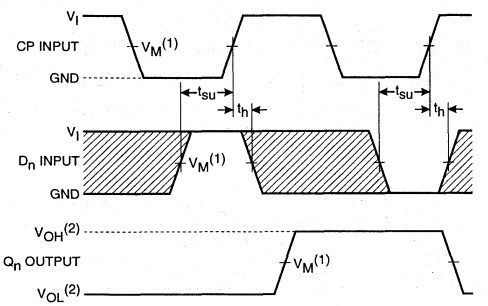
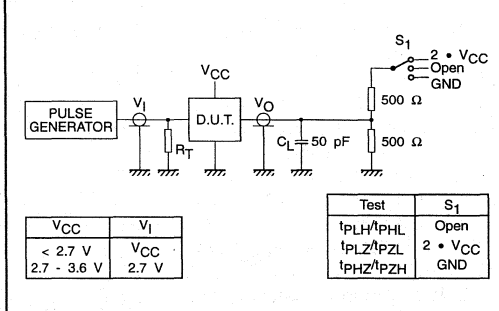


Fig.8 Waveforms showing the data set-up and hold times for the D_n input to the CP input.

Note to Fig.8:

The shaded areas indicate when the input is permitted to change for predictable output performance.



VCC	VI
< 2.7 V	VCC
2.7 - 3.6 V	2.7 V

Test	S1
tPLH/tPHL	Open
tPLZ/tPZL	2 • VCC
tPHZ/tPZH	GND

Fig.9 Load circuitry for switching times.

Notes:

(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **CMOS low power consumption**
- **Direct interface with TTL levels**
- **Univeral bus transceiver with D-type latches and D-type Flip-flops capabable of operating in transparant, latched or clocked mode.**
- **All inputs have bushold circuitry**
- **Output drive capability 50Ω transmission lines @ 85 °C**
- **3-state non-inverting outputs for bus oriented applications**

DESCRIPTION

The 74ALVC16500 is an 18-bit universal bus transceiver.
Data flow in each direction is controlled by output enable (OE_{AB}, $\overline{OE}_{BA}$), latch-enable (LE_{AB}, LE_{BA}) and clock inputs (CP_{AB}, $\overline{CP}_{BA}$).
When LE_{AB} is HIGH, the A-B dataflow is transparant. When LE_{AB} is LOW, and $\overline{CP}_{AB}$ is held at LOW or HIGH, the A data is latched; on the HIGH-to-LOW transition of $\overline{CP}_{AB}$ the A-data is stored in the latch/flip-flop. The outputs are active when OE_{AB} is HIGH. When OE_{AB} is LOW the B-outputs are in 3-state.
Similarly, the LE_{BA}, $\overline{OE}_{BA}$ and $\overline{CP}_{BA}$ control the B-to-A dataflow. Please note that both output enables are complementary: OE_{AB} is active HIGH, $\overline{OE}_{BA}$ is active LOW.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n to B_n LE_{AB} to A_n	C_L = 50 pF V_{CC} = 3.3 V	3.0 3.2	ns
C_I	input capacitance		5.0	pF
$C_{I/O}$	input/output capacitance		10	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	22	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC16500DL	56	SSOP56	plastic	SSOP56/SOT371
74ALVC16500DGG	56	TSSOP56	plastic	TSSOP56/SOT364

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}_{AB}$	output enable A-to-B
2	LE_{AB}	latch enable A-to-B
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	A_0 to A_{17}	'A' data inputs/outputs
4, 11, 18, 25, 29, 32, 39, 46, 53, 56	GND	ground (0 V)
7, 22, 35, 50	V_{CC}	positive supply voltage
27	OE_{BA}	output enable B-to-A
28	LE_{BA}	latch enable B-to-A
30	$\overline{CP}_{BA}$	clock input B-to-A, HIGH-to-LOW
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	B_0 to B_{17}	'B' data inputs/outputs
55	$\overline{CP}_{AB}$	clock input A-to-B, HIGH-to-LOW

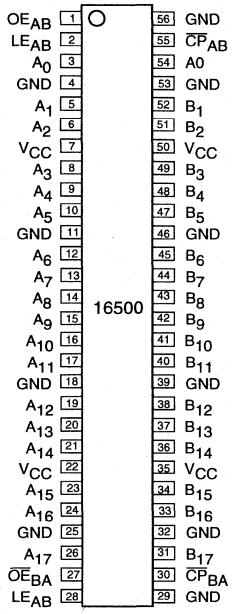


Fig.1 Pin configuration.

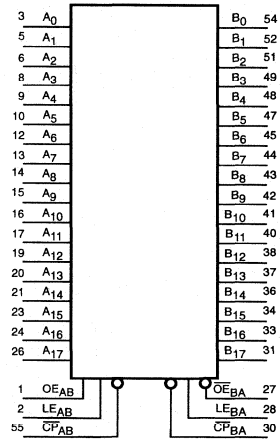


Fig.2 Logic symbol.

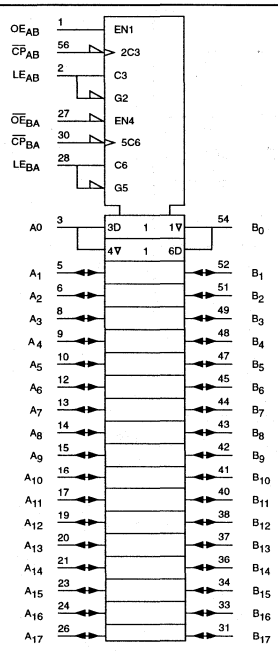


Fig.3 IEC Logic Symbol

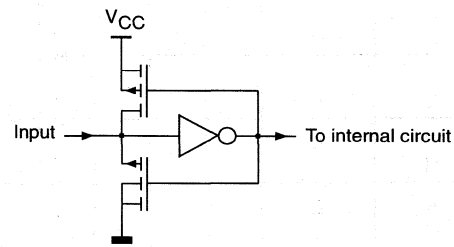


Fig.4 Bushold circuit

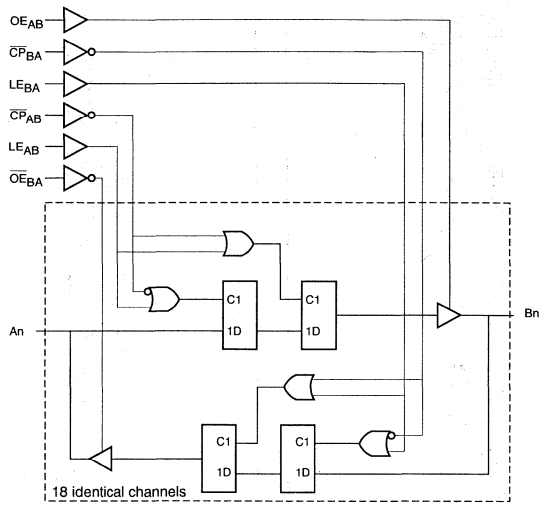


Fig.5 Logic diagram (one section)

FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
OE_{AB} [1]	LE_{XX}	$\overline{CP}_{XX}$	DATA		
L	X	X	X	Z	Disabled
H H	H H	X X	H L	H L	Transparant
L L	L L	↓ ↓	h l	Z Z	Disabled + latch
H H	L L	↓ ↓	h l	H L	Latch + display
H H	L L	H L	X X	NC NC1	Hold

XX = AB for A-to-B direction, BA for B-to-A direction
H = HIGH voltage level
L = LOW voltage level
h = High state must be present one setup time before the low-to-high transition of $\overline{CP}$
l = Low state must be present one setup time before the low-to-high transition of $\overline{CP}$
X = Don't care
↓ = HIGH-to-LOW level transition
NC = No change
NC1 = No change provided that CP was LOW before LE_{XX} went low
Z = High impedance "off" state

[1] For the B-to-A direcion $\overline{OE}_{BA}$ is the inverse of OE_{AB}

DC CHARACTERISTICS FOR 74ALVC16500

For the DC characteristics see chapter "ALVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74ALVC16500

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		−40 to +85				V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t_{PHL}/t_{PLH}	propagation delay A_n to B_n, B_n to A_n	–	–	–	ns	1.2	Fig. 6
		–	–	4.8		2.7	
		–	3.0*	4.4		3.0 to 3.6	
t_{PHL}/t_{PLH}	propagation delay LE_{BA} to A_n, LE_{AB} to B_n	–	–	–	ns	1.2	Fig. 7
		–	–	6.0		2.7	
		–	3.2*	5.4		3.0 to 3.6	
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}_{BA}$ to A_n, $\overline{CP}_{AB}$ to B_n	–	–	–	ns	1.2	
		–	–	6.0		2.7	
		–	3.2*	5.4		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_{BA}$ to A_n, OE_{AB} to B_n	–	–	–	ns	1.2	Fig. 8
		–	–	6.1		2.7	
		–	–	5.5		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time OE_{BA} to A_n, OE_{AB} to B_n	–	–	–	ns	1.2	
		–	–	6.1		2.7	
		–	–	5.5		3.0 to 3.6	

SYMBOL	PARAMETER		T_{amb} (°C)			UNIT	TEST CONDITIONS	
			−40 to +85				V_{CC} (V)	WAVEFORMS
			MIN.	TYP.	MAX.			
t_w	LE pulse width, LE_{AB} or LE_{BA} HIGH		–	–	–	ns	1.2	Fig. 7
			2.5	–	–		2.7 to 3.6	
	$\overline{CP}$ pulse width, $\overline{CP}_{AB}$ or $\overline{CP}_{BA}$ HIGH or LOW		–	–	–	ns	1.2	
			2.5	–	–		2.7 to 3.6	
t_{su}	set–up time, A_n before $\overline{CP}_{AB}$ ↓		–	–	–	ns	1.2	Fig. 9
			3	–	–		2.7 to 3.6	
	set–up time, B_n before $\overline{CP}_{AB}$ ↓		–	–	–	ns	1.2	
			3	–	–		2.7 to 3.6	
	set–up time, A_n before LE_{AB} ↓ or B_n before LE_{AB} ↓	$\overline{CP}$ high	–	–	–	ns	1.2	
			1.5	–	–		2.7 to 3.6	
		$\overline{CP}$ low	–	–	–	ns	1.2	
			4.5	–	–		2.7 to 3.6	
t_h	hold time, A_n after $\overline{CP}_{AB}$ ↓ or B_n before $\overline{CP}_{AB}$ ↓		–	–	–	ns	1.2	
			0	–	–		2.7 to 3.6	
	hold time, A_n after LE_{AB} ↓ or B_n before LE_{BA} ↓		–	–	–	ns	1.2	
			1	–	–		2.7 to 3.6	

Notes: All typical values are measured at T_{amb} = 25 °C.
* Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

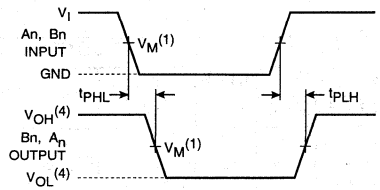


Fig.6 Waveforms showing the input (A_n, B_n) to output (B_n, A_n) propagation delay times.

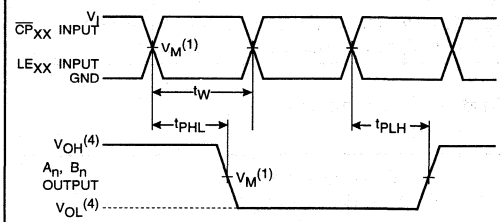


Fig.7 Waveforms showing the latch enable input (LE_{AB}, LE_{AB}) and clock pulse input ($\overline{CP}_{AB}$, $\overline{CP}_{BA}$) to output (A_n, B_n) propagation delays and latch enable pulse width

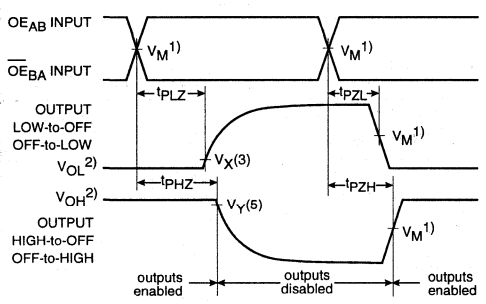


Fig.8 Waveforms showing the 3-state enable and disable times

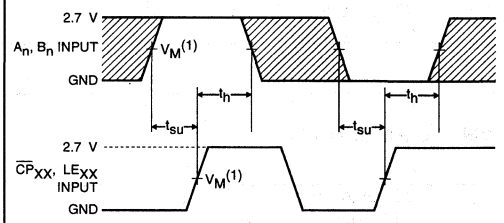
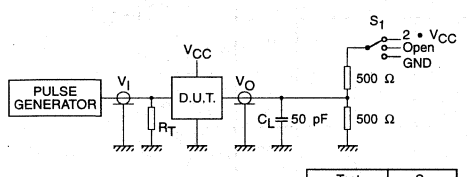


Fig.9 Waveforms showing the data set-up and hold times for the A_n and B_n inputs to the LE_{AB}, LE_{BA}, $\overline{CP}_{AB}$ and $\overline{CP}_{AB}$ inputs.
The shaded areas indicate when the input is permitted to change for predictable output performance.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.10 Load circuitry for switching times.

Notes:

(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(3) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

18-Bit Universal bus transceiver; 3-state — 74ALVC16501

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **CMOS low power consumption**
- **Direct interface with TTL levels**
- **Univeral bus transceiver with D-type latches and D-type Flip-flops capabable of operating in transparant, latched or clocked mode.**
- **All inputs have bushold circuitry**
- **Output drive capability 50Ω transmission lines @ 85 °C**
- **3-state non-inverting outputs for bus oriented applications**

DESCRIPTION

The 74ALVC16501 is an 18-bit universal bus transceiver.
Data flow in each direction is controlled by output enable (OE_{AB}, $\overline{OE}_{BA}$), latch-enable (LE_{AB}, LE_{BA}) and clock inputs (CP_{AB}, CP_{BA}).
When LE_{AB} is HIGH, the A-B dataflow is transparant. When LE_{AB} is LOW, and CP_{AB} is held at LOW or HIGH, the A data is latched; on the LOW-to-HIGH transition of CP_{AB} the A-data is stored in the latch/flip-flop. The outputs are active when OE_{AB} is HIGH. When OE_{AB} is LOW the B-outputs are in 3-state.
Similarly, the LE_{BA}, $\overline{OE}_{BA}$ and CP_{BA} control the B-to-A dataflow. Please note that both output enables are complementary: OE_{AB} is active HIGH, $\overline{OE}_{BA}$ is active LOW.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; LE_{AB} to A_n	C_L = 50 pF; V_{CC} = 3.3 V	3.0 3.2	ns
C_I	input capacitance		5.0	pF
$C_{I/O}$	input/output capacitance		10	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	22	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC16501DL	56	SSOP56	plastic	SSOP56/SOT371
74ALVC16501DGG	56	TSSOP56	plastic	TSSOP56/SOT364

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}_{AB}$	output enable A-to-B
2	LE_{AB}	latch enable A-to-B
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	A_0 to A_{17}	'A' data inputs/outputs
4, 11, 18, 25, 29, 32, 39, 46, 53, 56	GND	ground (0 V)
7, 22, 35, 50	V_{CC}	positive supply voltage
27	OE_{BA}	output enable B-to-A
28	LE_{BA}	latch enable B-to-A
30	CP_{BA}	clock input B-to-A, HIGH-to-LOW
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	B_0 to B_{17}	'B' data inputs/outputs
55	CP_{AB}	clock input A-to-B, HIGH-to-LOW

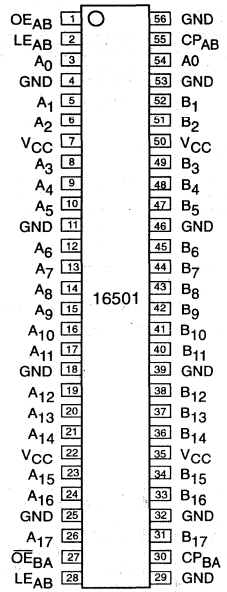


Fig.1 Pin configuration.

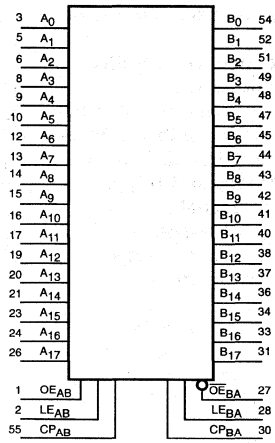


Fig.2 Logic symbol.

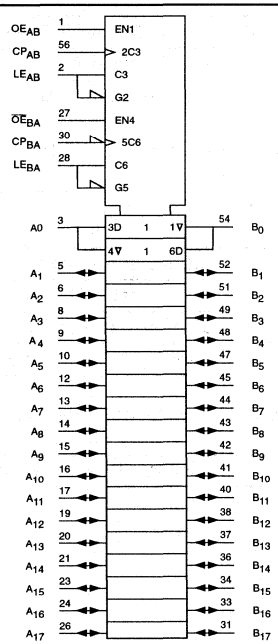


Fig.3 IEC Logic Symbol

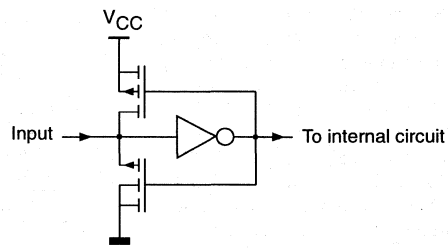


Fig.4 Bushold circuit

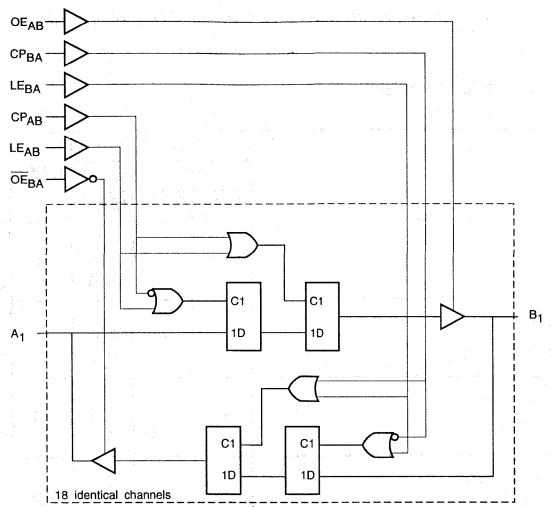


Fig.4 Logic diagram (one section)

FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
OE_{AB} [1]	LE_{XX}	CP_{XX}	DATA		
L	X	X	X	Z	Disabled
H H	H H	X X	H L	H L	Transparant
L L	L L	↑ ↑	h l	Z Z	Disabled + latch
H H	L L	↑ ↑	h l	H L	Latch + display
H H	L L	L H	X X	NC NC1	Hold

XX = AB for A-to-B direction, BA for B-to-A direction
H = HIGH voltage level
L = LOW voltage level
h = High state must be present one setup time before the low-to-high transition of CP
l = Low state must be present one setup time before the low-to-high transition of CP
X = Don't care
↑ = LOW-to-HIGH level transition
NC = No change
NC1 = No change provided that CP was LOW before LE_{XX} went low
Z = High impedance "off" state

[1] For the B-to-A direcion $\overline{OE}_{BA}$ is the inverse of OE_{AB}

DC CHARACTERISTICS FOR 74ALVC16501

For the DC characteristics see chapter "ALVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74ALVC16501

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C) −40 to +85 MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay A_n to B_n, B_n to A_n	–	–	–	ns	1.2	Fig. 6
		–	–	4.8		2.7	
		–	3.0*	4.4		3.0 to 3.6	
t_{PHL}/t_{PLH}	propagation delay LE_{BA} to A_n, LE_{AB} to B_n	–	–	–	ns	1.2	Fig. 7
		–	–	6.0		2.7	
		–	3.2*	5.4		3.0 to 3.6	
t_{PHL}/t_{PLH}	propagation delay CP_{BA} to A_n, CP_{AB} to B_n	–	–	–	ns	1.2	
		–	–	6.0		2.7	
		–	3.2*	5.4		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_{BA}$ to A_n, OE_{AB} to B_n	–	–	–	ns	1.2	Fig. 8
		–	–	6.1		2.7	
		–	–	5.5		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time OE_{BA} to A_n, OE_{AB} to B_n	–	–	–	ns	1.2	
		–	–	6.1		2.7	
		–	–	5.5		3.0 to 3.6	

SYMBOL	PARAMETER		T_{amb} (°C) −40 to +85 MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS V_{CC} (V)	WAVEFORMS
t_W	LE pulse width, LE_{AB} or LE_{BA} HIGH		–	–	–	ns	1.2	Fig.7
			2.5	–	–		2.7 to 3.6	
	LE pulse width, CP_{AB} or CP_{BA} HIGH or LOW		–	–	–		1.2	
			2.5	–	–		2.7 to 3.6	
t_{su}	set–up time, A_n before CP_{AB} ↓		–	–	–	ns	1.2	Fig.9
			3	–	–		2.7 to 3.6	
	set–up time, B_n before CP_{AB} ↓		–	–	–		1.2	
			3	–	–		2.7 to 3.6	
	set–up time, A_n before LE_{AB} ↓ or B_n before LE_{AB} ↓	CP high	–	–	–		1.2	
			1.5	–	–		2.7 to 3.6	
		CP low	–	–	–		1.2	
			1.5	–	–		2.7 to 3.6	
t_h	hold time, A_n after CP_{AB} ↓ or B_n before CP_{AB} ↓		–	–	–	ns	1.2	
			0	–	–		2.7 to 3.6	
	hold time, A_n after LE_{AB} ↓ or B_n before LE_{BA} ↓		–	–	–		1.2	
			1	–	–		2.7 to 3.6	

Notes: All typical values are measured at T_{amb} = 25 °C.
* Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

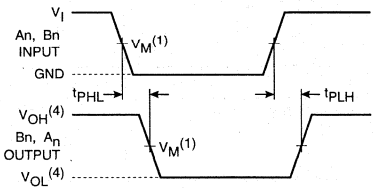


Fig.6 Waveforms showing the input (A_n, B_n) to output (B_n, A_n) propagation delays.

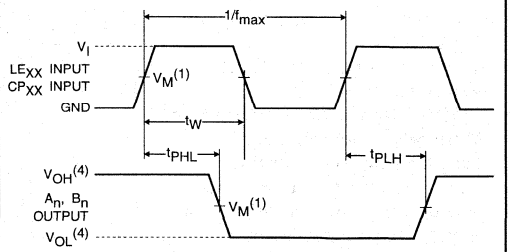


Fig.7 Waveforms showing the latch enable input (E_{AB}, LE_{BA}) and clock pulse input (CP_{AB}, CP_{BA}) to output propagation delays and their pulse width.

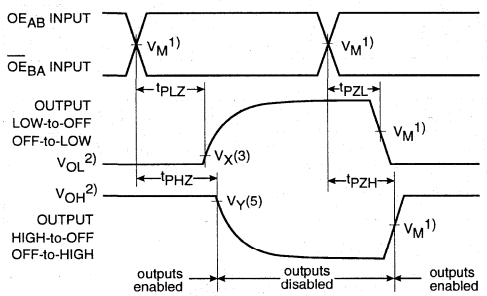


Fig.8 Waveforms showing the 3-state enable and disable times

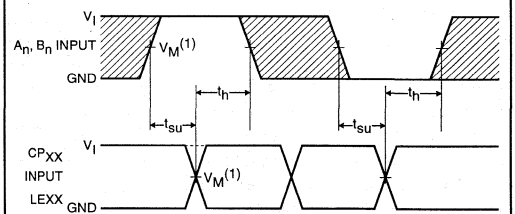
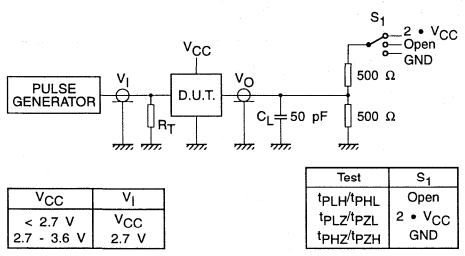


Fig.9 Waveforms showing the data set-up and hold times for the A_n and B_n inputs to the LE_{AB}, LE_{BA}, CP_{AB} and CP_{AB} inputs.
The shaded areas indicate when the input is permitted to change for predictable output performance.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.10 Load circuitry for switching times.

Notes:

(1) V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
V_M = 0.5 · V_{CC} at V_{CC} < 2.7 V

(2) $V_X = V_{OL}$ + 0.3 V at $V_{CC} \geq$ 2.7 V
$V_X = V_{OL}$ + 0.1 · V_{CC} at V_{CC} < 2.7 V

(3) $V_Y = V_{OH}$ − 0.3 V at $V_{CC} \geq$ 2.7 V
$V_Y = V_{OH}$ − 0.1 · V_{CC} at V_{CC} < 2.7 V

(4) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no.8-1A**
- **CMOS low power consumption**
- **Multibyte™ flow-through standard pin-out architecture**
- **Low inductance multiple power and ground pins for minimum noise and ground bounce**
- **Direct interface with TTL levels**
- **All data inputs have bushold**
- **Output drive capability 50 Ω transmission lines @ 85 °C**

DESCRIPTION

The 74ALVC16540 is a high-performance, low-power, low-voltage, Si-gate CMOS device superior to most advanced CMOS compatible TTL families.

The 74ALVC16540 is a 16-bit inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $1\overline{OE}_n$ and $2\overline{OE}_n$. A HIGH on $n\overline{OE}_n$ causes the outputs to assume a high impedance OFF-state. The "16540" is identical to the "16541" but has inverting outputs.

FUNCTION TABLE

INPUTS			OUTPUT
$n\overline{OE}_1$	$n\overline{OE}_2$	nA_n	nY_n
L	L	L	H
L	L	H	L
X	H	X	Z
H	X	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	C_L = 50 pF; V_{CC} = 3.3 V	2.1	ns
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	30	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC16540DL	48	SSOP48	plastic	SSOP48/SOT370
74ALVC16540DGG	48	TSSOP48	plastic	TSSOP48/SOT362

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 24	$n\overline{OE}_1$	'1' output enable input (active LOW)
2, 3, 5, 6, 8, 9, 11, 12	$1Y_0$ to $1Y_7$	'1Y' data outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	ground (0 V)
7, 18, 31, 42	V_{CC}	positive supply voltage
13, 14, 16, 17, 19, 20, 22, 23	$2Y_0$ to $2Y_7$	'2Y' data outputs
25, 48	$n\overline{OE}_2$	'2' output enable input (active LOW)
36, 35, 33, 32, 30, 29, 27, 26	$2A_0$ to $2A_7$	'2A' data inputs
47, 46, 44, 43, 41, 40, 38, 37	$1A_0$ to $1A_7$	'1A' data inputs

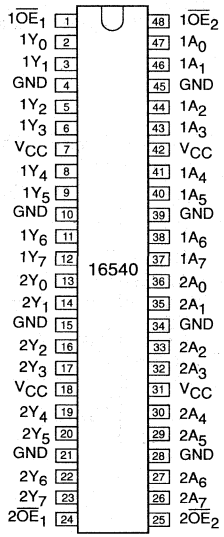


Fig.1 Pin configuration.

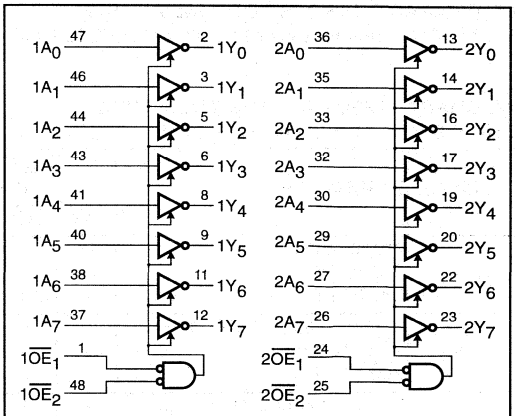


Fig.2 Logic symbol.

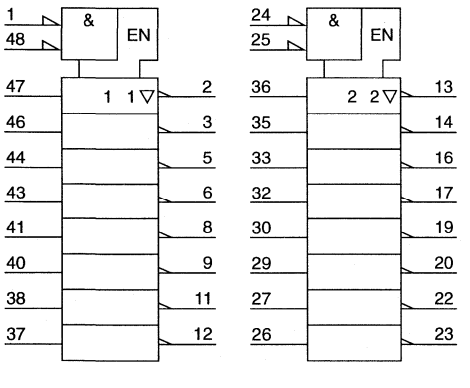


Fig.3 IEC logic symbol.

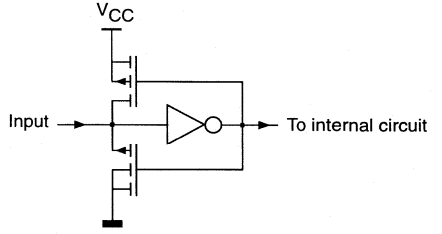


Fig.4 Bushold circuit.

DC CHARACTERISTICS FOR 74ALVC16540

For the DC characteristics see chapter "ALVC16 family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74ALVC16540

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C) −40 to +85			UNIT	TEST CONDITIONS	
		MIN.	TYP.	MAX.		V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay	–	–	–	ns	1.2	Fig. 5
	$1A_n$ to $1Y_n$;	–	–	4.5		2.7	
	$2A_n$ to $2Y_n$	–	2.1*	4.0		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time	–	–	–	ns	1.2	Figs 6, 7
	$1\overline{OE}_n$ to $1Y_n$;	–	–	5.5		2.7	
	$2\overline{OE}_n$ to $2Y_n$	–	–	4.7		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time	–	–	–	ns	1.2	Figs 6, 7
	$1\overline{OE}_n$ to $1Y_n$;	–	–	6.0		2.7	
	$2\overline{OE}_n$ to $2Y_n$	–	–	5.0		3.0 to 3.6	

Notes: All typical values are measured at T_{amb} = 25 °C.
* Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

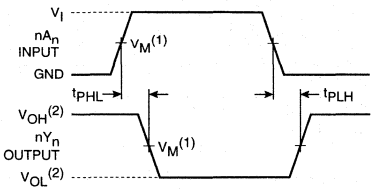


Fig.5 Waveforms showing the input (A_n) to output (Y_n) propagation delay times.

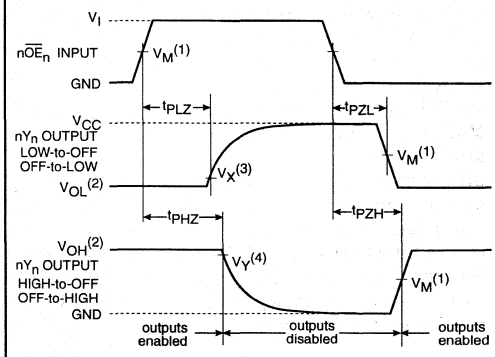
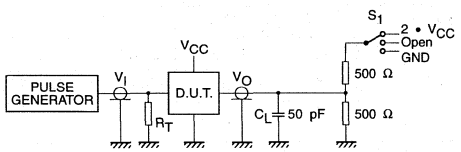


Fig.6 Waveforms showing the 3-state enable and disable times.



V_{CC}	V_I
< 2.7 V 2.7 - 3.6 V	V_{CC} 2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.7 Load circuitry for switching times.

Notes:

(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no.8-1A**
- **CMOS low power consumption**
- **Multibyte™ flow-through standard pin-out architecture**
- **Low inductance multiple power and ground pins for minimum noise and ground bounce**
- **Direct interface with TTL levels**
- **All data inputs have bushold**
- **Output drive capability 50 Ω transmission lines @ 85 °C**

DESCRIPTION

The 74ALVC16541 is a high-performance, low-power, low-voltage, Si-gate CMOS device superior to most advanced CMOS compatible TTL families.

The 74ALVC16541 is a 16-bit buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $1\overline{OE}_n$ and $2\overline{OE}_n$. A HIGH on $n\overline{OE}_n$ causes the outputs to assume a high impedance OFF-state. The "16541" is identical to the "16541" but has non-inverting outputs.

FUNCTION TABLE

INPUTS			OUTPUT
$n\overline{OE}_1$	$n\overline{OE}_2$	nA_n	nY_n
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	C_L = 50 pF; V_{CC} = 3.3 V	2.1	ns
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	30	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC16541DL	48	SSOP48	plastic	SSOP48/SOT370
74ALVC16541DGG	48	TSSOP48	plastic	TSSOP48/SOT362

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 24	$n\overline{OE}_1$	'1' output enable input (active LOW)
2, 3, 5, 6, 8, 9, 11, 12	$1Y_0$ to $1Y_7$	'1Y' data outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	ground (0 V)
7, 18, 31, 42	V_{CC}	positive supply voltage
13, 14, 16, 17, 19, 20, 22, 23	$2Y_0$ to $2Y_7$	'2Y' data outputs
25, 48	$n\overline{OE}_2$	'2' output enable input (active LOW)
36, 35, 33, 32, 30, 29, 27, 26	$2A_0$ to $2A_7$	'2A' data inputs
47, 46, 44, 43, 41, 40, 38, 37	$1A_0$ to $1A_7$	'1A' data inputs

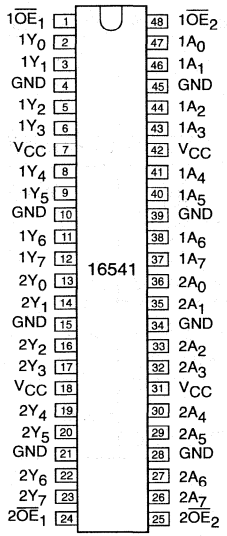


Fig.1 Pin configuration.

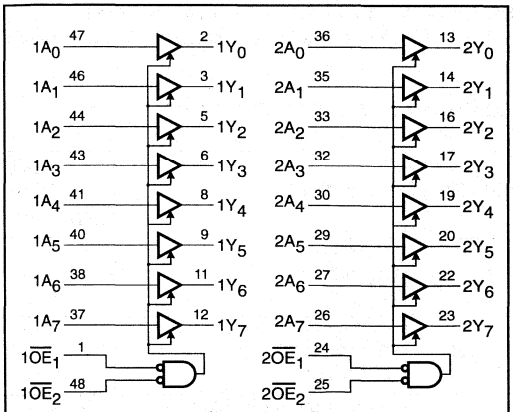


Fig.2 Logic symbol.

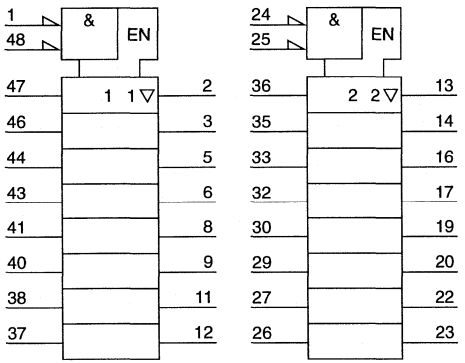


Fig.3 IEC logic symbol.

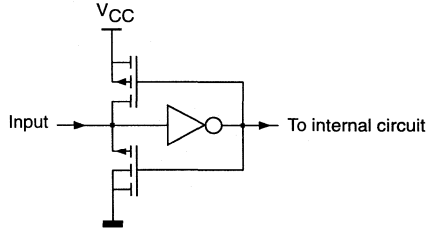


Fig.4 Bushold circuit.

DC CHARACTERISTICS FOR 74ALVC16541

For the DC characteristics see chapter "ALVC16 family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74ALVC16541

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C) −40 to +85			UNIT	TEST CONDITIONS	
		MIN.	TYP.	MAX.		V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay	–	–	–	ns	1.2	Fig. 5
	$1A_n$ to $1Y_n$;	–	–	4.2		2.7	
	$2A_n$ to $2Y_n$	–	2.1*	3.6		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time	–	–	–	ns	1.2	Fig. 6
	$1\overline{OE}_n$ to $1Y_n$;	–	–	5.5		2.7	
	$2\overline{OE}_n$ to $2Y_n$	–	–	4.7		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time	–	–	–	ns	1.2	Fig. 6
	$1\overline{OE}_n$ to $1Y_n$;	–	–	6.0		2.7	
	$2\overline{OE}_n$ to $2Y_n$	–	–	5.0		3.0 to 3.6	

Notes: All typical values are measured at T_{amb} = 25 °C.
* Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

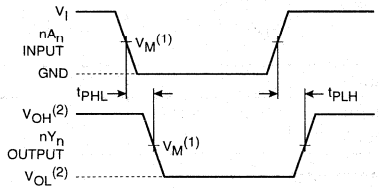


Fig.5 Waveforms showing the input (A_n) to output (Y_n) propagation delay times.

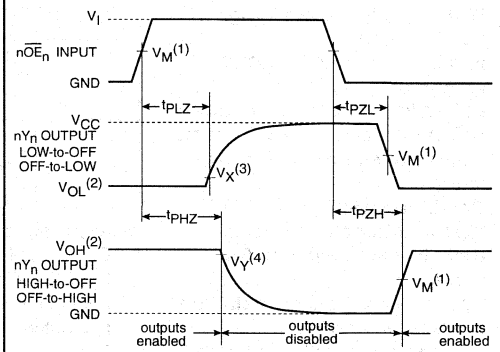
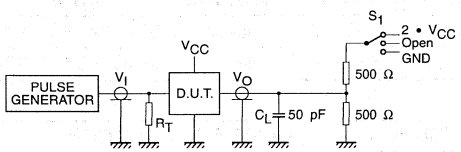


Fig.6 Waveforms showing the 3-state enable and disable times.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.7 Load circuitry for switching times.

Notes:

(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

16-Bit D-type registered transceiver; 3-state — 74ALVC16543

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **CMOS low power consumption**
- **Direct interface with TTL levels**
- **16-Bit transceiver with D-type latch**
- **Combines '16245 and '16373 type functions in one chip**
- **Back-to-back registers for storage**
- **Separate controls for data flow in each direction**
- **3-state non-inverting outputs for bus oriented applications**

DESCRIPTION

The 74ALVC16543 is a dual octal registered transceiver. Each section contains two sets of D-type latches for temporary storage of the data flow in either direction. Separate latch enable ($\overline{LE}_{AB}$, $\overline{LE}_{BA}$) and output enable ($\overline{OE}_{AB}$, $\overline{OE}_{BA}$) inputs are provided for each register to permit independent control in either direction of the data flow.

The '16543' contains two sections each consisting of two sets of eight D-type latches with separate inputs and controls for each set. For data flow from A to B, for example, the A-to-B enable ($n\overline{E}_{AB}$, where n equals 1 or 2) input must be LOW in order to enter data from nA_0-nA_7 or take data from nB_0-nB_7, as indicated in the function table. With $n\overline{E}_{AB}$ LOW, a LOW signal on the A-to-B latch enable ($n\overline{LE}_{AB}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $n\overline{LE}_{AB}$ signal stores the A data into the latches.With $\overline{E}_{AB}$ and $\overline{OE}_{AB}$ both LOW, the 3-state B output buffers are active and display the data present at the output of the A latches. Similarly, the $\overline{E}_{BA}$, $\overline{LE}_{BA}$ and $\overline{OE}_{BA}$ signals control the data flow from B-to-A.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n; LE to Q_n	C_L = 50 pF; V_{CC} = 3.3 V	3.0 3.2	ns
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	22	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC16543DL	56	SSOP56	plastic	SSOP56/SOT371
74ALVC16543DGG	56	TSSOP56	plastic	TSSOP56/SOT364

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 28	$n\overline{OE}_{AB}$	Output enable A-to-B for register 1 or 2
2, 27	$n\overline{LE}_{AB}$	Latch enable A-to-B for register 1 or 2
3, 26	$n\overline{E}_{AB}$	A-to-B enable for register 1 or 2
5, 6, 8, 9, 10, 12, 13, 14	$1A_0$ to $1A_7$	'1A' data inputs/outputs
4, 11, 18, 25, 32, 39, 46, 53	GND	ground (0 V)
7, 22, 35, 50	V_{CC}	positive supply voltage
15, 16, 17, 19, 20, 21, 23, 24	$2B_0$ to $2B_7$	'2B' data inputs/outputs
29, 56	$n\overline{OE}_{BA}$	Output enable B-to-A for register 1 or 2
30, 55	$n\overline{LE}_{BA}$	Latch enable B-to-A for register 1 or 2
31, 54	$n\overline{E}_{BA}$	B-to-A enable for register 1 or 2
42, 41, 40, 38, 37, 36, 34, 33	$2B_0$ to $2B_7$	'2B' data inputs/outputs
52, 51, 49, 48, 47, 45, 44, 43	$1B_0$ to $1B_7$	'1B' data inputs/outputs

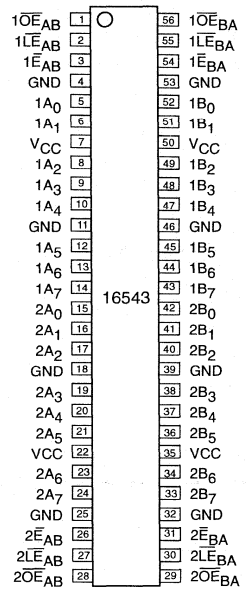


Fig.1 Pin configuration.

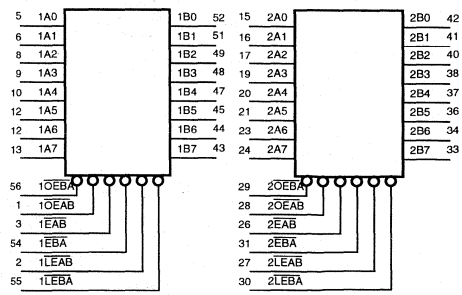


Fig.2 Logic symbol.

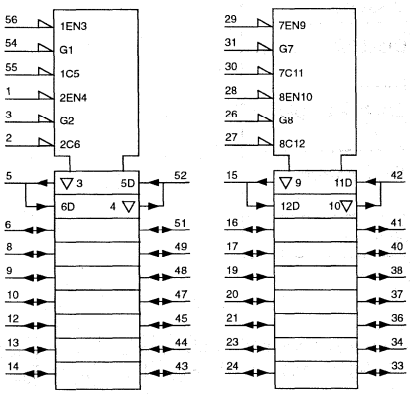


Fig.3 IEC Logic Symbol

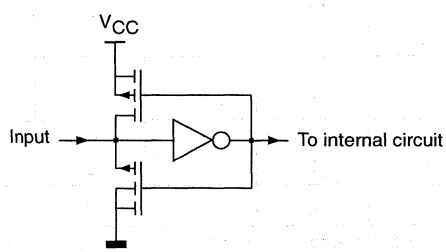


Fig.4 Functional diagram

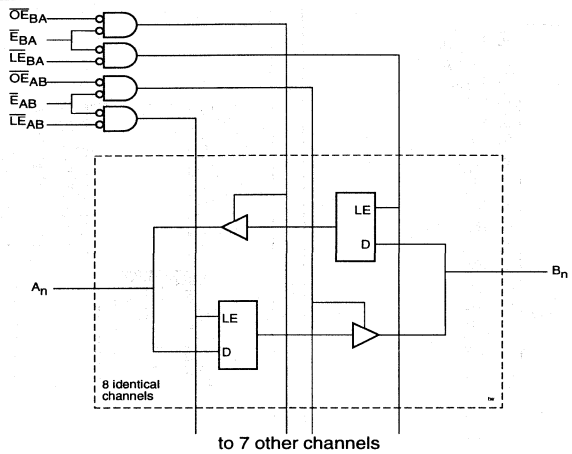


Fig.5 Logic diagram (one section)

FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
$\overline{OE}_{XX}$	$\overline{E}_{XX}$	$\overline{LE}_{XX}$	DATA		
H	X	X	X	Z	Disabled
X	H	X	X	Z	Disables
L L	↑ ↑	L L	h l	Z Z	Disabled + Latch
L L	L L	↑ ↑	h l	H L	Latch + Display
L L	L L	L L	H L	H L	Transparent
L	L	H	X	NC	Hold

XX = AB for A-to-B direction, BA for B-to-A direction
H = HIGH voltage level
L = LOW voltage level
h = High state must be present one setup time before the low-to-high transition of $\overline{LE}_{AB}$, $\overline{LE}_{BA}$, $\overline{E}_{AB}$ or $\overline{E}_{BA}$
l = Low state must be present one setup time before the low-to-high transition of $\overline{LE}_{AB}$, $\overline{LE}_{BA}$, $\overline{E}_{AB}$ or $\overline{E}_{BA}$
X = Don't care
↑ = LOW-to-HIGH level transition
NC = No change
Z = High impedance "off" state

DC CHARACTERISTICS FOR 74ALVC16543

For the DC characteristics see chapter "ALVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74ALVC16543

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		−40 to +85				V_{CC} (V)	WAVEFORMS
		MIN.		MAX.			
t_{PHL}/t_{PLH}	propagation delay A_n to B_n, B_n to A_n	–	–	18.0	ns	1.2	Fig.6
		–	–	4.8		2.7	
		–	3.0*	4.4		3.0 to 3.6	
t_{PHL}/t_{PLH}	propagation delay $\overline{LE}_{BA}$ to A_n, $\overline{LE}_{AB}$ to B_n	–	–	20.0	ns	1.2	Fig.6
		–	–	6.0		2.7	
		–	3.2*	5.4		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_{BA}$ to A_n, $\overline{OE}_{AB}$ to B_n	–	–	22.0	ns	1.2	Fig.7
		–	–	6.1		2.7	
		–	–	5.5		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_{BA}$ to A_n, $\overline{OE}_{AB}$ to B_n	–	–	22.0	ns	1.2	Fig.7
		–	–	6.1		2.7	
		–	–	5.5		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time $\overline{E}_{BA}$ to A_n, $\overline{E}_{AB}$ to B_n	–	–	22.0	ns	1.2	Fig.8
		–	–	6.1		2.7	
		–	–	5.5		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{E}_{BA}$ to A_n, $\overline{E}_{AB}$ to B_n	–	–	22.0	ns	1.2	Fig.8
		–	–	6.1		2.7	
		–	–	5.5		3.0 to 3.6	

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		−40 to +85				V_{CC} (V)	WAVEFORMS
		MIN.		MAX.			
t_W	LE pulse width LOW	2.8	–	–	ns	2.7	Fig.7
		2.5	–	–		3.0 to 3.6	
t_{su}	set-up time A_n/B_n to $\overline{LE}_{XX}$, A_n/B_n to $\overline{E}_{XX}$	2.2	–	–	ns	1.2	Fig.9
		0.7	–	–		2.7	
		0.6	–	–		3.0 to 3.6	
t_h	hold time A_n/B_n to $\overline{LE}_{XX}$, A_n/B_n to $\overline{E}_{XX}$	2.2	–	–	ns	1.2	Fig.9
		0.7	–	–		2.7	
		0.6	–	–		3.0 to 3.6	

Notes: All typical values are measured at T_{amb} = 25 °C.
* Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

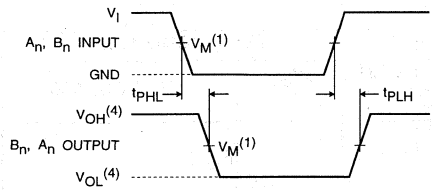


Fig.6 Waveforms showing the input (D_n) to output (Q_n) propagation delay times.

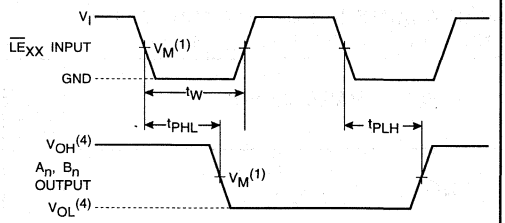


Fig.7 Waveforms showing the latch enable input ($\overline{LE}_{XX}$) pulse width, the latch enable input to output (Q_n) propagation delay times.

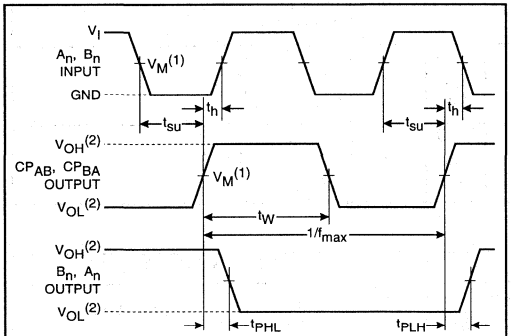


Fig.8 Waveforms showing the 3-state enable and disable times

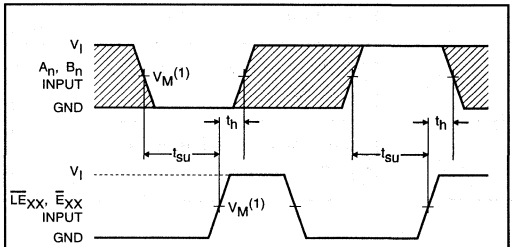
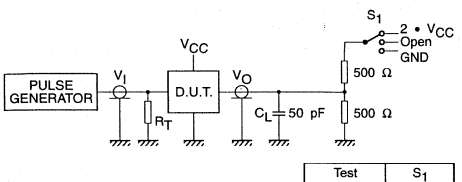


Fig.9 Waveforms showing the data set-up and hold times for the D_n input to the LE input.

Note to Fig.9:

The shaded areas indicate when the input is permitted to change for predictable output performance.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.10 Load circuitry for switching times.

Notes:

(1) V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
V_M = 0.5 · V_{CC} at V_{CC} < 2.7 V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

(3) $V_X = V_{OL}$ + 0.3 V at $V_{CC} \geq$ 2.7 V
$V_X = V_{OL}$ + 0.1 · V_{CC} at V_{CC} < 2.7 V

(4) $V_Y = V_{OH}$ − 0.3 V at $V_{CC} \geq$ 2.7 V
$V_Y = V_{OH}$ − 0.1 · V_{CC} at V_{CC} < 2.7 V

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **CMOS low power consumption**
- **Direct interface with TTL levels**
- **Univeral bus transceiver with D-type latches and D-type Flip-flops capabable of operating in transparant, latched, clocked or clocked-enabled mode.**
- **All inputs have bushold circuitry**
- **Output drive capability 50Ω transmission lines @ 85 °C**
- **3-state non-inverting outputs for bus oriented applications**

DESCRIPTION

The 74ALVC16600 is an 18-bit universal bus transceiver.
Data flow in each direction is controlled by output enable ($\overline{OE}_{AB}$, $\overline{OE}_{BA}$), latch-enable (LE_{AB}, LE_{BA}) and clock inputs ($\overline{CP}_{AB}$, $\overline{CP}_{BA}$). The clock enable inputs (CE_{AB}, $\overline{CE}_{BA}$) control the clock.
When LE_{AB} is HIGH, the A-B dataflow is transparant. When LE_{AB} is LOW, and $\overline{CP}_{AB}$ is held at LOW or HIGH, the A data is latched; on the HIGH-to-LOW transition of $\overline{CP}_{AB}$ the A-data is stored in the latch/flip-flop. The outputs are active when $\overline{OE}_{AB}$ is LOW. When $\overline{OE}_{AB}$ is LOW the B-outputs are in 3-state.
Similarly, the LE_{BA}, $\overline{OE}_{BA}$ and $\overline{CP}_{BA}$ control the B-to-A dataflow.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n to B_n LE_{AB} to A_n	C_L = 50 pF V_{CC} = 3.3 V	 3.0 3.2	ns
C_I	input capacitance		5.0	pF
$C_{I/O}$	input/output capacitance		10	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	22	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC16600DL	56	SSOP56	plastic	SSOP56/SOT371
74ALVC16600DGG	56	TSSOP56	plastic	TSSOP56/SOT364

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}_{AB}$	Output enable A-to-B
2	LE_{AB}	Latch enable A-to-B
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	A_0 to A_{17}	'A' data inputs/outputs
4, 11, 18, 25, 29, 32, 39, 46, 53, 56	GND	ground (0 V)
7, 22, 35, 50	V_{CC}	positive supply voltage
27	$\overline{OE}_{BA}$	Output enable B-to-A
28	LE_{BA}	Latch enable B-to-A
30	$\overline{CP}_{BA}$	Clock input B-to-A, HIGH-to-LOW
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	B_0 to B_{17}	'B' data inputs/outputs
55	$\overline{CP}_{AB}$	Clock input A-to-B, HIGH-to-LOW

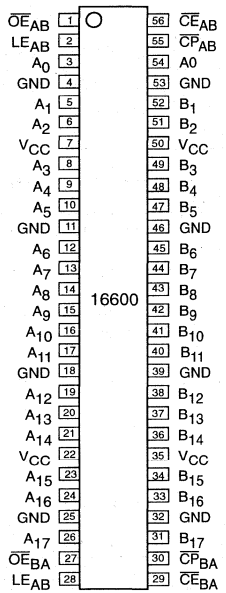


Fig.1 Pin configuration.

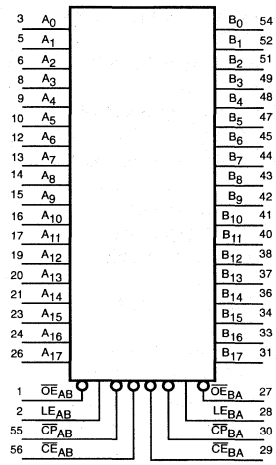


Fig.2 Logic symbol.

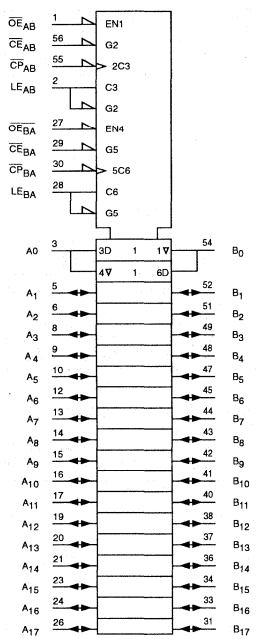


Fig.3 IEC Logic Symbol

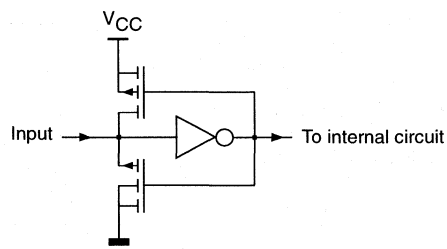


Fig.4 Bushold circuit

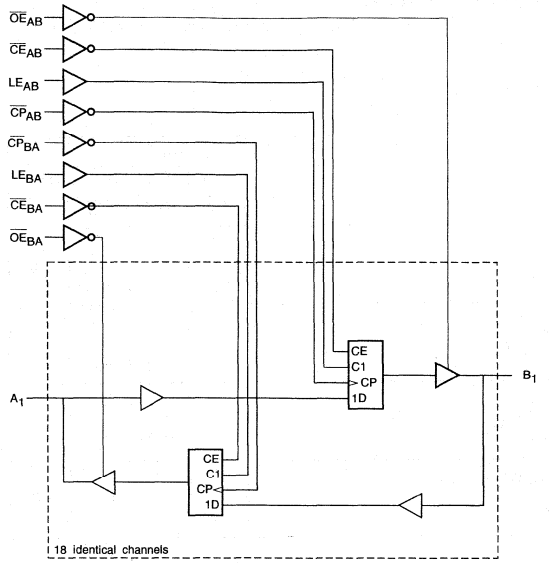


Fig.4 Logic diagram (one section)

FUNCTION TABLE

INPUTS					OUTPUTS	STATUS
$\overline{CE}_{XX}$	$\overline{OE}_{XX}$	LE_{XX}	$\overline{CP}_{XX}$	DATA		
X	H	X	X	X	Z	Disabled
X	L	H	X	H	H	Transparant
X	L	H	X	L	L	
H	L	L	X	X	NC	Hold
H	L	L	X	X	NC1	
L	L	L	↓	h	Z	Disabled + latch
L	L	L	↓	l	Z	
L	L	L	↓	h	H	Latch + display
L	L	L	↓	l	L	
L	L	L	H	X	NC	Hold
L	L	L	L	X	NC1	

XX = AB for A-to-B direction, BA for B-to-A direction
H = HIGH voltage level
L = LOW voltage level
h = High state must be present one setup time before the low-to-high transition of $\overline{CP}_{XX}$
l = Low state must be present one setup time before the low-to-high transition of $\overline{CP}_{XX}$
X = Don't care
↓ = HIGH-to-LOW level transition
NC = No change
NC1 = No change provided that $\overline{CP}_{XX}$ was LOW before LE_{XX} went low
Z = High impedance "off" state

DC CHARACTERISTICS FOR 74ALVC16600

For the DC characteristics see chapter "ALVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74ALVC16600

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C) −40 to +85 MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay A_n to B_n, B_n to A_n	–	–	18.0	ns	1.2	Fig.6
		–	–	4.8		2.7	
		–	3.0*	4.4		3.0 to 3.6	
t_{PHL}/t_{PLH}	propagation delay LE_{BA} to A_n, LE_{AB} to B_n	–	–	20.0	ns	1.2	Fig.7
		–	–	6.0		2.7	
		–	3.2*	5.4		3.0 to 3.6	
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}_{BA}$ to A_n, $\overline{CP}_{AB}$ to B_n	–	–	20.0	ns	1.2	
		–	–	6.0		2.7	
		–	3.2*	5.4		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_{BA}$ to A_n, OE_{AB} to B_n	–	–	22.0	ns	1.2	Fig.8
		–	–	6.1		2.7	
		–	–	5.5		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time OE_{BA} to A_n, OE_{AB} to B_n	–	–	22.0	ns	1.2	
		–	–	6.1		2.7	
		–	–	5.5		3.0 to 3.6	

SYMBOL	PARAMETER		T_{amb} (°C) −40 to +85 MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS V_{CC} (V)	WAVEFORMS
t_w	LE pulse width, LE_{AB} or LE_{BA} HIGH		–	–	–	ns	1.2	Fig. 7
			2.5	–	–		2.7 to 3.6	
	LE pulse width, $\overline{CP}_{AB}$ or $\overline{CP}_{BA}$ HIGH or LOW		–	–	–		1.2	
			2.5	–	–		2.7 to 3.6	
t_{su}	set–up time, A_n before $\overline{CP}_{AB}$ ↓		–	–	–	ns	1.2	Fig.9
			3	–	–		2.7 to 3.6	
	set–up time, B_n before $\overline{CP}_{AB}$ ↓		–	–	–		1.2	
			3	–	–		2.7 to 3.6	
	set–up time, A_n before LE_{AB} ↓ or B_n before LE_{AB} ↓	$\overline{CP}$ high	–	–	–		1.2	
			1.5	–	–		2.7 to 3.6	
		$\overline{CP}$ low	–	–	–		1.2	
			1.5	–	–		2.7 to 3.6	
t_h	hold time, A_n after $\overline{CP}_{AB}$ ↓ or B_n before $\overline{CP}_{AB}$ ↓		–	–	–	ns	1.2	
			0	–	–		2.7 to 3.6	
	hold time, A_n after LE_{AB} ↓ or B_n before LE_{BA} ↓		–	–	–		1.2	
			1	–	–		2.7 to 3.6	

Notes: All typical values are measured at T_{amb} = 25 °C.
* Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

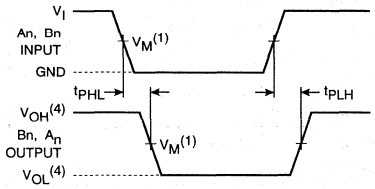


Fig.6 Waveforms showing the input (A_n, B_n) to output (B_n, A_n) propagation delay times.

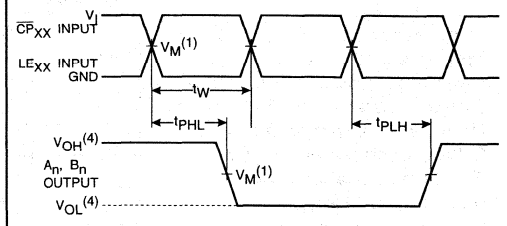


Fig.7 Waveforms showing the latch enable input (LE_{AB}, LE_{AB}) and clock pulse input ($\overline{CP}_{AB}$, $\overline{CP}_{BA}$) to output (A_n, B_n) propagation delays and latch enable pulse width

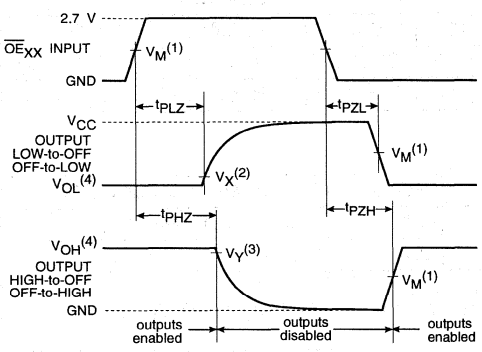


Fig.8 Waveforms showing the 3-state enable and disable times

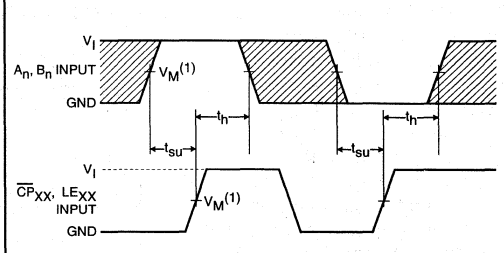
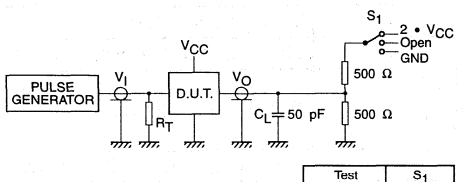


Fig.9 Waveforms showing the data set-up and hold times for the A_n and B_n inputs to the LE_{AB}, LE_{BA}, $\overline{CP}_{AB}$ and $\overline{CP}_{AB}$ inputs.
The shaded areas indicate when the input is permitted to change for predictable output performance.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.10 Load circuitry for switching times.

Notes:

(1) V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
$V_M = 0.5 \cdot V_{CC}$ at V_{CC} < 2.7 V

(2) $V_X = V_{OL}$ + 0.3 V at $V_{CC} \geq$ 2.7 V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at V_{CC} < 2.7 V

(3) $V_Y = V_{OH}$ − 0.3 V at $V_{CC} \geq$ 2.7 V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at V_{CC} < 2.7 V

(4) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

18-Bit Universal bus transceiver; 3-state | 74ALVC16601

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **CMOS low power consumption**
- **Direct interface with TTL levels**
- **Univeral bus transceiver with D-type latches and D-type Flip-flops capabable of operating in transparant, latched or clocked mode.**
- **All inputs have bushold circuitry**
- **Output drive capability 50Ω transmission lines @ 85 °C**
- **3-state non-inverting outputs for bus oriented applications**

DESCRIPTION

The 74ALVC16601 is an 18-bit universal bus transceiver.
Data flow in each direction is controlled by output enable (OE_{AB}, $\overline{OE}_{BA}$), latch-enable (LE_{AB}, LE_{BA}) and clock inputs (CP_{AB}, CP_{BA}).
When LE_{AB} is HIGH, the A-B dataflow is transparant. When LE_{AB} is LOW, and CP_{AB} is held at LOW or HIGH, the A data is latched; on the LOW-to-HIGH transition of CP_{AB} the A-data is stored in the latch/flip-flop. The outputs are active when OE_{AB} is HIGH. When OE_{AB} is LOW the B-outputs are in 3-state.

Similarly, the LE_{BA}, $\overline{OE}_{BA}$ and CP_{BA} control the B-to-A dataflow. Please note that both output enables are complementary: OE_{AB} is active HIGH, $\overline{OE}_{BA}$ is active LOW.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n to B_n LE_{AB} to A_n	C_L = 50 pF V_{CC} = 3.3 V	3.0 3.2	ns
C_I	input capacitance		5.0	pF
$C_{I/O}$	input/output capacitance		10	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	22	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC16601DL	56	SSOP56	plastic	SSOP56/SOT371
74ALVC16601DGG	56	TSSOP56	plastic	TSSOP56/SOT364

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}_{AB}$	Output enable A-to-B
2	LE_{AB}	Latch enable A-to-B
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	A_0 to A_{17}	'A' data inputs/outputs
4, 11, 18, 25, 29, 32, 39, 46, 53, 56	GND	ground (0 V)
7, 22, 35, 50	V_{CC}	positive supply voltage
27	$\overline{OE}_{BA}$	Output enable B-to-A
28	LE_{BA}	Latch enable B-to-A
30	CP_{BA}	Clock input B-to-A, HIGH-to-LOW
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	B_0 to B_{17}	'B' data inputs/outputs
55	CP_{AB}	Clock input A-to-B, HIGH-to-LOW

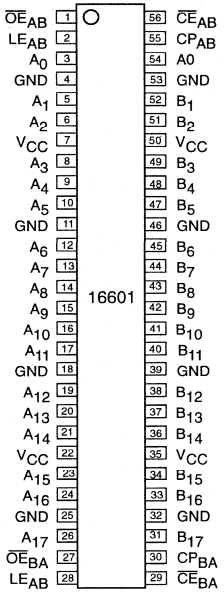


Fig.1 Pin configuration.

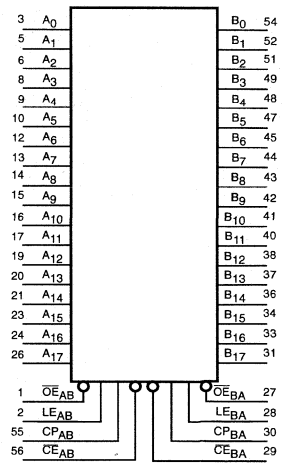


Fig.2 Logic symbol.

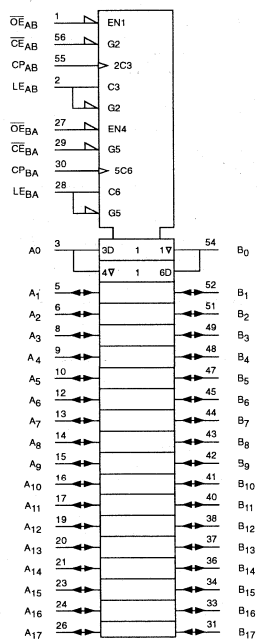


Fig.3 IEC Logic Symbol

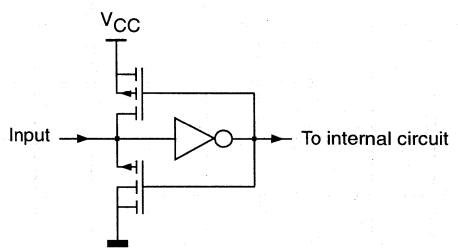


Fig.4 Bushold circuit

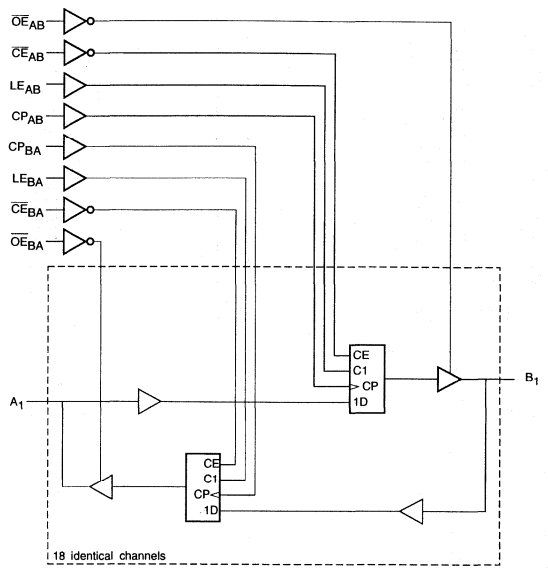


Fig.4 Logic diagram (one section)

FUNCTION TABLE

INPUTS					OUTPUTS	STATUS
$\overline{CE}_{xx}$	$\overline{OE}_{xx}$	LE_{xx}	CP_{xx}	DATA		
X	H	X	X	X	Z	Disabled
X X	L L	H H	X X	H L	H L	Transparant
H H	L L	L L	X X	X X	NC NC1	Hold
L L	L L	L L	↑ ↑	h l	Z Z	Disabled + latch
L L	L L	L L	↑ ↑	h l	H L	Latch + display
L L	L L	L L	L H	X X	NC NC1	Hold

XX = AB for A-to-B direction, BA for B-to-A direction
H = HIGH voltage level
L = LOW voltage level
h = High state must be present one setup time before the low-to-high transition of CP_{xx}
l = Low state must be present one setup time before the low-to-high transition of CP_{xx}
X = Don't care
↑ = LOW-to-HIGH level transition
NC = No change
NC1 = No change provided that CP_{xx} was LOW before LE_{xx} went low
Z = High impedance "off" state

DC CHARACTERISTICS FOR 74ALVC16601

For the DC characteristics see chapter "ALVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74ALVC16601

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C) −40 to +85 MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay A_n to B_n, B_n to A_n	–	–	18.0	ns	1.2	Fig.6
		–	–	4.8		2.7	
		–	3.0*	4.4		3.0 to 3.6	
t_{PHL}/t_{PLH}	propagation delay LE_{BA} to A_n, LE_{AB} to B_n	–	–	20.0	ns	1.2	Fig.7
		–	–	6.0		2.7	
		–	3.2*	5.4		3.0 to 3.6	
t_{PHL}/t_{PLH}	propagation delay CP_{BA} to A_n, CP_{AB} to B_n	–	–	20.0	ns	1.2	
		–	–	6.0		2.7	
		–	3.2*	5.4		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_{BA}$ to A_n, OE_{AB} to B_n	–	–	22.0	ns	1.2	Fig.8
		–	–	6.1		2.7	
		–	–	5.5		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time OE_{BA} to A_n, OE_{AB} to B_n	–	–	22.0	ns	1.2	
		–	–	6.1		2.7	
		–	–	5.5		3.0 to 3.6	

SYMBOL	PARAMETER		T_{amb} (°C) −40 to +85 MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS V_{CC} (V)	WAVEFORMS
t_W	LE pulse width, LE_{AB} or LE_{BA} HIGH		–	–	–	ns	1.2	Fig.7
			2.5	–	–		2.7 to 3.6	
	LE pulse width, CP_{AB} or CP_{BA} HIGH or LOW		–	–	–		1.2	
			2.5	–	–		2.7 to 3.6	
t_{su}	set–up time, A_n before CP_{AB} ↓		–	–	–	ns	1.2	Fig.9
			3	–	–		2.7 to 3.6	
	set–up time, B_n before CP_{AB} ↓		–	–	–		1.2	
			3	–	–		2.7 to 3.6	
	set–up time, A_n before LE_{AB} ↓ or B_n before LE_{AB} ↓	CP high	–	–	–		1.2	
			1.5	–	–		2.7 to 3.6	
		CP low	–	–	–		1.2	
			1.5	–	–		2.7 to 3.6	
t_h	hold time, A_n after CP_{AB} ↓ or B_n before CP_{AB} ↓		–	–	–	ns	1.2	
			0	–	–		2.7 to 3.6	
	hold time, A_n after LE_{AB} ↓ or B_n before LE_{BA} ↓		–	–	–		1.2	
			1	–	–		2.7 to 3.6	

Notes: All typical values are measured at T_{amb} = 25 °C.
* Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

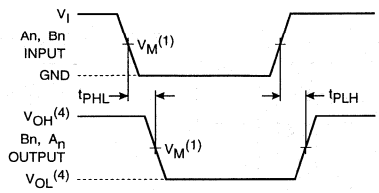


Fig.6 Waveforms showing the input (A_n, B_n) to output (B_n, A_n) propagation delays.

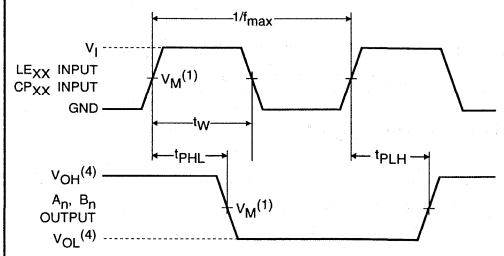


Fig.7 Waveforms showing the latch enable input (E_{AB}, LE_{BA}) and clock pulse input (CP_{AB}, CP_{BA}) to output propagation delays and their pulse width.

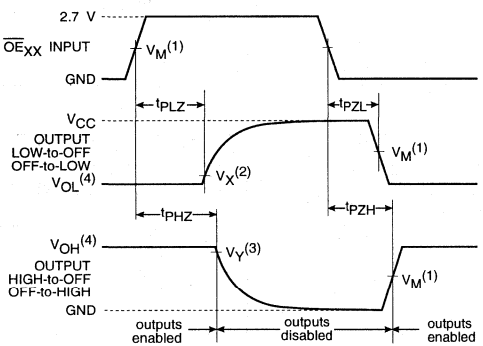


Fig.8 Waveforms showing the 3-state enable and disable times

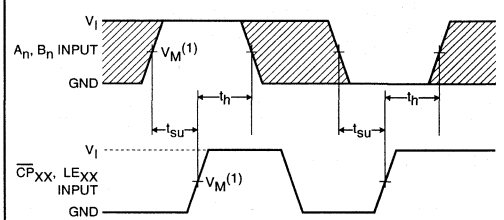
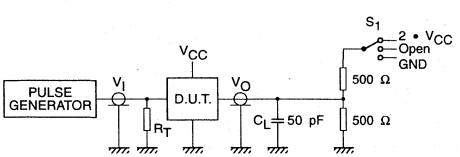


Fig.9 Waveforms showing the data set-up and hold times for the A_n and B_n inputs to the LE_{AB}, LE_{BA}, CP_{AB} and CP_{AB} inputs.
The shaded areas indicate when the input is permitted to change for predictable output performance.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.10 Load circuitry for switching times.

Notes:

(1) V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
$V_M = 0.5 \cdot V_{CC}$ at V_{CC} < 2.7 V

(2) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq$ 2.7 V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at V_{CC} < 2.7 V

(3) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq$ 2.7 V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at V_{CC} < 2.7 V

(4) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **CMOS low power consumption**
- **Multibyte™ pin-out architecture**
- **Direct interface with TTL levels**

DESCRIPTION

The 74ALVC16623 is a high-performance, low-power, low-voltage, Si-gate CMOS device superior to most advanced CMOS compatible TTL families.

The 74ALVC16623 is a dual octal transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions.

This dual octal bus transceiver is designed for asynchronous two-way communication between data buses. The control function implementation allows maximum flexibility in timing. This device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the enable inputs (nOE_{AB}, $n\overline{OE}_{BA}$). The enable inputs can be used to disable the device so that the buses are effectively isolated. The dual enable function configuration gives this transceiver the capability to store data by simultaneous enabling of nOE_{AB} and $n\overline{OE}_{BA}$. Each output reinforces its input in this transceiver configuration. Thus, when all control inputs are enabled and all other data sources to the four sets of the bus lines are at high impedance OFF-state, all sets of bus lines will remain at their last states. The 8-bit codes appearing on the two double sets of buses will be complementary.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n	C_L = 50 pF V_{CC} = 3.3 V	2.7	ns
C_I	input capacitance		3.0	pF
$C_{I/O}$	input/output capacitance		10	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	35	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC16623DL	48	SSOP48	plastic	SSOP48/SOT370
74ALVC16623DGG	48	TSSOP48	plastic	TSSOP48/SOT362

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$1OE_{AB}$	'1' output enable input (active HIGH)
2, 3, 5, 6, 8, 9, 11, 12	$1B_0$ to $1B_7$	'1B' data inputs/outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	ground (0 V)
7, 18, 31, 42	V_{CC}	positive supply voltage
13, 14, 16, 17, 19, 20, 22, 23	$2B_0$ to $2B_7$	'2B' data inputs/outputs
24	$2OE_{AB}$	'2' output enable input (active HIGH)
25	$2\overline{OE}_{BA}$	'2' output enable input (active LOW)
36, 35, 33, 32, 30, 29, 27, 26	$2A_0$ to $2A_7$	'2A' data inputs/outputs
47, 46, 44, 43, 41, 40, 38, 37	$1A_0$ to $1A_7$	'1A' data inputs/outputs
48	$1\overline{OE}_{BA}$	'1' output enable input (active LOW)

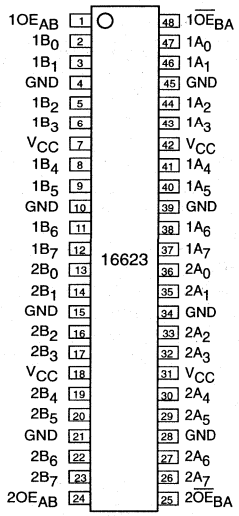


Fig.1 Pin configuration.

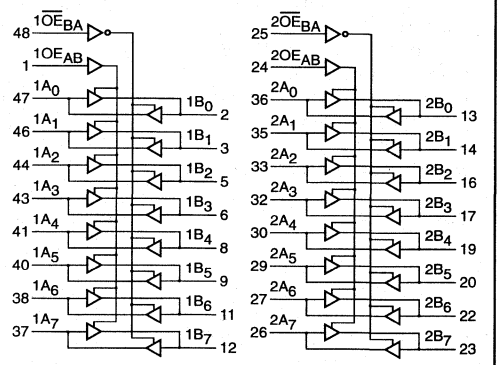


Fig.2 Logic symbol.

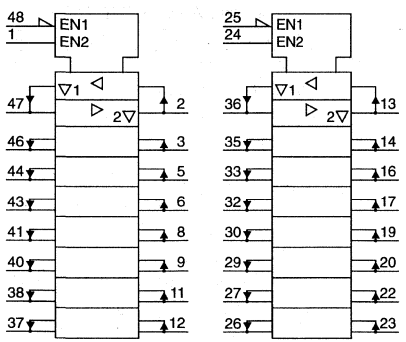


Fig.3 IEC logic symbol.

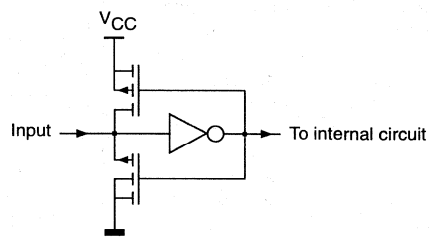


Fig. 4 Bushold circuit

FUNCTION TABLE

ENABLE INPUTS		OPERATION
nOE_{AB}	$n\overline{OE}_{BA}$	
L	L	B data to A bus
H	H	A data to B bus
L	H	Z
H	L	B data to A bus, A data to B bus

H = HIGH voltage level
L = LOW voltage level
Z = high impedance OFF-state

DC CHARACTERISTICS FOR 74ALVC16623

For the DC characteristics see chapter "MBC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74ALVC16623

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C) −40 to +85			UNIT	TEST CONDITIONS	
		MIN.	TYP.	MAX.		V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay nA_n to nB_n; nB_n to nA_n	– 1.5 1.5	15 3.1 2.7*	– 4.2 3.6	ns	1.2 2.7 3.0 to 3.6	Fig. 4
t_{PZH}/t_{PZL}	3-state output enable time nOE_{AB} to nB_n	– 1.5 1.5	* 3.5 3.1*	– 5.5 4.7	ns	1.2 2.7 3.0 to 3.6	Fig. 5
t_{PHZ}/t_{PLZ}	3-state output disable time nOE_{AB} to nB_n	– 1.5 1.5	* 3.3 3.1*	– 6.0 5.0	ns	1.2 2.7 3.0 to 3.6	Fig. 5
t_{PZH}/t_{PZL}	3-state output enable time $n\overline{OE}_{BA}$ to nA_n	– 1.5 1.5	* 3.9 3.4*	– 5.5 4.7	ns	1.2 2.7 3.0 to 3.6	Fig. 5
t_{PHZ}/t_{PLZ}	3-state output disable time $n\overline{OE}_{BA}$ to nA_n	– 1.5 1.5	* 3.0 2.8*	– 6.0 5.0	ns	1.2 2.7 3.0 to 3.6	Fig. 5

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

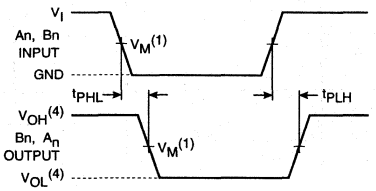


Fig. 4 Waveforms showing the input (nA_n, nB_n) to output (nB_n, nA_n) propagation delay times.

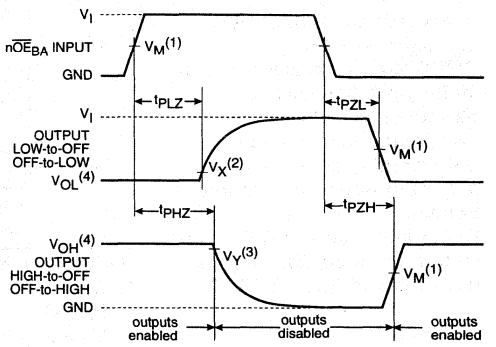


Fig.5 Waveforms showing the 3-state enable and disable times for $n\overline{OE}_{AB}$ input.

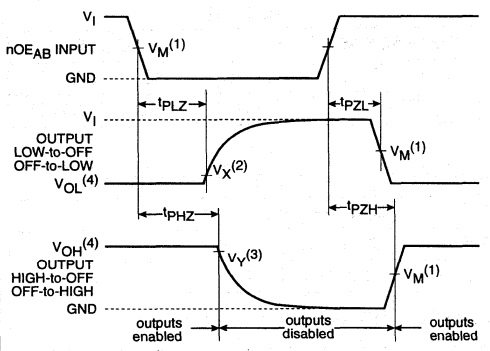
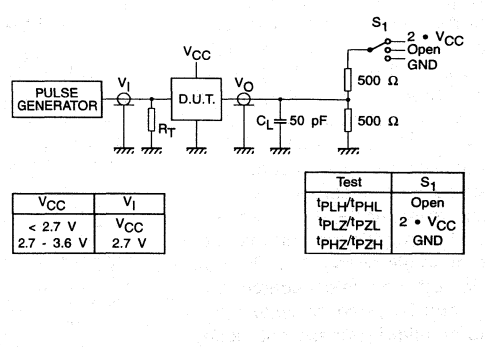


Fig.6 Waveforms showing the 3-state enable and disable times for nOE_{BA} input.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig. 7 Load circuitry for switching times.

Notes:

(1) $V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
$V_M = 1.5$ V at $V_{CC} \geq 2.7$ V

(2) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(3) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.9 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no.8-1A**
- **CMOS low power consumption**
- **Multibyte™ flow-through pin-out architecture**
- **Low inductance, multiple power and ground pins for minimum noise and ground bounce**
- **Direct interface with TTL levels**
- **Output drive capability 50 Ω transmission lines @ 85 °C**

DESCRIPTION

The 74ALVC16646 consist of 16 non-inverting bus transceiver circuits with 3-state outputs, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the internal registers. Data on the 'A' or 'B' bus will be clocked in the internal registers, as the appropiate clock (CP_{AB} or CP_{BA}) goes to a HIGH logic level. Output enable ($\overline{OE}$) and direction (DIR) inputs are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the 'A' or 'B' register, or in both.The select source inputs (S_{AB} and S_{BA}) can multiplex stored and real-time (transparent mode) data. The direction (DIR) input determines which bus will receive data when $\overline{OE}$ is active (LOW). In the isolation mode ($\overline{OE}$ = HIGH), 'A' data may be stored in the 'B' register and/or 'B' data may be stored in the 'A' register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, 'A' or 'B' may be driven at a time.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to B_n, A_n	C_L = 50 pF V_{CC} = 3.3 V	3.2	ns
f_{max}	maximum clock frequency		350	MHz
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	30	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC16646DL	56	SSOP56	plastic	SSOP56/SOT371
74ALVC16646DGG	56	TSSOP56	plastic	TSSOP56/SOT364

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 28	nDIR	Direction control input
2, 27	nCP_{AB}	Clock Input A-to-B
3, 26	nS_{AB}	Select input A-to-B
5, 6, 8, 9, 10, 12, 13, 14	$1A_0$ to $1A_7$	'1A' data inputs/outputs
4, 11, 18, 25, 32, 39, 46, 53	GND	ground (0 V)
7, 22, 35, 50	V_{CC}	positive supply voltage
15, 16, 17, 19, 20, 21, 23, 24	$2B_0$ to $2B_7$	'2B' data inputs/outputs
29, 56	$n\overline{OE}$	Output enable
30, 55	nCP_{BA}	Clock input B-to-A
31, 54	nS_{BA}	Select input B-to-A
42, 41, 40, 38, 37, 36, 34, 33	$2B_0$ to $2B_7$	'2B' data inputs/outputs
52, 51, 49, 48, 47, 45, 44, 43	$1B_0$ to $1B_7$	'1B' data inputs/outputs

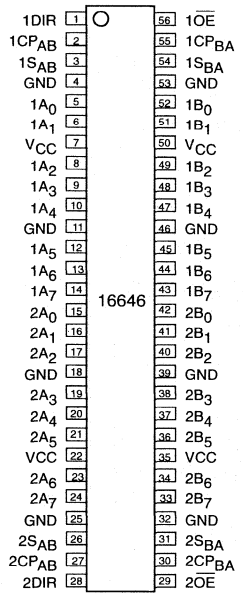


Fig.1 Pin configuration.

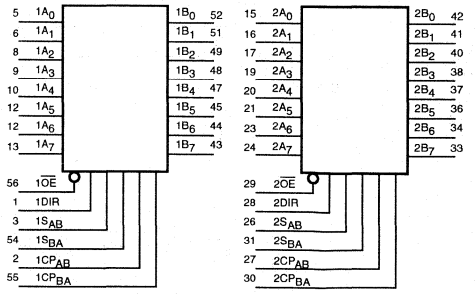


Fig.2 Logic symbol.

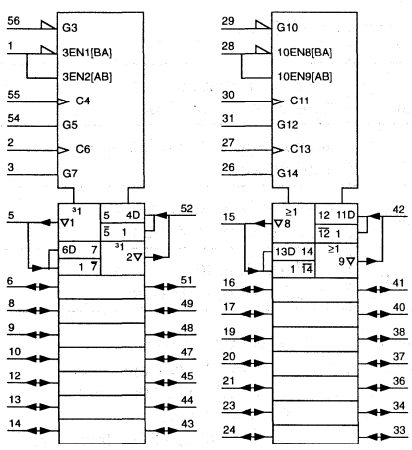


Fig.3 IEC logic symbol.

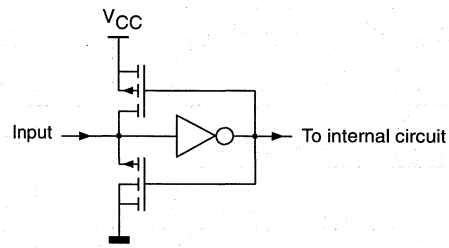


Fig.4 Bushold circuit

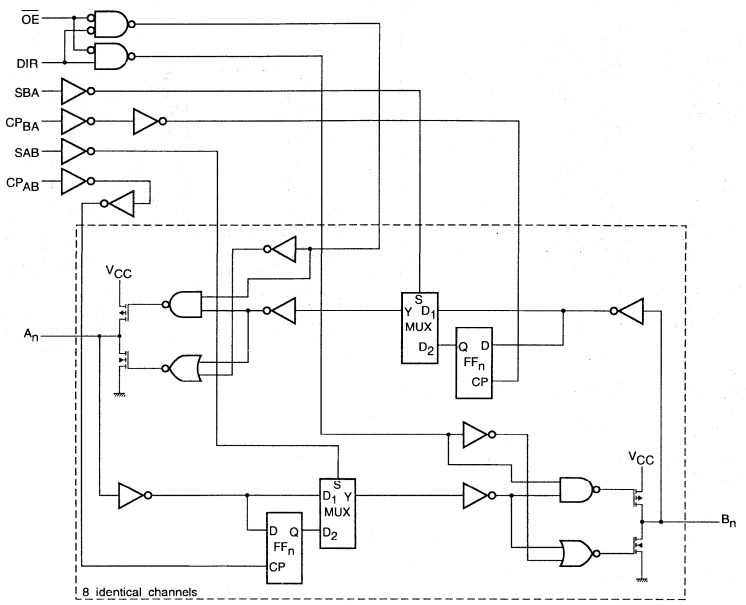


Fig.5 Logic diagram (one section)

FUNCTION TABLE

INPUTS						DATA I/O *		FUNCTION
$\overline{OE}$	DIR	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	A_0 to A_7	B_0 to B_7	
X X	X X	↑ X	X ↑	X X	X X	input un*	un* input	store A, B unspecified* store B, A unspecified*
H H	X X	↑ H or L	↑ H or L	X X	X X	input	input	store A and B data, isolation hold storage
L L	L L	X X	X H or L	X X	L H	output	input	real-time B data to A bus stored B data to A bus
L L	H H	X H or L	X X	L H	X X	input	output	real-time A data to B bus stored A data to B bus

* The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

un = unspecified
H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH level transition

DC CHARACTERISTICS FOR 74ALVC16646

For the DC characteristics see chapter "ALVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74ALVC16646

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C) -40 to +85			UNIT	TEST CONDITIONS	
		MIN.	TYP.	MAX.		V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to B_n, A_n	– – –	– – 3.0*	20.8 5.8 5.2	ns	1.2 2.7 3.0 to 3.6	Fig.6
t_{PHL}/t_{PLH}	propagation delay CP_{AB}, CP_{BA} to B_n, A_n	– – –	– – –	26.4 7.3 6.6	ns	1.2 2.7 3.0 to 3.6	Fig.7
t_{PHL}/t_{PLH}	propagation delay S_{AB}, S_{BA} to B_n, A_n	– – –	– – –	26.8 7.4 6.7	ns	1.2 2.7 3.0 to 3.6	Fig.8
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to A_n, B_n	– – –	– – –	20.7 7.2 6.5	ns	1.2 2.7 3.0 to 3.6	Fig.9
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to A_n, B_n	– – –	– – –	16.7 5.6 5.1	ns	1.2 2.7 3.0 to 3.6	Fig.9
t_{PZH}/t_{PZL}	3-state output enable time DIR to A_n, B_n	– – –	– – –	23.5 7.5 6.8	ns	1.2 2.7 3.0 to 3.6	Fig.10
t_{PHZ}/t_{PLZ}	3-state output disable time DIR to A_n, B_n	– – –	– – –	19.0 6.3 5.7	ns	1.2 2.7 3.0 to 3.6	Fig.10
t_W	clock pulse width HIGH or LOW CP_{AB} or CP_{BA}	3.0 2.5	– –	– –	ns	2.7 3.0 to 3.6	Figs 7 and 8
t_{su}	set–up time A_n, B_n to CP_{AB}, CP_{BA}	– – 0.5	– – –	– – –	ns	1.2 2.7 3.0 to 3.6	Fig.7
t_h	hold time A_n, B_n to CP_{AB}, CP_{BA}	– – 0.5	– – –	– – –	ns	1.2 2.7 3.0 to 3.6	Fig.7
f_{max}	maximum clock pulse frequency	180 200	– –	– –	ns	2.7 3.0 to 3.6	Fig.7

Notes: All typical values are measured at T_{amb} = 25 °C.
* Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

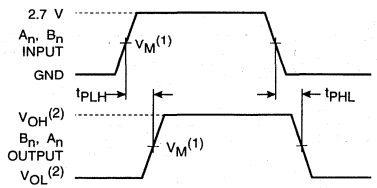


Fig.6 Waveforms showing the input A_n, B_n to output B_n, A_n propagation delay times.

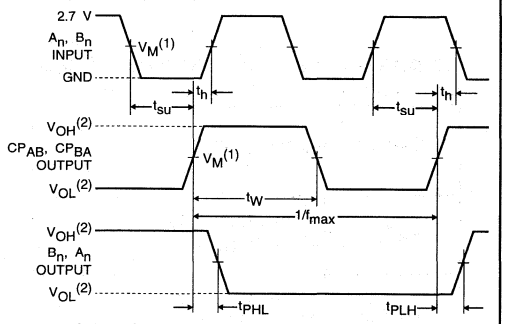


Fig.7 Waveforms showing the A_n, B_n to CPAB, CPBA set-up and hold times, clock CPAB, CPBA pulse width, maximum clock pulse frequency and the CPAB, CPBA to output B_n, A_n propagation delays.

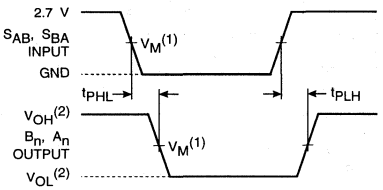


Fig.8 Waveforms showing the input S_{AB}, S_{BA} to output B_n, A_n propagation delay times

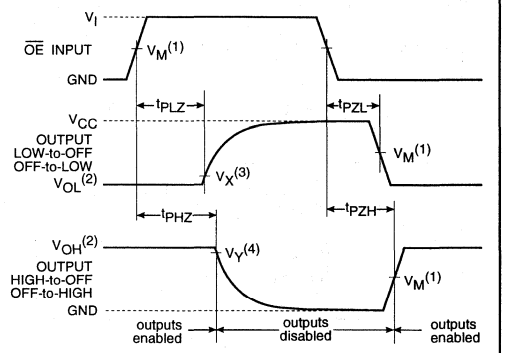


Fig.9 Waveforms showing the input $\overline{OE}$ to output A_n, B_n 3-state enable and disable times.

Notes: (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = 0.9 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

AC WAVEFORMS
(Continued)

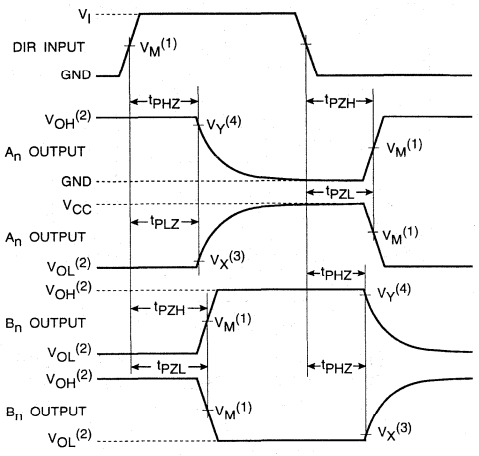
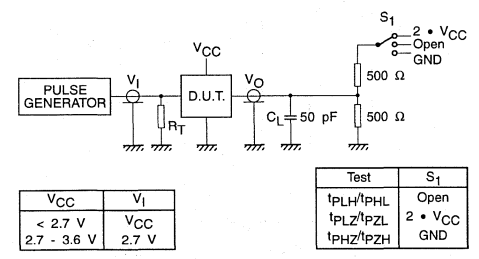


Fig.10 Waveforms showing the input DIR to output A_n, B_n 3-state enable and disable times.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.11 Load circuitry for switching times.

Notes:

(1) V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
$V_M = 0.5 \cdot V_{CC}$ at V_{CC} < 2.7 V

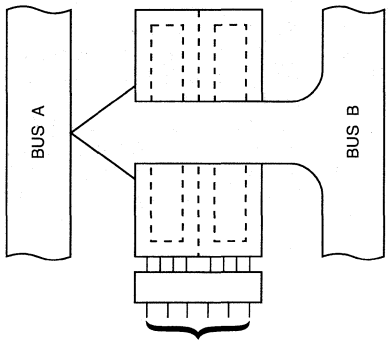
(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

(3) $V_X = V_{OL}$ + 0.3 V at $V_{CC} \geq$ 2.7 V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at V_{CC} < 2.7 V

(4) $V_Y = V_{OH}$ – 0.3 V at $V_{CC} \geq$ 2.7 V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at V_{CC} < 2.7 V

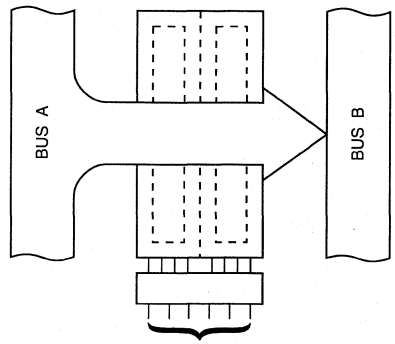
APPLICATION INFORMATION

Real-time transfer; bus B to bus A



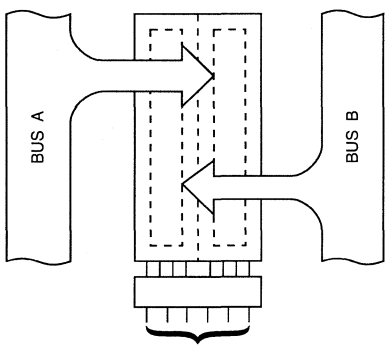
(1) $\overline{OE}$	(14) DIR	(28) CPAB	(16) CPBA	(27) SAB	(15) SBA
L	L	X	X	X	L

Real-time transfer; bus A to bus B



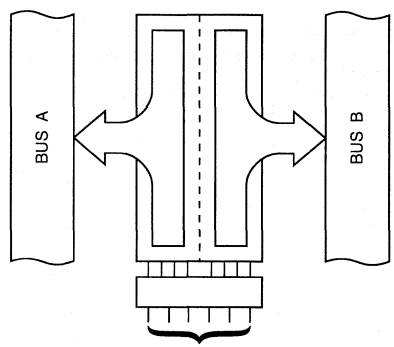
(1) $\overline{OE}$	(14) DIR	(28) CPAB	(16) CPBA	(27) SAB	(15) SBA
L	H	X	X	L	X

Storage from A, B or A and B



(1) $\overline{OE}$	(14) DIR	(28) CPAB	(16) CPBA	(27) SAB	(15) SBA
X	X	↑	X	X	
X	X	X	↑	X	
H	X	↑	↑	X	

Transfer storage data to A or B



(1) $\overline{OE}$	(14) DIR	(28) CPAB	(16) CPBA	(27) SAB	(15) SBA
L	X	H or L	X	H	L
L	H	H or L	X	H	X

16-Bit transceiver/register with dual enable; 3-state 74ALVC16652

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A**
- **CMOS low power consumption**
- **Multibyte™ flow-through pin-out architecture**
- **Low inductance, multiple power and ground pins for minimum noise and ground bounce**
- **Direct interface with TTL levels**
- **Output drive capability 50 Ω transmission lines @ 85 °C**

DESCRIPTION

The 74ALVC16652 consist of 16 non-inverting bus transceiver circuits with 3-state outputs, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Data on the 'A' or 'B' or both buses, will be stored in the internal registers, at the appropiate clock inputs (CP_{AB} or CP_{BA}) regardless of the select inputs (S_{AB} and S_{BA}) or output enable (OE_{AB} and $\overline{OE}_{BA}$) control inputs. Depending on the select inputs S_{AB} and S_{BA} data can directly go from input to output (real time mode) or data can be controlled by the clock (storage mode), this is when the OE inputs permit this operating mode. The output enable inputs OE_{AB} and $\overline{OE}_{BA}$ determine the operation mode of the transceiver. When OE_{AB} is LOW, no data transmission from A_n to B_n is possible and when $\overline{OE}_{BA}$ is HIGH, there is no data transmission from Bn to An possible. When S_{AB} and S_{BA} are in the real time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OE_{AB} and $\overline{OE}_{BA}$. In this configuration each output reinforces its input.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to B_n, A_n	C_L = 50 pF V_{CC} = 3.3 V	3.2	ns
f_{max}	maximum clock frequency		350	MHz
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	30	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC16652DL	56	SSOP56	plastic	SSOP56/SOT371
74ALVC16652DGG	56	TSSOP56	plastic	TSSOP56/SOT364

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 28	nOE_{AB}	Output enable A-to-B
2, 27	nCP_{AB}	Clock Input A-to-B
3, 26	nS_{AB}	Select input A-to-B
5, 6, 8, 9, 10, 12, 13, 14	$1A_0$ to $1A_7$	'1A' data inputs/outputs
4, 11, 18, 25, 32, 39, 46, 53	GND	ground (0 V)
7, 22, 35, 50	V_{CC}	positive supply voltage
15, 16, 17, 19, 20, 21, 23, 24	$2B_0$ to $2B_7$	'2B' data inputs/outputs
29, 56	$n\overline{OE}_{BA}$	Output enable B-to-A
30, 55	nCP_{BA}	Clock input B-to-A
31, 54	nS_{BA}	Select input B-to-A
42, 41, 40, 38, 37, 36, 34, 33	$2B_0$ to $2B_7$	'2B' data inputs/outputs
52, 51, 49, 48, 47, 45, 44, 43	$1B_0$ to $1B_7$	'1B' data inputs/outputs

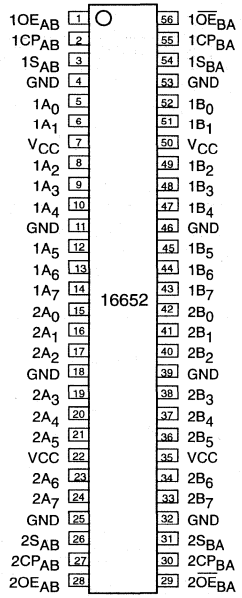


Fig.1 Pin configuration.

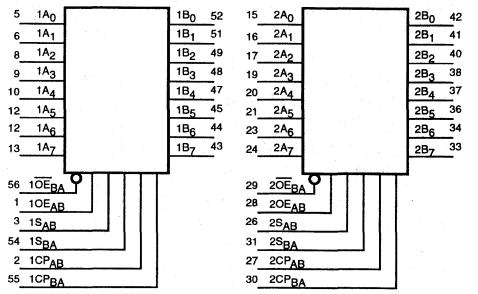


Fig.2 Logic symbol.

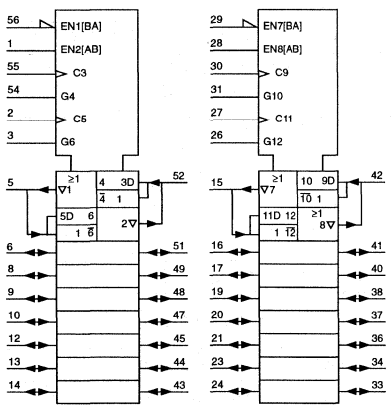


Fig.3 IEC Logic symbol

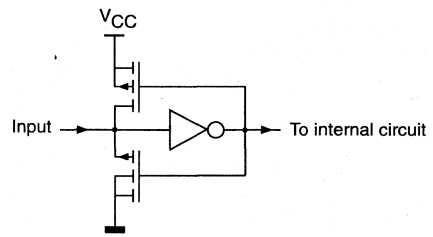


Fig.4 Bushold circuit.

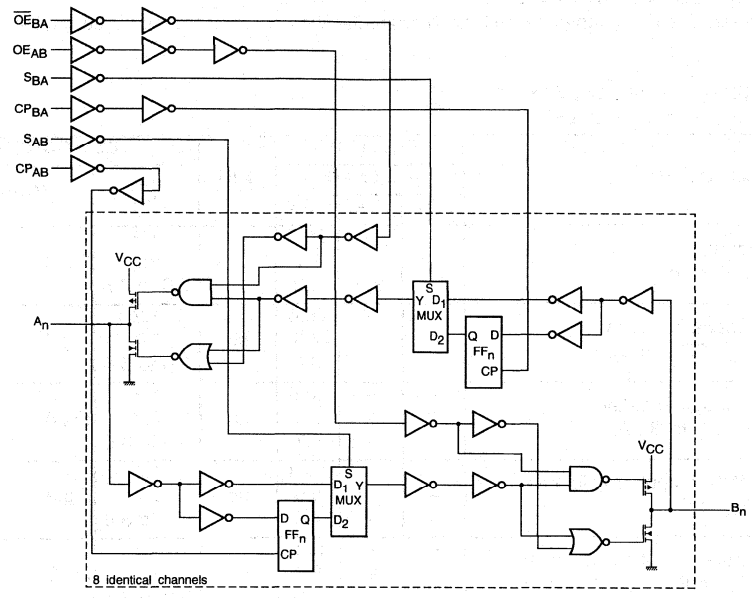


Fig.5 Logic diagram (one section).

FUNCTION TABLE

INPUTS						DATA I/O *		FUNCTION
OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	A_0 to A_7	B_0 to B_7	
L L	H H	H or L ↑	H or L ↑	X X	X X	input	input	isolation store A and B data
X H	H H	↑ ↑	H or L ↑	X L	X X	input input	un* output	store A, hold B store A in both registers
L L	X L	H or L ↑	↑ ↑	X X	X L	un* output	input input	hold A, store B store B in both registers
L L	L L	X X	X H or L	X X	L H	output	input	real time B data to A bus stored B data to A bus
H H	H H	X H or L	X X	L H	X X	input	output	real-time A data to B bus stored A data to B bus
H	L	H or L	H or L	H	H	output	output	stored A data to B bus and stored B data to A bus

* The data output functions may be enabled or disabled by various signals at the OE_{AB} and $\overline{OE}_{BA}$ inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

un = unspecified
H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH level transition

DC CHARACTERISTICS FOR 74ALVC16652

For the DC characteristics see chapter "ALVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74ALVC16652

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		–40 to +85				V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to B_n, A_n	–	–	20.8	ns	1.2	Fig.6
		–	–	5.7		2.7	
		–	3.0*	5.2		3.0 to 3.6	
t_{PHL}/t_{PLH}	propagation delay CP_{AB}, CP_{BA} to B_n, A_n	–	–	26.4	ns	1.2	Fig.7
		–	–	7.3		2.7	
		–	–	6.6		3.0 to 3.6	
t_{PHL}/t_{PLH}	propagation delay S_{AB}, S_{BA} to B_n, A_n	–	–	26.8	ns	1.2	Fig.8
		–	–	7.4		2.7	
		–	–	6.7		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time OE_{AB} to B_n	–	–	14.3	ns	1.2	Fig.9
		–	–	5.0		2.7	
		–	–	4.5		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time OE_{AB} to B_n	–	–	15.5	ns	1.2	Fig.9
		–	–	5.3		2.7	
		–	–	4.8		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_{BA}$ to A_n	–	–	13.5	ns	1.2	Fig.9
		–	–	4.8		2.7	
		–	–	4.3		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_{BA}$ to A_n	–	–	13.9	ns	1.2	Fig.9
		–	–	4.8		2.7	
		–	–	4.3		3.0 to 3.6	
t_W	clock pulse width HIGH or LOW CP_{AB} or CP_{BA}	–	–	–	ns	2.7	Fig.7
		2.5	–	–		3.0 to 3.6	
t_{su}	set–up time A_n, B_n to CP_{AB}, CP_{BA}	–	–	–	ns	1.2	Fig.7
		–	–	–		2.7	
		0.9	–	–		3.0 to 3.6	
t_h	hold time A_n, B_n to CP_{AB}, CP_{BA}	–	–	–	ns	1.2	Fig.7
		–	–	–		2.7	
		0.9	–	–		3.0 to 3.6	
f_{max}	maximum clock pulse frequency	180	–	–	MHz	2.7	Fig.7
		200	–	–		3.0 to 3.6	

Notes: All typical values are measured at T_{amb} = 25 °C.
* Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

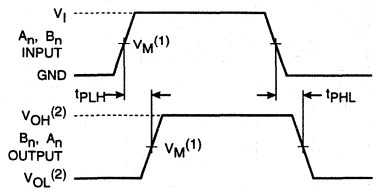


Fig.6 Waveforms showing the input A_n, B_n to output B_n, A_n propagation delay times.

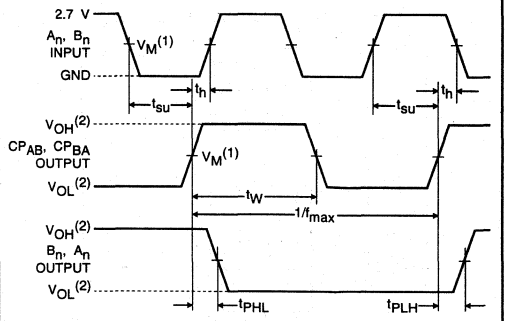


Fig.7 Waveforms showing the A_n, B_n to CP_{AB}, CP_{BA} set-up and hold times, clock CP_{AB}, CP_{BA} pulse width, maximum clock pulse frequency and the CP_{AB}, CP_{BA} to output B_n, A_n propagation delays.

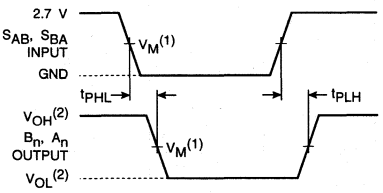


Fig.8 Waveforms showing the input S_{AB}, S_{BA} to output B_n, A_n propagation delay times.

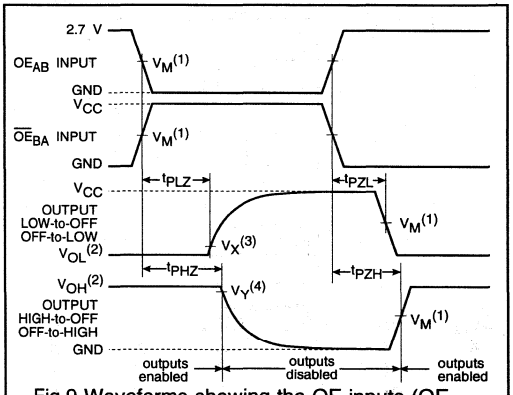
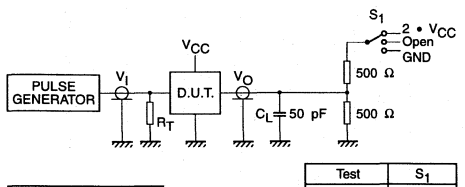


Fig.9 Waveforms showing the OE inputs (OE_{AB}, $\overline{OE}_{BA}$) to outputs A_n, B_n enable and disable times and the input rise and fall times.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.10 Load circuitry for switching times.

Notes:

(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

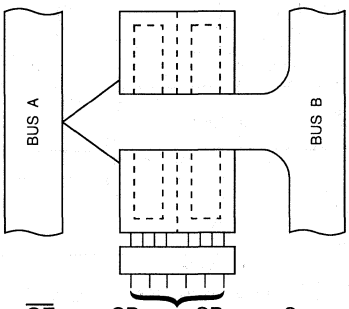
(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

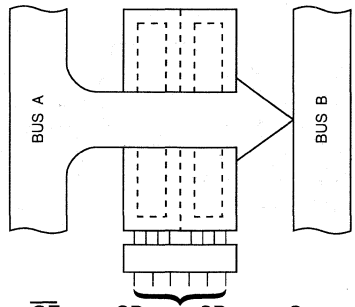
APPLICATION INFORMATION

Real-time transfer; bus B to bus A



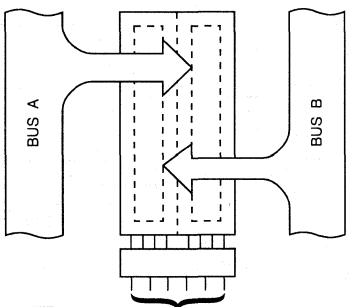
OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
L	L	X	X	X	L

Real-time transfer; bus A to bus B



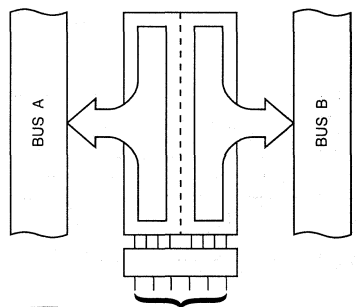
OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
H	H	X	X	L	X

Store A, B or A and B in one register



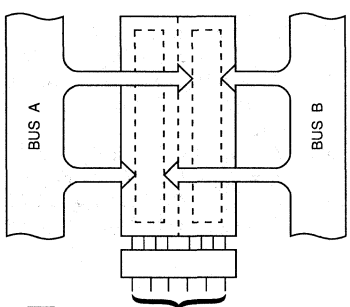
OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

Transfer A stored data to B bus or B stored data to A bus or both at the same time



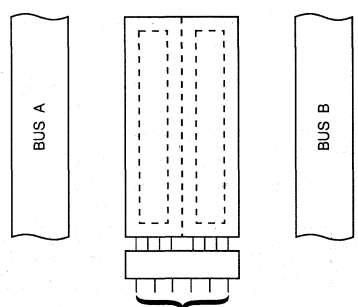
OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
H	H	H or L	X	H	X
L	L	X	H or L	X	H
H	L	H or L	H or L	H	H

Store bus A in both registers or store bus B in both registers



OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
H	H	↑	↑	L	X
L	L	↑	↑	X	L

Isolation



OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
L	H	H or L	H or L	X	X

16-Bit registered transceiver; 3-state | 74ALVC16952

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A**
- **CMOS low power consumption**
- **Multibyte™ flow-through pin-out architecture**
- **Low inductance, multiple centre power and ground pins for minimum noise and ground bounce**
- **Direct interface with TTL levels**
- **Output drive capability 50 Ω transmission lines @ 85 °C**

DESCRIPTION

The 74ALVC16952 is a high-performance, low-power, low-voltage, Si-gate CMOS device superior to most advanced CMOS compatible TTL families.

The 74ALVC16952 consists of two section each containing a dual octal non-inverting registered transceiver. Two 8-bit back to back registers store data flowing in both directions between two bi-directional busses. Data applied to the inputs is entered and stored on the rising edge of the clock (CP_{XX}, where X is AB or BA) provided that the clock enable ($\overline{CE}_{XX}$) is LOW. The data is then present at the 3-state output buffers, but is only accessible when the output enable input ($\overline{OE}_{XX}$) is LOW. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay CP_{nn} to A_n, B_n	C_L = 50 pF; V_{CC} = 3.3 V	3.2	ns
f_{max}	maximum clock frequency		350	MHz
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	30	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC16952DL	56	SSOP56	plastic	SSOP56/SOT371
74ALVC16952DGG	56	TSSOP56	plastic	TSSOP56/SOT364

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 28	$n\overline{OE}_{AB}$	Output enable A-to-B
2, 27	nCPAB	Clock input A-to-B
3, 26	$n\overline{CE}_{AB}$	A-to-B enable
5, 6, 8, 9, 10, 12, 13, 14	$1A_0$ to $1A_7$	'1A' data inputs/outputs
4, 11, 18, 25, 32, 39, 46, 53	GND	ground (0 V)
7, 22, 35, 50	V_{CC}	positive supply voltage
15, 16, 17, 19, 20, 21, 23, 24	$2B_0$ to $2B_7$	'2B' data inputs/outputs
29, 56	$n\overline{OE}_{BA}$	Output enable B-to-A
30, 55	nCP_{BA}	Clock input B-to-A
31, 54	$n\overline{CE}_{BA}$	B-to-A enable
42, 41, 40, 38, 37, 36, 34, 33	$2B_0$ to $2B_7$	'2B' data inputs/outputs
52, 51, 49, 48, 47, 45, 44, 43	$1B_0$ to $1B_7$	'1B' data inputs/outputs

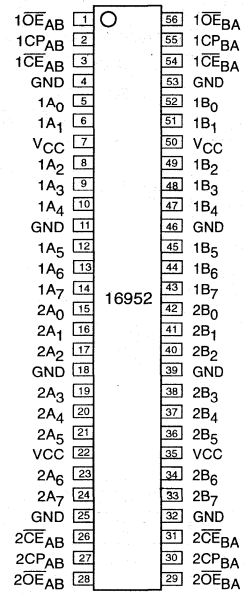


Fig.1 Pin configuration.

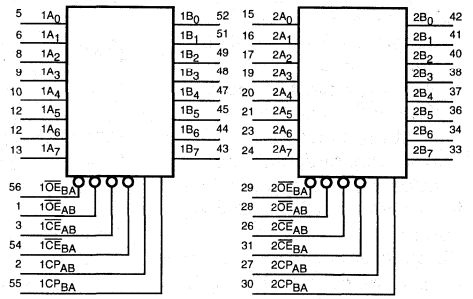


Fig.2 Logic symbol.

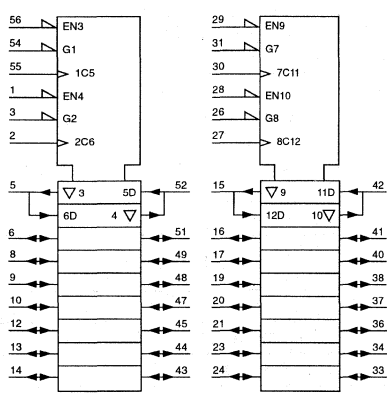


Fig.3 IEC logic symbol.

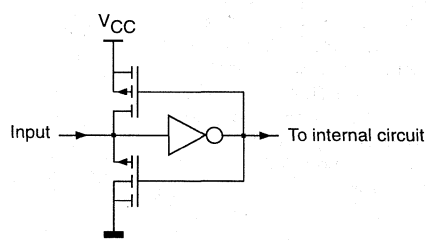


Fig.4 Bushold circuit.

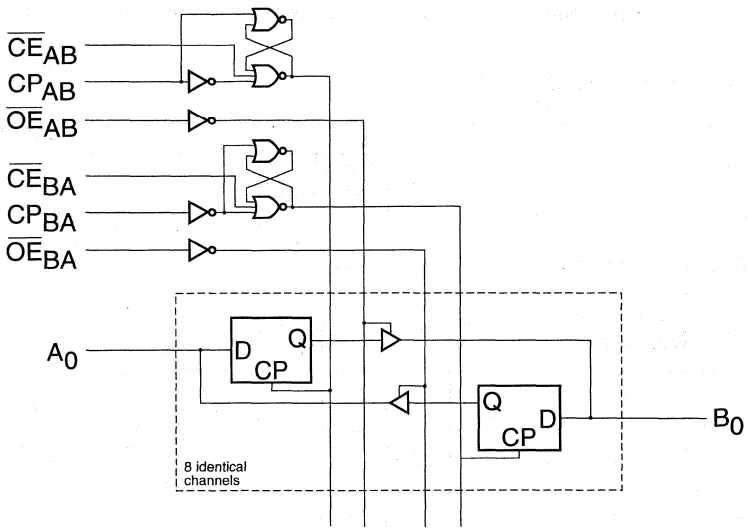


Fig.5 Logic diagram (one section)

FUNCTION TABLE for register A_n or B_n

INPUTS			INTERNAL Q	OPERATIN G MODE
A_n or B_n	CP_{xx}	$\overline{CE}_{xx}$		
X	X	H	NC	Hold data
L	↑	L	L	Load data
H	↑	L	H	Load data

H = HIGH voltage level
L = LOW voltage level
↑ = Low-to-High transition

FUNCTION TABLE for output enable

INPUTS	INTERNAL Q	A_n or B_n OUTPUTS	OPERATING MODE
$\overline{OE}_{xx}$			
H	X	Z	disable outputs
L	L	L	enable outputs
L	H	H	enable outputs

NC = no change
X = don't care
Z = high impedance OFF-state

DC CHARACTERISTICS FOR 74ALVC16952

For the DC characteristics see chapter "ALVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74ALVC16952

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		−40 to +85				V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t_{PHL}/t_{PLH}	propagation delay CP_{BA}, CP_{AB} to A_n, B_n	– – –	– – 3.2*	– 7.5 6.8	ns	1.2 2.7 3.0 to 3.6	Fig.6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_{BA}$, $\overline{OE}_{AB}$ to A_n, B_n	– – –	– – –	– 7.5 6.6	ns	1.2 2.7 3.0 to 3.6	Fig.8
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_{BA}$, $\overline{OE}_{AB}$ to A_n, B_n	– – –	– – –	– 7.5 6.6	ns	1.2 2.7 3.0 to 3.6	Fig.8
t_W	CP_{AB}, CP_{BA} pulse width, HIGH or LOW	2.0 1.6	– –	– –	ns	2.7 3.0 to 3.6	Fig.6
t_{su}	set–up time, HIGH or LOW A_n, B_n to CP_{AB}, CP_{BA}	−0.7 −0.6	– –	– –	ns	2.7 3.0 to 3.6	Fig.7
t_{su}	set–up time, HIGH or LOW $\overline{CE}_{AB}$, $\overline{CE}_{BA}$ to CP_{AB}, CP_{BA}	1.8 1.5	– –	– –	ns	2.7 3.0 to 3.6	Fig.7
t_h	hold time A_n, B_n to CP_{AB}, CP_{BA}	0.9 0.7	– –	– –	ns	2.7 3.0 to 3.6	Fig.7
t_h	hold time $\overline{CE}_{AB}$, $\overline{CE}_{BA}$ to CP_{AB}, CP_{BA}	1.5 1.3	– –	– –	ns	2.7 3.0 to 3.6	Fig.7
f_{max}	maximum clock pulse frequency	140 200	– –	– –	MHz	2.7 3.0 to 3.6	Fig.7

Notes: All typical values are measured at T_{amb} = 25 °C.
* Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

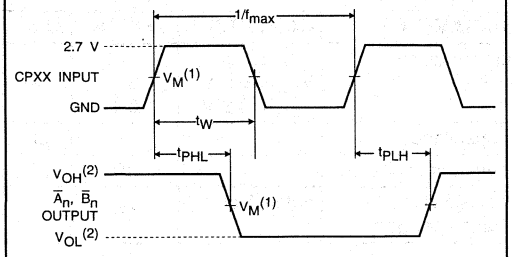


Fig.6 Waveforms showing the clock input (CP_{BA}, CP_{AB}) to output ($\overline{B}_n$, $\overline{A}_n$) propagation delays, the clock pulse width and the maximum clock pulse frequency.

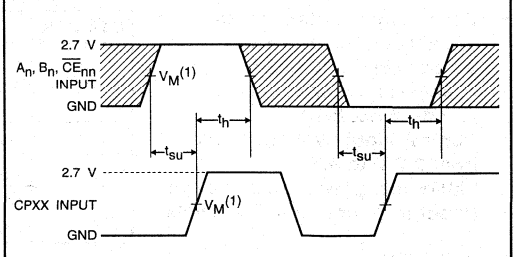


Fig.7 Waveforms showing the set-up and hold times for the A_n, B_n and $\overline{CE}_{XX}$ inputs.
The shaded areas indicate when the input is permitted to change for predictable output performance.

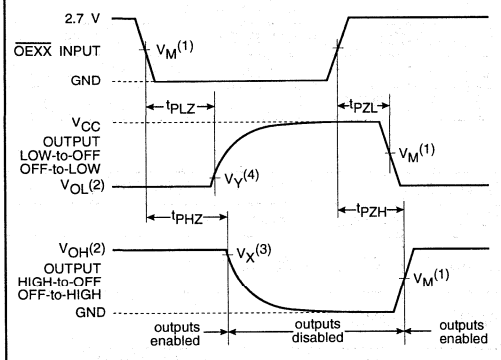
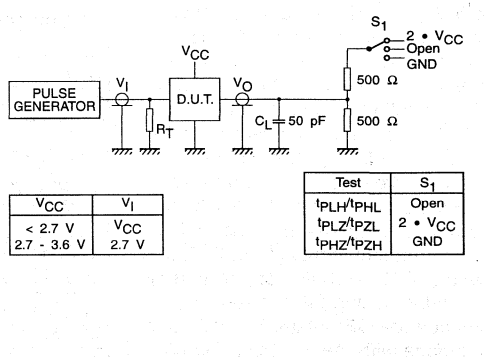


Fig.8 Waveforms showing the 3-state enable and disable times.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.9 Load circuitry for switching times.

Notes:

(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

16-bit dual supply translating transceiver; 3-state 74ALVC164245

FEATURES

- **Wide supply voltage range**
  3 Volt port: 1.2 to 3.6 V
  5 Volt port: 1.2 to 5.5 V
- **In accordance with JEDEC standard no. 8-1A.**
- **Control inputs voltage range from 2.7 V to 5.5 V**
- **CMOS low power consumption**
- **Direct interface with TTL levels**

DESCRIPTION

The 74ALVC164245 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families. The 74ALVC164245 is a 16-bit (dual-octal) translating transceiver and is designed to interface between a 5 V bus and 3 V bus in a mixed 3 V/5 V supply environment. This device can be used as two 8-bit transceivers or one 16-bit transceiver. The direction control inputs (1DIR, 2DIR) determine the direction of the data flow. nDIR (active HIGH) enables data from nA ports to nB ports. nDIR (active LOW) enables data from nB ports to nA ports.The output enable inputs ($1\overline{OE}$, $2\overline{OE}$), when HIGH, disable both nA and nB ports by placing them in a high impedance OFF-state. The nB ports interface with the 5 V bus; The nA ports interfaces with the 3 V bus. In suspend mode, when one of the supply voltages is zero, there will be no current flow from the non zero supply towards the zero supply. $V_{CC1} \geq V_{CC2}$ (except in suspend mode)

FUNCTION TABLE

INPUTS		OUTPUTS	
$n\overline{OE}$	nDIR	nA_n	nB_n
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA to nB nB to nA	C_L = 50 pF V_{CC1} = 5.0 V V_{CC2} = 3.3 V	 3.7 3.1	ns
C_I	input capacitance		5	pF
$C_{I/O}$	input/output capacitance		10	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	20	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC164245DL	48	SSOP	plastic	SSOP48/SOT370
74ALVC164245DGG	48	TSSOP	plastic	TSSOP48/SOT362

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	1DIR	'1' direction control
2, 3, 5, 6, 8, 9, 11, 12	$1B_0$ to $1B_7$	'1B' data inputs/outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	GND
7, 18	V_{CC1}	positive supply voltage (5 V bus)
13, 14, 16, 17, 19, 20, 22, 23	$2B_0$ to $2B_7$	'2B' data inputs/outputs
24	2DIR	'2B' direction control
25	$2\overline{OE}$	'2' output enable input (active LOW)
26, 27, 29, 30, 32, 33, 35, 36	$2A_7$ to $2A_0$	'2A' data inputs/outputs
31, 42	V_{CC2}	positive supply voltage (3 V bus)
37, 38, 40, 41, 43, 44, 46, 47	$1A_7$ to $1A_0$	'1A' data inputs/outputs
48	$1\overline{OE}$	'1' output enable input (active LOW)

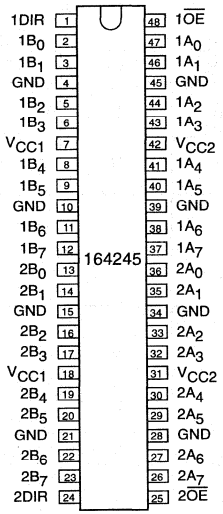


Fig.1 Pin configuration.

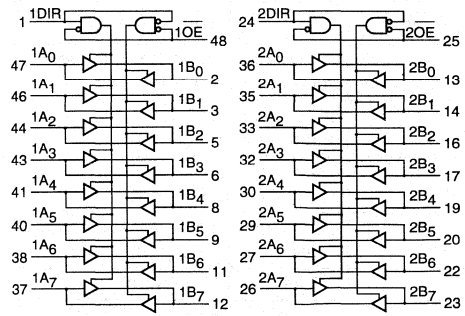


Fig.2 Logic symbol.

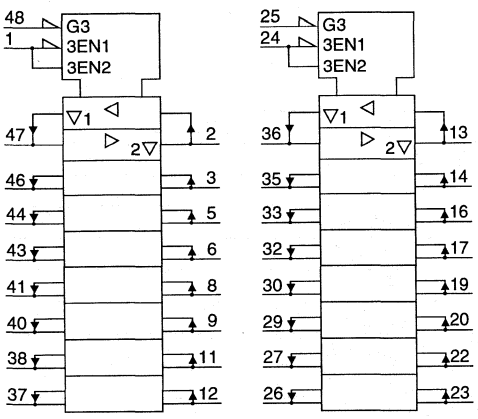


Fig.3 IEC Logic symbol.

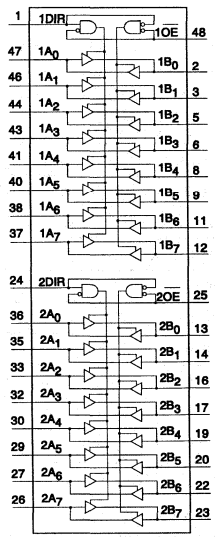


Fig. 4 Functional diagram

FAMILY DESCRIPTION

RECOMMENDED OPERATING CONDITIONS FOR THE ALVC FAMILY

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC1}	DC supply voltage (for max. speed performance) (5 V port)	2.7	5.5	V	$V_{CC1} \geq V_{CC2}$
V_{CC2}	DC supply voltage (for max. speed performance) (3 V port)	2.7	3.6	V	$V_{CC1} \geq V_{CC2}$
V_{CC1}	DC supply voltage (for low-voltage applications) (5 V port)	1.2	5.5	V	$V_{CC1} \geq V_{CC2}$
V_{CC2}	DC supply voltage (for low-voltage applications) (3 V port)	1.2	3.6	V	$V_{CC1} \geq V_{CC2}$
V_I	DC input voltage range	0	5.5	V	
$V_{I/O}$	DC input voltage range for I/Os	0	V_{CC2}	V	3V port
$V_{I/O}$	DC input voltage range for I/Os	0	V_{CC1}	V	5V port
V_O	DC output voltage range	0	V_{CC2}	V	3V port
V_O	DC output voltage range	0	V_{CC1}	V	5V port
T_{amb}	operating ambient temperature range in free air	−40	+85	°C	see DC and AC characteristics per device
t_r, t_f	input rise and fall times	0 0 0	50 20 10	ns/V	V_{CC} = 1.2 to 2.0 V V_{CC} = 2.7 to 3.0 V V_{CC} = 3.0 to 5.5 V

LIMITING VALUES FOR THE ALVC FAMILY

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC1}	DC supply voltage (5 V port)	−0.5	+6.0	V	
V_{CC2}	DC supply voltage (3 V port)	−0.5	+4.6	V	
I_{IK}	DC input diode current	–	−50	mA	$V_I < 0$
V_I	DC input voltage	−0.5	+5.5	V	note 2
$V_{I/O}$	DC input voltage range for I/Os	−0.5	V_{CC} + 0.5	V	
I_{OK}	DC output diode current	–	±50	mA	$V_O > V_{CC}$ or $V_O < 0$
V_O	DC output voltage	−0.5	V_{CC} + 0.5	V	note 2
I_O	DC output source or sink current	–	±50	mA	V_O = 0 to V_{CC}
I_{GND}, I_{CC}	DC V_{CC} or GND current	–	±100	mA	
T_{stg}	storage temperature range	−60	+150	°C	
P_{tot}	power dissipation per package				See chapter 1, "Thermal data"

Notes to the limiting values

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operating of the device at these or any other conditions beyond those under 'recommended operating conditions' is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS FOR THE ALVC FAMILY

Over recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C) −40 to +85			UNIT	TEST CONDITIONS		
		MIN.	TYP.	MAX.		V_{CC} (V)	V_I	OTHER
V_{IH}	HIGH level input voltage (5 V port)	2.0	–	–	V	4.5 to 5.5		
V_{IH}	HIGH level input voltage (3 V port)	2.0	–	–	V	2.7 to 3.6		
V_{IL}	LOW level input voltage (5 V port)	–	–	0.8	V	4.5 to 5.5		
V_{IL}	LOW level input voltage (3 V port)	–	–	0.8	V	2.7 to 3.6		
V_{OH}	HIGH level output voltage (5 V port)	V_{CC} − 0.2 V_{CC} − 0.8	V_{CC} –	– –	V	4.5 4.5	V_{IH} or V_{IL}	I_O = −100 µA I_O = −24 mA
V_{OH}	HIGH level output voltage (3 V port)	V_{CC} − 0.6 V_{CC} − 0.2 V_{CC} − 1.0	– V_{CC} –	– – –	V	2.7 3.0 3.0	V_{IH} or V_{IL}	I_O = −12 mA I_O = −100 µA I_O = −24 mA
V_{OL}	LOW level output voltage (5 V port)	– – –	– – –	0.20 0.40 0.55	V	4.5 4.5 4.5	V_{IH} or V_{IL}	I_O = 100 µA I_O = 12 mA I_O = 24 mA
V_{OL}	LOW level output voltage (3 V port)	– – –	– – –	0.40 0.20 0.55	V	2.7 3.0 3.0	V_{IH} or V_{IL}	I_O = 12 mA I_O = 100 µA I_O = 24 mA
I_I	input leakage current	–	±0.1	±5	µA	3.6	5.5 V or GND	not for I/O pins
I_{IHZ}/I_{ILZ}	input current for common I/O pins (5 V port)	–	±0.1	±15	µA	5.5	V_{CC} or GND	
I_{IHZ}/I_{ILZ}	input current for common I/O pins (3 V port)	–	±0.1	±15	µA	3.6	V_{CC} or GND	
I_{OZ}	3-state output OFF-state current (5 V port)	–	0.1	±10	µA	5.5	V_{IH} or V_{IL}	V_O = V_{CC} or GND
I_{OZ}	3-state output OFF-state current (3 V port)	–	0.1	±10	µA	3.6	V_{IH} or V_{IL}	V_O = V_{CC} or GND
I_{CC}	quiescent supply current (5 V port)	–	0.2	40	µA	5.5	V_{CC} or GND	I_O = 0
I_{CC}	quiescent supply current (3 V port)	–	0.2	40	µA	3.6	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current given per input pin (5 V port)	–	5	500	µA	4.5 to 5.5	V_{CC} − 2.1 V	I_O = 0
ΔI_{CC}	additional quiescent supply current given per input pin (3 V port)	–	5	500	µA	2.7 to 3.6	V_{CC} − 0.6 V	I_O = 0

Note: All typical values are measured at V_{CC1} = 5.0 V, V_{CC2} = 3.3 V and T_{amb} = 25 °C.

DC CHARACTERISTICS FOR 74ALVC164245

For the DC characteristics see chapter "ALVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74ALVC164245

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C) −40 to +85			UNIT	TEST CONDITIONS		
		MIN.	TYP.	MAX.		V_{CC1} (V)	V_{CC2} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay nA_n to nB_n	–	4.0	5.6	ns	4.5 to 5.5	2.7	Fig. 5
		–	3.7	5.6		4.5 to 5.5	3.0 to 3.6	
t_{PHL}/t_{PLH}	propagation delay nB_n to nA_n	–	3.1	5.0	ns	4.5 to 5.5	2.7	Fig. 5
		–	3.1	4.3		4.5 to 5.5	3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time $n\overline{OE}$ to nA_n	–	6.3	9.0	ns	4.5 to 5.5	2.7	Figs 6, 7
		–	5.0	7.7		4.5 to 5.5	3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time $n\overline{OE}$ to nB_n	–	5.2	7.5	ns	4.5 to 5.5	2.7	Figs 6, 7
		–	4.7	7.2		4.5 to 5.5	3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time $n\overline{OE}$ to nA_n	–	5.0	6.8	ns	4.5 to 5.5	2.7	Figs 6, 7
		–	5.0	6.6		4.5 to 5.5	3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time $n\overline{OE}$ to nB_n	–	5.2	7.2	ns	4.5 to 5.5	2.7	Figs 6, 7
		–	5.4	7.3		4.5 to 5.5	3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.

* Typical values are measured at $V_{CC1} = 5.0$ V and $V_{CC2} = 3.3$ V.

AC WAVEFORMS

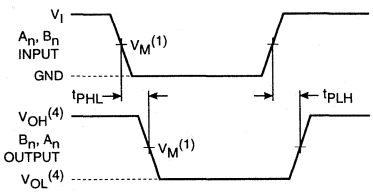


Fig. 5 Waveforms showing the input (nA_n, nB_n) to output (nB_n, nA_n) propagation delays.

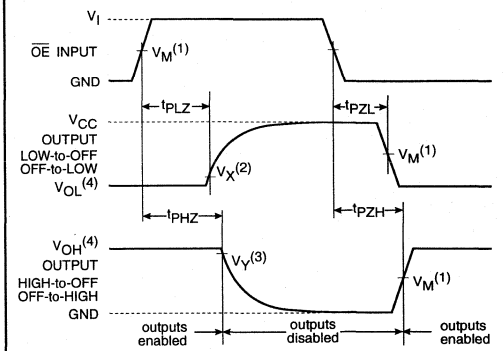
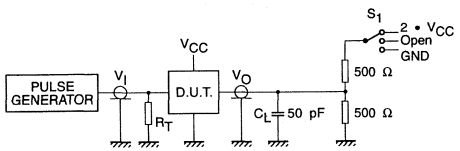


Fig.6 Waveforms showing the 3-state enable and disable times.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.7 Load circuitry for switching times.

Notes:

(1) $V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
$V_M = 1.5$ V at $V_{CC} \geq 2.7$ V

(2) $V_X = V_{OL} + 0.3$ V at
$V_{CC} \geq 2.7$ V & $V_{CC} \leq 3.6$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at
$V_{CC} < 2.7$ V & $V_{CC} > 3.6$ V

(3) $V_Y = V_{OH} - 0.3$ V at
$V_{CC} \geq 2.7$ V & $V_{CC} \leq 3.6$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at
$V_{CC} < 2.7$ V & $V_{CC} > 3.6$ V

(4) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

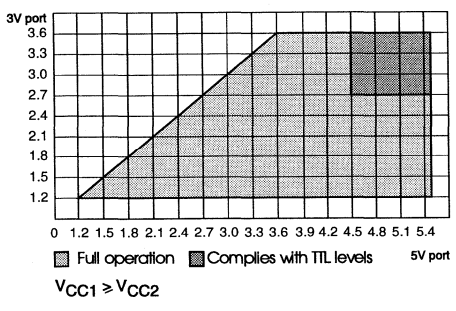


Fig.8 Supply operating area.

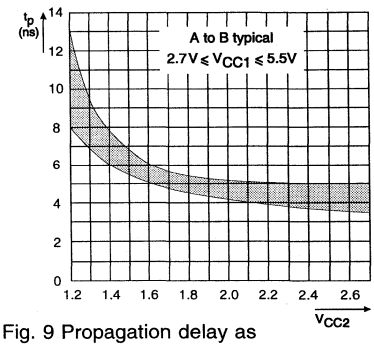


Fig. 9 Propagation delay as a function of the supply voltage V_{CC2}.

DEVICE DATA

LVT

3.3V ABT Quad buffer (3-State) 74LVT125

FEATURES

- Quad bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Power-up 3-State
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT125 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device combines low static and dynamic power dissipation with high speed and high output drive.

The 74LVT125 device is a quad buffer that is ideal for driving bus lines. The device features four Output Enables ($\overline{OE}0$, $\overline{OE}1$, $\overline{OE}2$, $\overline{OE}3$), each controlling one of the 3-State outputs.

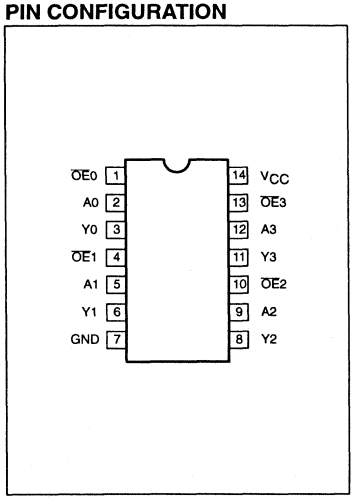
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Yn	C_L = 50pF; V_{CC} = 3.3V	2.9	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or 3.0V	8	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	0.13	mA

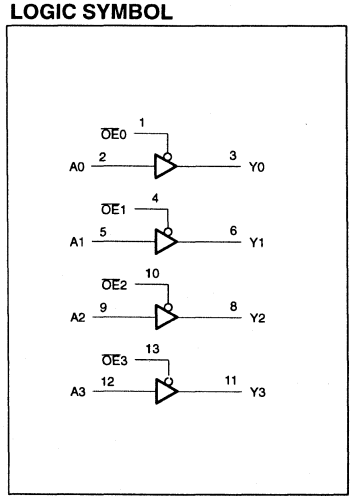
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
14-Pin Plastic Small Outline Package (SO)	–40°C to +85°C	74LVT125D	SOT108-1

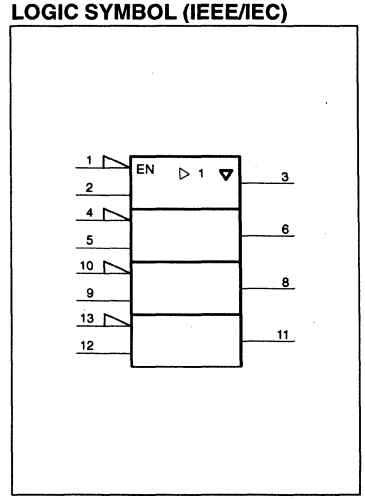
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 5, 9, 12	A0 – A3	Data inputs
3, 6, 8, 11	Y0 – Y3	Data outputs
1, 4, 10, 13	$\overline{OE}0$ – $\overline{OE}3$	Output enables
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

FUNCTION TABLE (EACH BUFFER)

INPUTS		OUTPUTS
$\overline{OE}n$	An	Yn
L	L	L
L	H	H
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "Off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
V_I	DC input voltage[3]		–0.5 to +7.0	V
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Out in High State	–64	mA
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%, f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = −18mA			−0.9	−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = −100µA		V_{CC}-0.2	V_{CC}-0.1		V
		V_{CC} = 2.7V; I_{OH} = −8mA		2.4	2.5		
		V_{CC} = 3.0V; I_{OH} = −32mA		2.0	2.2		
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.1	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
I_I	Input leakage current	V_{CC} = 0 or 3.6V; V_I = 5.5V	All inputs		1	10	µA
		V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		±0.1	±1	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 3.6V; V_I = 0			−1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			1	±100	µA
I_{HOLD}	Bus Hold current A inputs	V_{CC} = 3V; V_I = 0.8V		75	150		µA
		V_{CC} = 3V; V_I = 2.0V		−75	−150		µA
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			60	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			±1	±100	µA
I_{OZH}	3-State output high current	V_{CC} = 3.6V; V_O = 3.0V			1	5	µA
I_{OZL}	3-State output low current	V_{CC} = 3.6V; V_O = 0.5V			−1	−5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.13	0.19	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			2	7	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0			0.13	0.19	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.

AC CHARACTERISTICS

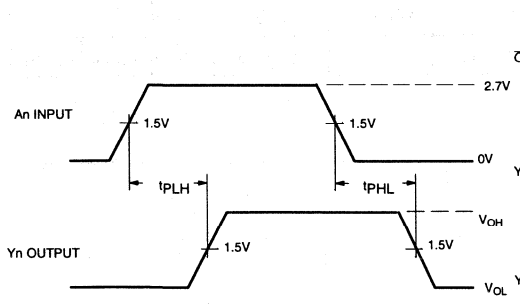
GND = 0V; $t_R = t_F$ = 6ns; C_L = 50pF; R_L = 500Ω, T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Yn	1	1.0 1.0	2.7 2.9	4.0 3.9	4.5 4.9	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}$n to Yn	2	1.0 1.1	3.4 3.4	4.7 4.7	6.0 6.5	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$n to Yn	2	1.8 1.3	3.7 2.6	5.1 4.5	5.7 4.0	ns

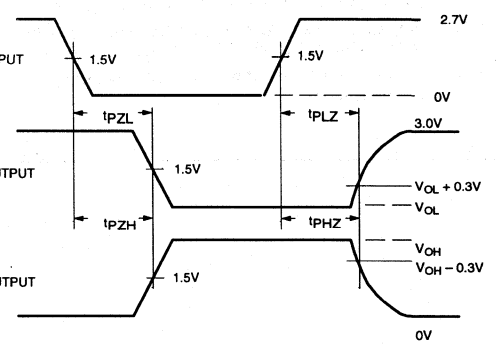
NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 2.7V

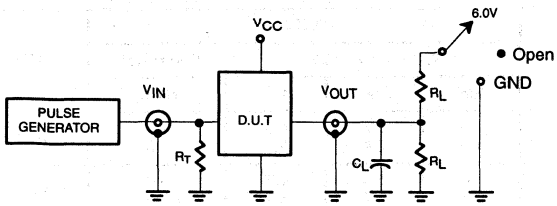


Waveform 1. Waveforms Showing the Input (An) to Output (Yn) Propagation Delays

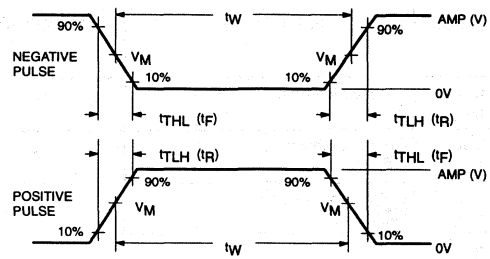


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

3.3V ABT Octal inverting buffer (3-State) 74LVT240

FEATURES

- Octal bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Power-up 3-State
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model.

DESCRIPTION

The LVT240 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is an octal inverting buffer that is ideal for driving bus lines. The device features two Output Enables ($1\overline{OE}$, $2\overline{OE}$), each controlling four of the 3-State outputs.

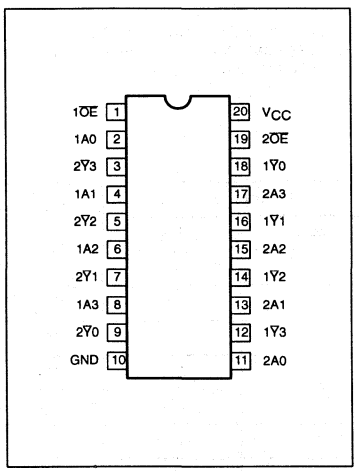
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to n$\overline{Y}$x	C_L = 50pF; V_{CC} = 3.3V	2.5	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or 3.0V	8	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	0.12	mA

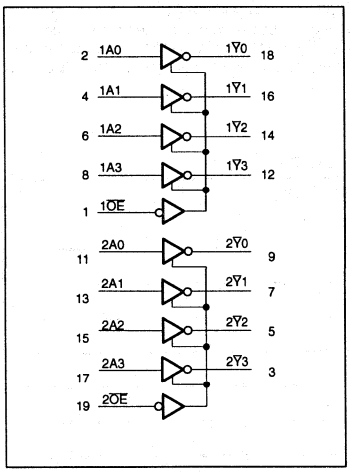
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-Pin Plastic Small Outline Large (300mil) (SOL)	–40°C to +85°C	74LVT240D	SOT163-1
20-Pin Plastic Shrink Small Outline (SSOP) Type II	–40°C to +85°C	74LVT240DB	SOT399-1
20-Pin Plastic Thin Shrink Small Outline (TSSOP) Type I	–40°C to +85°C	74LVT240PW	SOT360-1

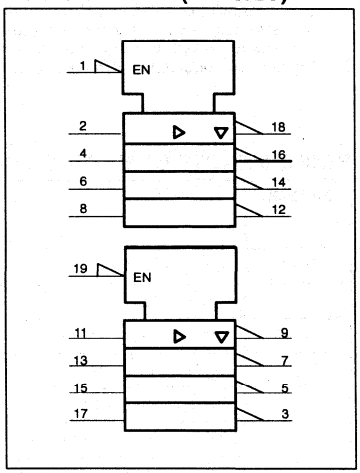
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS		OUTPUTS
$n\overline{OE}$	nAx	$n\overline{Y}x$
L	L	H
L	H	L
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "Off" state

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 4, 6, 8	1A0 – 1A3	Data inputs
11, 13, 15, 17	2A0 – 2A3	Data inputs
18, 16, 14, 12	$1\overline{Y}0 - 1\overline{Y}3$	Data outputs
9, 7, 5, 3	$2\overline{Y}0 - 2\overline{Y}3$	Data outputs
1, 19	$1\overline{OE}$, $2\overline{OE}$	Output enables
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
V_I	DC input voltage[3]		–0.5 to +7.0	V
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				T_{amb} = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_I = –18mA			0.9	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2	V_{CC}-0.1		V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4	2.5		V
		V_{CC} = 3V; I_{OH} = –32mA		2	2.2		V
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.1	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 3V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3V; I_{OL} = 64mA			0.4	0.55	
I_I	Input leakage current	V_{CC} = 0 or 3.6V; V_I = 5.5V			1	10	µA
		V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		±0.1	±1	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 3.6V; V_I = 0			–1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			1	±100	µA
I_{HOLD}	Bus hold current A inputs	V_{CC} = 3.0V; V_I = 0.8V	A inputs	75	150		µA
		V_{CC} = 3.0V; V_I = 2.0V		-75	–150		
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			60	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} = ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; OE/$\overline{OE}$ = Don't care			±1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V			1	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V			–1	–5	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; I_O = 0; V_I =V_{CC} or GND	Outputs High		0.12	0.19	mA
			Outputs Low		3	12	
			Outputs Disabled		0.12	0.19	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3.0 to 3.6V; One input at V_{CC} -0.6V; Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at T_{amb} = 25°C.
2. This is the increase in supply current for each input at V_{CC} –0.6V.
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 10% a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C.
4. Unused pins at V_{CC} or GND

AC CHARACTERISTICS

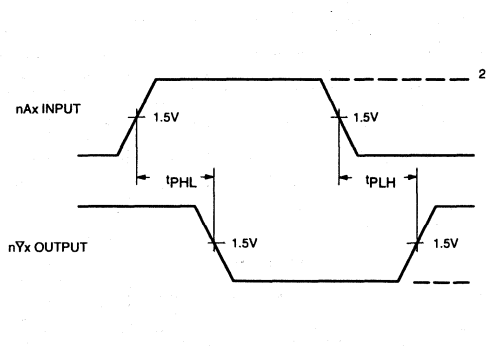
GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			T_{amb} = –40°C to +85°C, V_{CC} = +3.3V ±0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to n$\overline{Y}$x	1	1 1	2.5 2.5	4.3 4.3	5.2 5.0	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1 1	3.7 3.1	5.2 5.2	6.3 6.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	2 1.6	3.4 3.2	5.6 5.1	6.3 5.6	ns

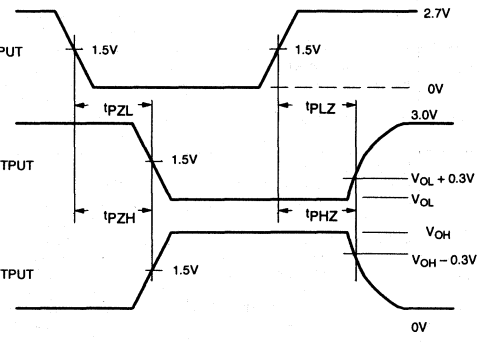
NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 2.7V

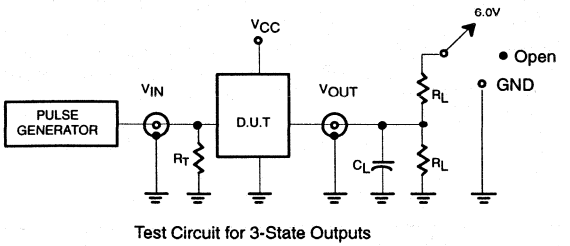


Waveform 1. Waveforms Showing the Input (nAx) to Output (n$\overline{Y}$x) Propagation Delays

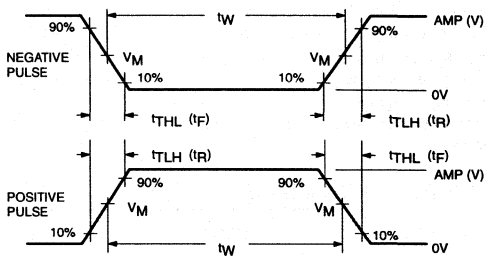


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

3.3V ABT Octal buffer/line driver (3-State) 74LVT244A

FEATURES

- Octal bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Power-up 3-State
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT244A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is an octal buffer that is ideal for driving bus lines. The device features two Output Enables ($\overline{OE}1$, $\overline{OE}2$), each controlling four of the 3-State outputs.

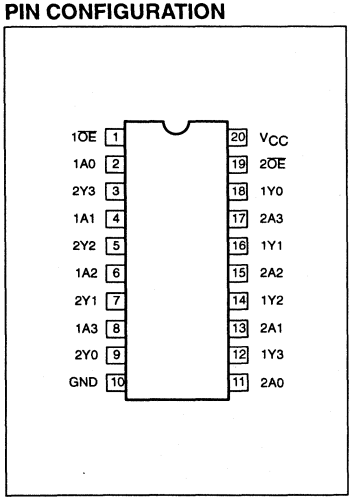
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	C_L = 50pF; V_{CC} = 3.3V	2.5	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or 3.0V	8	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	0.13	mA

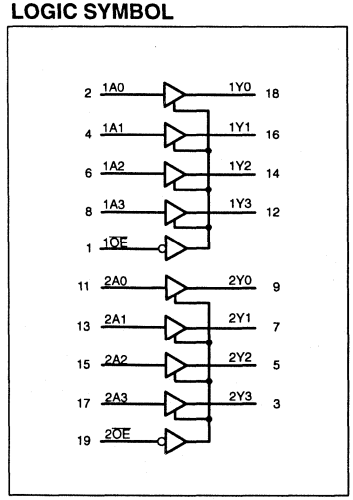
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-Pin Plastic Small Outline Large (300mil) (SOL)	–40°C to +85°C	74LVT244AD	SOT163-1
20-Pin Plastic Shrink Small Outline SSOP Type II	–40°C to +85°C	74LVT244ADB	SOT399-1
20-Pin Plastic Thin Shrink Small Outline TSSOP Type I	–40°C to +85°C	74LVT244APW	SOT360-1

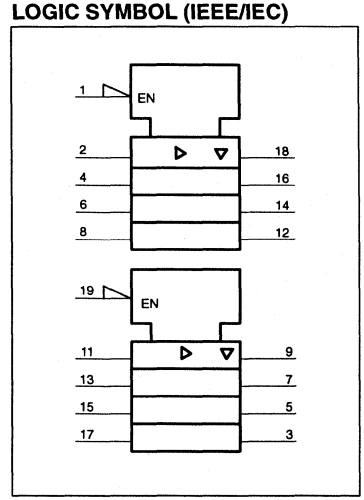
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{nOE1}$	nAx	nYx
L	L	L
L	H	H
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 4, 6, 8	1A0 – 1A3	Data inputs
11. 13, 15, 17	2A0 – 2A3	Data inputs
18, 16, 14, 12	1Y0 – 1Y3	Data outputs
9, 7, 5, 3	2Y0 – 2Y3	Data outputs
1, 19	$1\overline{OE}$, $2\overline{OE}$	Output enables
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
V_I	DC input voltage[3]		–0.5 to +7.0	V
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%, f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–0.9	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2	V_{CC}-0.1		V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4	2.5		
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.2		
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.1	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
I_I	Input leakage current	V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	µA
		V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		±0.1	±1	
		V_{CC} = 3.6V; V_I = V_{CC}	Data Pins[4]		0.1	1	
		V_{CC} = 3.6V; V_I = 0			–1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			1	±100	µA
I_{HOLD}	Bus Hold current A inputs	V_{CC} = 3V; V_I = 0.8V		75	150		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–150		µA
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			60	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			±1	±100	µA
I_{OZH}	3-State output high current	V_{CC} = 3.6V; V_O = 3V; V_I = V_{IL} or V_{IH}			1	5	µA
I_{OZL}	3-State output low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			–1	–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.13	0.19	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3	12	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0			0.13	0.19	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.

AC CHARACTERISTICS

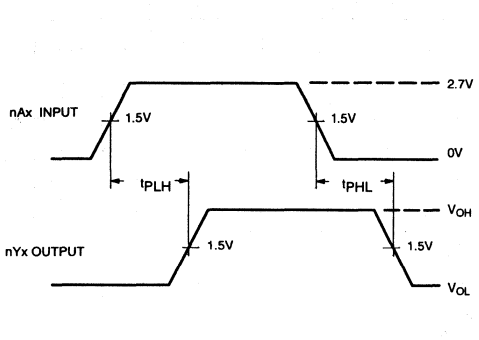
GND = 0V; $t_R = t_F$ = 6ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	1	1 1	2.5 2.6	4.1 4.1	5.0 5.1	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1 1.1	3.2 3.1	5.2 5.2	6.3 6.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.9 1.8	3.3 3.3	5.6 5.1	6.3 5.6	ns

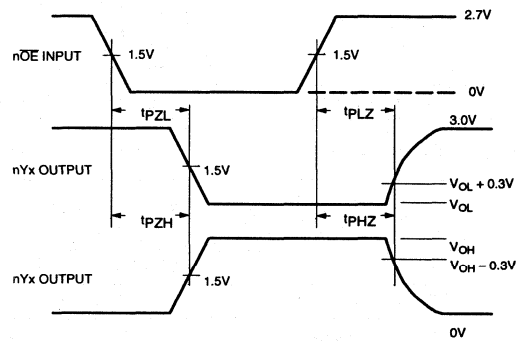
NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 2.7V

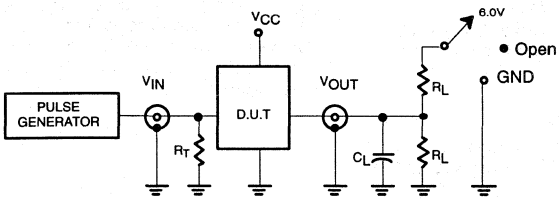


Waveform 1. Waveforms Showing the Input (nAx) to Output (nYx) Propagation Delays

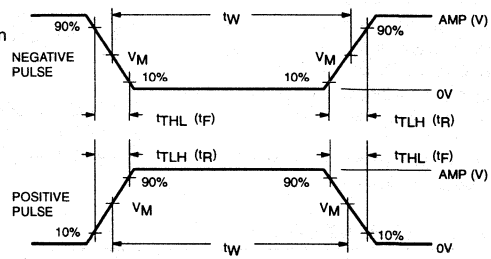


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

3.3V ABT Octal transceiver with direction pin (3-State)

74LVT245

FEATURES

- Octal bidirectional bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT245 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an Output Enable ($\overline{OE}$) input for easy cascading and a Direction (DIR) input for direction control.

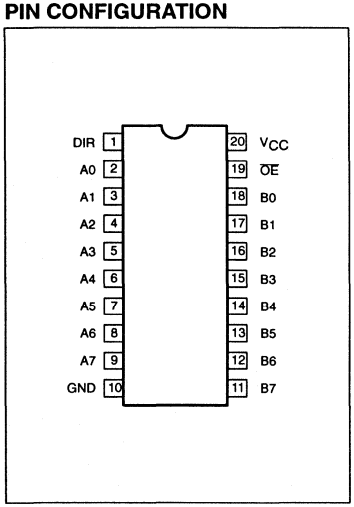
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 3.3V	2.4	ns
C_{IN}	Input capacitance DIR, $\overline{OE}$	V_I = 0V or 3.0V	4	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O}$ = 0V or 3.0V	10	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	0.13	mA

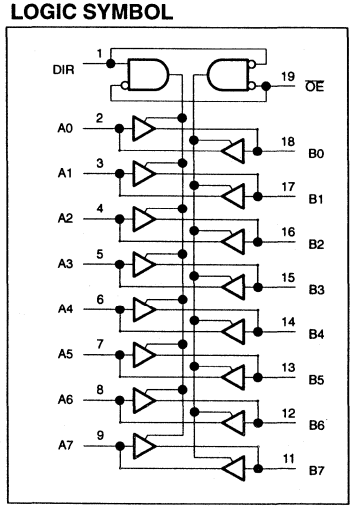
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-pin Plastic Small Outline Large (300mil) (SOL)	–40°C to +85°C	74LVT245D	SOT163-1
20-pin Plastic Shrink Small Outline SSOP Type II	–40°C to +85°C	74LVT245DB	SOT339-1
20-pin Plastic Thin Shrink Small Outline TSSOP Type I	–40°C to +85°C	74LVT245PW	SOT360-1

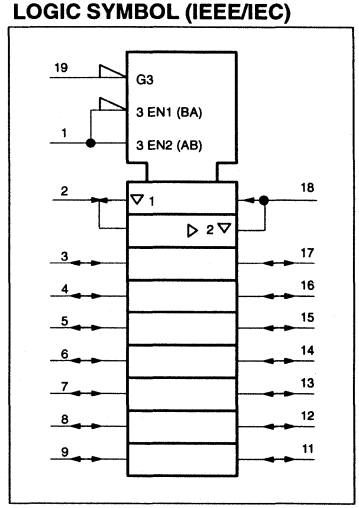
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



3.3V ABT Octal transceiver with direction pin (3-State)

74LVT245

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}n$	DIR	An	Bn
L	L	An = Bn	Inputs
L	H	Inputs	Bn = An
H	X	Z	Z

H = High Voltage Level
L = Low Voltage Level
X = Don't Care
Z = High impedance "Off" State

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	DIR	Direction control input
2, 3, 4, 5, 6, 7, 8, 9	A0 – A7	Data inputs/outputs (A side)
18, 17, 16, 15, 14, 13, 12, 11	B0 – B7	Data inputs/outputs (B side)
19	$\overline{OE}$	Output enable input (active–Low)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

ABSOLUTE MAXIMUM RATINGS[1,2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–0.9	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2	V_{CC}-0.1		V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4	2.5		
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.2		
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.1	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
I_I	Input leakage current	V_{CC} = 0 or 3.6V; V_I = 5.5V	Control pins		1	10	µA
		V_{CC} = 3.6V; V_I = V_{CC} or GND			±0.1	±1	
		V_{CC} = 3.6V; V_I = 5.5V	I/O Data pins[4]		1	20	
		V_{CC} = 3.6V; V_I = V_{CC}			0.1	1	
		V_{CC} = 3.6V; V_I = 0			–1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			1	±100	µA
I_{HOLD}	Bus Hold current A or B ports	V_{CC} = 3V; V_I = 0.8V		75	150		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–150		µA
I_{EX}	Current into an ouptut in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			60	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			15	±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.13	0.19	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3	12	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0			0.13	0.19	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specificed voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = +25°C only.
4. Unused pins at V_{CC} or GND.

AC CHARACTERISTICS

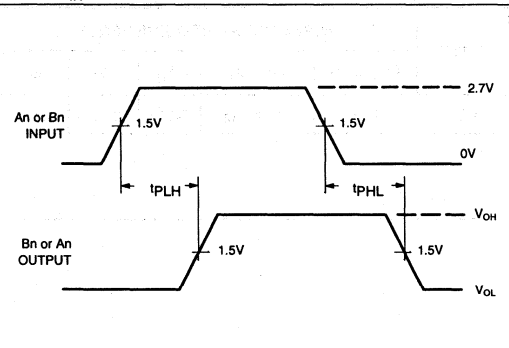
GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V +0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	1	1.0 1.0	2.4 2.4	4.0 4.0	4.7 4.6	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.1 1.5	3.3 3.2	5.5 5.5	7.1 6.5	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	2.2 2.0	3.6 3.4	5.9 4.8	6.5 4.8	ns

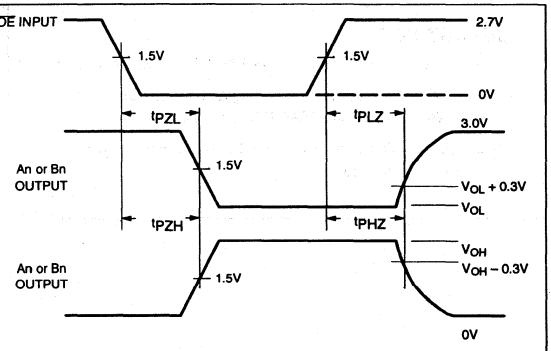
NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 2.7V

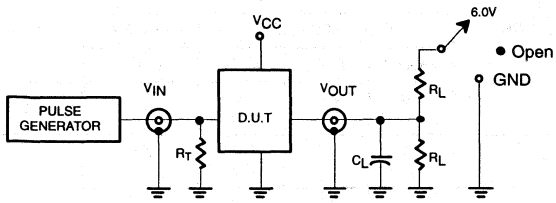


Waveform 1. Waveforms Showing the Input to Output Propagation Delays

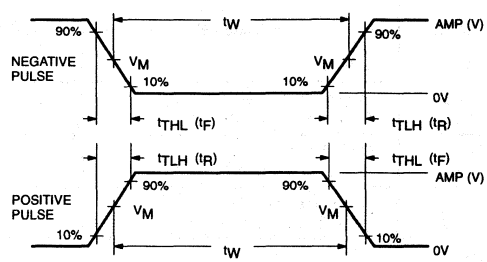


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

3.3V ABT Octal D flip-flop | 74LVT273

FEATURES

- Eight edge-triggered D-type flip-flops
- Buffered common clock
- Buffered asynchronous Master Reset
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Power-up reset
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus

DESCRIPTION

The LVT273 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced Low independent of Clock or Data inputs by a Low voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the CP and $\overline{MR}$ are common elements.

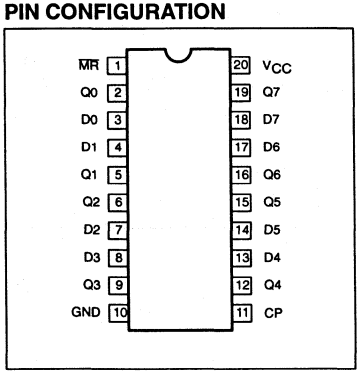
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Qn	C_L = 50pF; V_{CC} = 3.3V	3.5	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	4	pF

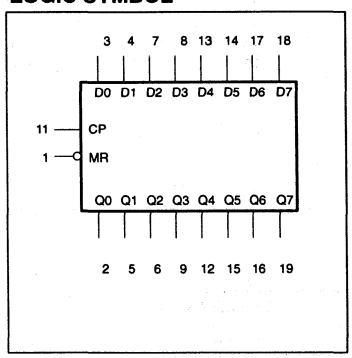
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-pin Plastic Small Outline Large (300mil)(SOL)	–40°C to +85°C	74LVT273D	SOT163-1
20-pin Plastic Shrink Small Outline (SSOP) Type II	–40°C to +85°C	74LVT273DB	SOT399-1
20-pin Plastic Thin Shrink Small Outline (TSSOP) Type I	–40°C to +85°C	74LVT273PW	SOT360-1

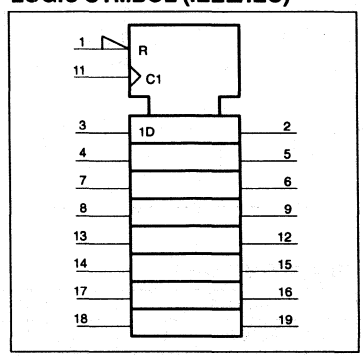
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

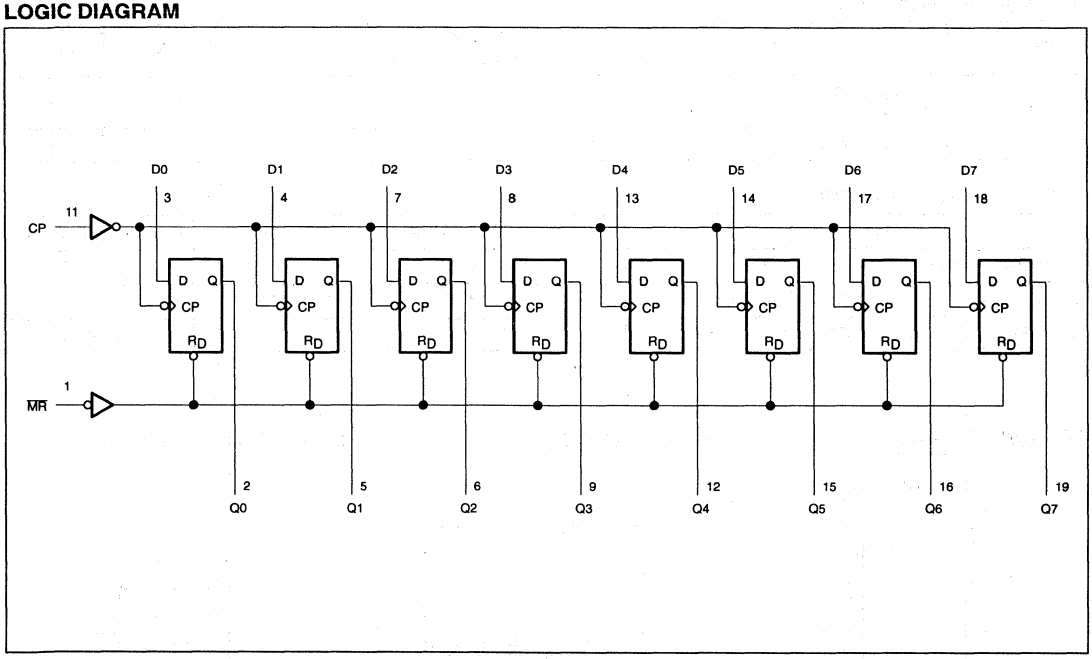


3.3V ABT Octal D flip-flop | 74LVT273

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
11	CP	Clock pulse input (active rising edge)
3, 4, 7, 8, 13, 14, 17, 18	D0 – D7	Data inputs
2, 5, 6, 9, 12, 15, 16, 19	Q0 – Q7	Data outputs
1	$\overline{MR}$	Master Reset input (active-Low)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING
$\overline{MR}$	CP	D_n	Q0 – Q7	MODE
L	X	X	L	Reset (clear)
H	↑	h	H	Load "1"
H	↑	l	L	Load "0"
H	L	X	Q_0	Retain state

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
Q_0 = Output as it was

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High State	–64	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–0.9	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2	V_{CC}–0.1		V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4	2.5		
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.2		
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.1	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[4]	V_{CC} = 3.6V; I_O = 1mA; V_I = GND or V_{CL}			0.13	0.55	V
I_I	Input leakage current	V_{CC} = 0 or 3.6V; V_I = 5.5V			1	10	µA
		V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		±0.1	±1	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[3]		0.1	1	
		V_{CC} = 3.6V; V_I = 0			–1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			1	±100	µA
I_{HOLD}	Bus Hold current A inputs	V_{CC} = 3V; V_I = 0.8V		75	150		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–150		µA
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			60	125	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.13	0.19	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3	12	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC} -0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. Unused pins at V_{CC} or GND.
4. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
f_{MAX}	Maximum clock frequency	1	150				MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn	1	1.7 1.9	3.5 3.5	5.5 5.5	6.3 5.9	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Qn	2	1.3	3.2	6.2	6.2	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

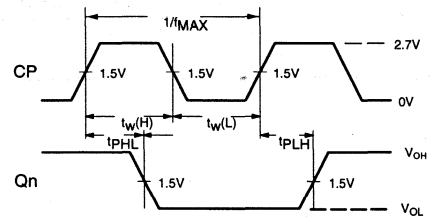
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω, T_{amb} = –40°C to +85°C.

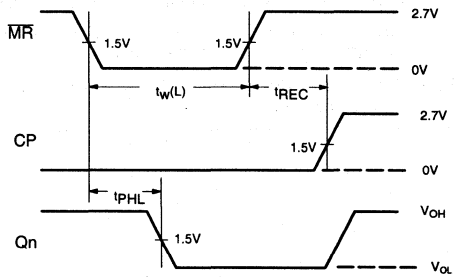
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = +3.3 ± 0.3V		V_{CC} = 2.7V	
			MIN	TYP	MIN	
$t_s(H)$ $t_s(L)$	Setup time, High or Low Dn to CP	3	2.3 2.3	1.0 1.0	2.7 2.7	ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to CP	3	0 0	–0.6 –0.6	0 0	ns
$t_w(H)$ $t_w(L)$	Clock pulse width High or Low	1	3.3 3.3	1.5 1.5	3.3 3.3	ns
$t_w(L)$	Master Reset pulse width, Low	2	3.3	1.5	3.3	ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	2.7	1.0	3.2	ns

AC WAVEFORMS

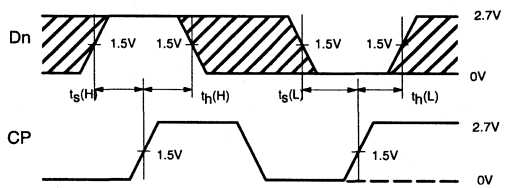
V_M = 1.5V, V_{IN} = GND to 2.7V



Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



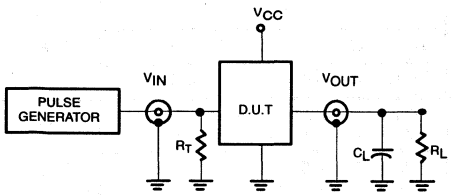
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



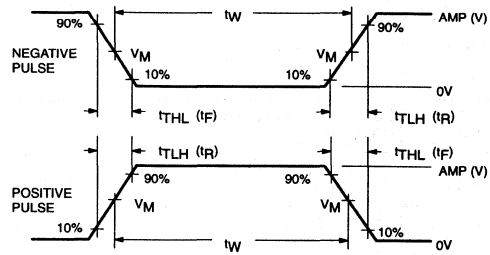
Waveform 3. Data Setup and Hold Times

NOTE: The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Outputs



V_M = 1.5V
Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

3.3V ABT Octal latched transceiver with dual enable (3-State)

74LVT543

FEATURES

- Combines 74LVT245 and 74LVT373 type functions in one device
- 8-bit octal transceiver with D-type latch
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- Output capability: +64mA/–32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Power-up 3-State
- Power-up reset
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT543 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable ($\overline{LEAB}$, $\overline{LEBA}$) and Output Enable ($\overline{OEAB}$, $\overline{OEBA}$) inputs are provided for each register to permit independent control of data transfer in either direction. The outputs are guaranteed to sink 64mA.

FUNCTIONAL DESCRIPTION

The 'LVT543 contains two sets of eight D–type latches, with separate control pins for each set. Using data flow from A to B as an example, when the A-to-B Enable ($\overline{EAB}$) input and the A-to-B Latch Enable ($\overline{LEAB}$) input are Low the A-to-B path is transparent. A subsequent Low-to-High transition of the $\overline{LEAB}$ signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With $\overline{EAB}$ and $\overline{OEAB}$ both Low, the 3-State B output buffers are active and display the data present at the outputs of the A latches.

Control of data flow from B to A is similar, but using the $\overline{EBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

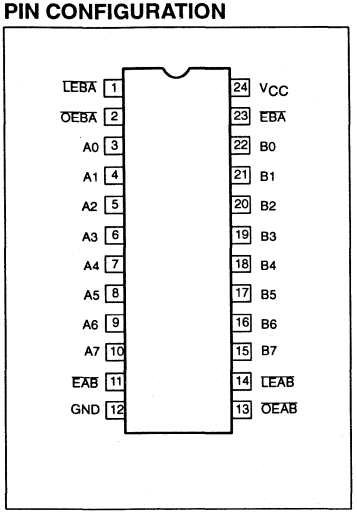
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 3.3V	3.3	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	4.5	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; $V_{I/O}$ = 0V or 3.0V	11	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	.13	mA

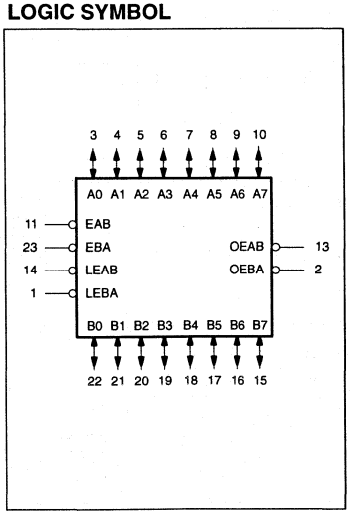
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
24-pin Plastic Small Outline Large (300mil) (SOL)	–40°C to +85°C	74LVT543D	SOT137-1
24-pin Plastic Shrink Small Outline (SSOP) Type II	–40°C to +85°C	74LVT543DB	SOT340-1
24-pin Plastic Thin Shrink Small Outline (TSSOP) Type I	–40°C to +85°C	74LVT543PW	SOT355-1

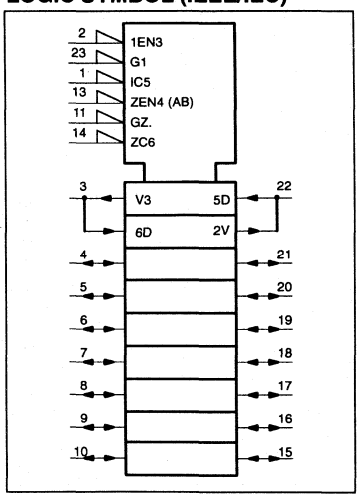
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



3.3V ABT Octal latched transceiver with dual enable (3-State)

74LVT543

PIN DESCRIPTION

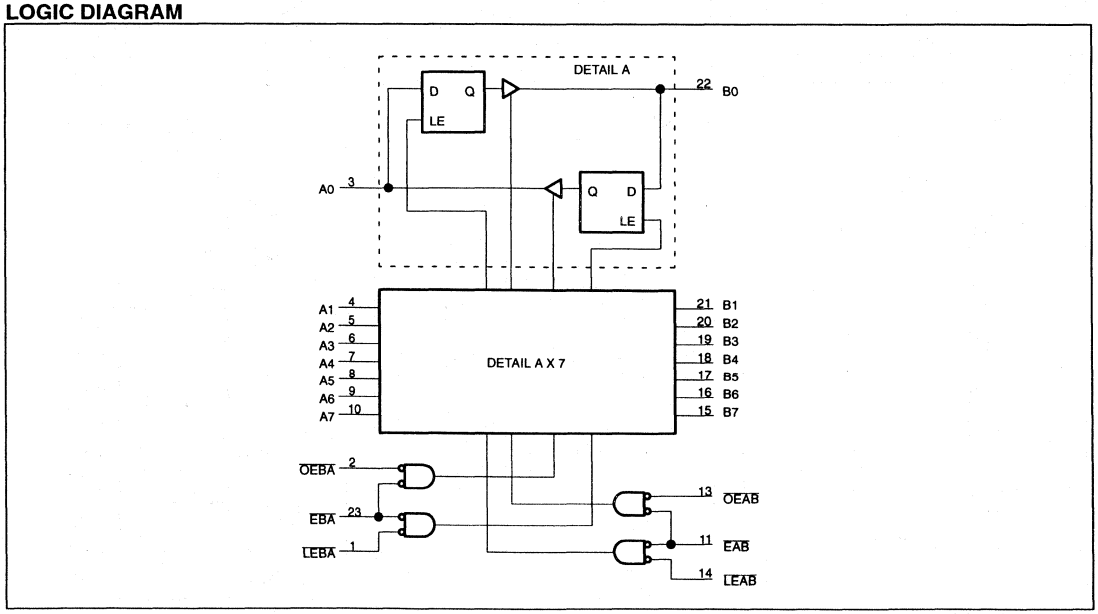
PIN NUMBER	SYMBOL	FUNCTION
14, 1	$\overline{LEAB}$ / $\overline{LEBA}$	A to B / B to A Latch Enable Input (active-Low)
11, 23	$\overline{EAB}$ / $\overline{EBA}$	A to B / B to A Enable input (active-Low)
13, 2	$\overline{OEAB}$ / $\overline{OEBA}$	A to B / B to A Output Enable input (active-Low)
3, 4, 5, 6, 7, 8, 9, 10	A0 – A7	Port A, 3-State outputs
22, 21, 20, 19, 18, 17, 16, 15	B0 – B7	Port B, 3-State outputs
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
$\overline{OEXX}$	$\overline{EXX}$	$\overline{LEXX}$	An or Bn	Bn or An	
H	X	X	X	Z	Disabled
X	H	X	X	Z	Disabled
L L	↑ ↑	L L	h l	Z Z	Disabled + Latch
L L	L L	↑ ↑	h l	H L	Latch + Display
L L	L L	L L	H L	H L	Transparent
L	L	H	X	NC	Hold

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX = AB or BA)
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX = AB or BA)
X = Don't care
↑ = Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX = AB or BA)
NC= No change
Z = High impedance or "off" state

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–0.9	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2	V_{CC}-0.1		V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4	2.5		
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.2		
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.1	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[5]	V_{CC} = 3.6V; I_O = 1mA; V_I = GND or V_{CC}			0.13	0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		±0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			1	10	
		V_{CC} = 3.6V; V_I = 5.5V	I/O Data pins[4]		1	20	
		V_{CC} = 3.6V; V_I = V_{CC}			0.1	1	
		V_{CC} = 3.6V; V_I = 0			–1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			1	±100	µA
I_{HOLD}	Bus Hold current A or B ports	V_{CC} = 3V; V_I = 0.8V		75	150		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–150		
I_{EX}	Current into an ouptut in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			60	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			15	±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.13	0.19	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3	12	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0			0.13	0.19	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC} -0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specificed voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn, Bn to An	2	1.0 1.0	2.3 3.0	4.7 4.6	5.5 5.8	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEBA}$ to An, $\overline{LEAB}$ to Bn	1, 2	1.0 1.0	3.6 4.2	5.9 5.7	7.3 7.3	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	4 5	1.0 1.1	3.8 3.8	5.8 6.4	7.6 8.2	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	4 5	2.4 2.0	3.7 3.5	6.5 5.8	7.1 5.9	ns
t_{PZH} t_{PZL}	Output enable time $\overline{EBA}$ to An, $\overline{EAB}$ to Bn	4 5	1.0 1.4	4.0 4.1	6.0 6.7	7.6 8.3	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{EBA}$ to An, $\overline{EAB}$ to Bn	4 5	2.3 2.0	3.7 3.5	6.4 5.4	7.1 5.6	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

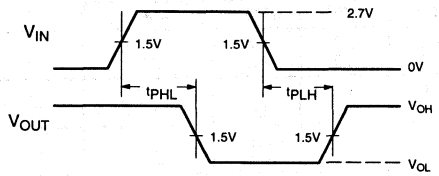
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

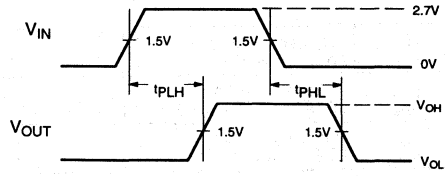
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V ±0.3V		V_{CC} = 2.7V	
			MIN	MAX	MIN	
t_s(H) t_s(L)	Setup time An to $\overline{LEAB}$, Bn to $\overline{LEBA}$	3	0 0.8		0 1.1	ns
t_h(H) t_h(L)	Hold time An to $\overline{LEAB}$, Bn to $\overline{LEBA}$	3	1.7 1.7		1.7 1.7	ns
t_s(H) t_s(L)	Setup time An to $\overline{EAB}$, Bn to $\overline{EBA}$	3	0 0.9		0 1.2	ns
t_h(H) t_h(L)	Hold time An to $\overline{EAB}$, Bn to $\overline{EBA}$	3	1.8 1.8		1.8 1.8	ns
t_w(L)	Latch enable pulse width, Low	3	3.3		3.3	ns

AC WAVEFORMS

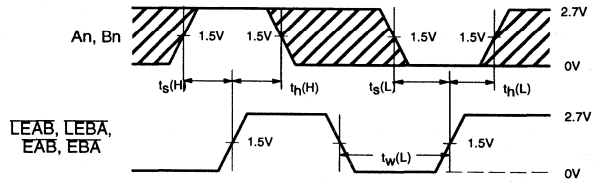
V_M = 1.5V, V_{IN} = GND to 2.7V



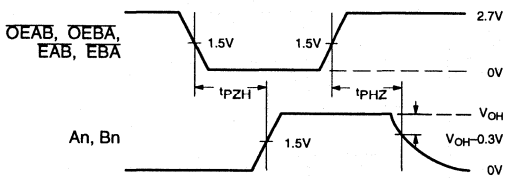
Waveform 1. Propagation Delay For Inverting Output



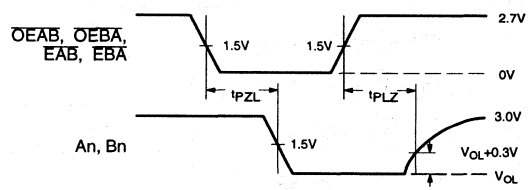
Waveform 2. Propagation Delay For Non-Inverting Output



Waveform 3. Data Setup and Hold Times And Latch Enable Pulse Width



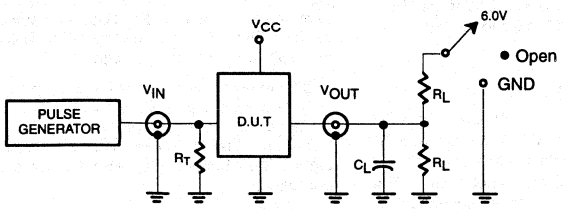
Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



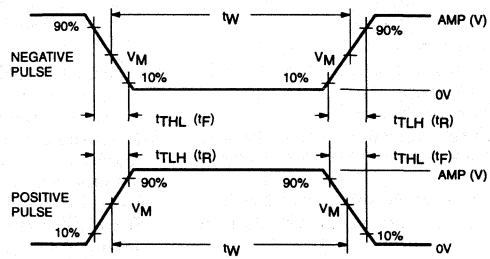
Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

3.3V ABT Octal D-type transparent latch (3-State) 74LVT573

FEATURES

- Inputs and outputs on opposite side of package allow easy interface to microprocessors
- 3-State output buffers
- Common output enable
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- Power-up 3-State
- Power-up reset
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT573 is a high-performance BiCMOS product designed for VCC operation at 3.3V. This device is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates. The 74LVT573 has a broadside pinout configuration to facilitate PC board layout and allow easy interface with microprocessors.

The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is High. The latch remains transparent to the data inputs while E is High, and stores the data that is present one setup time before the High-to-Low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation.

When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

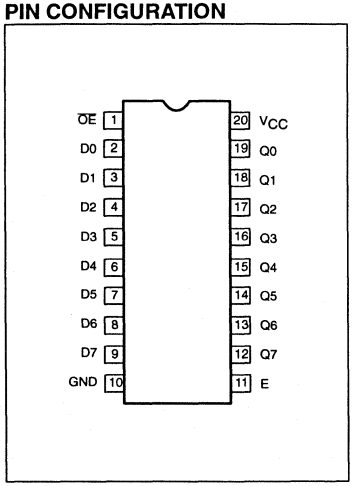
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	C_L = 50pF; V_{CC} = 3.3V	2.7	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or 3.0V	8	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	.13	mA

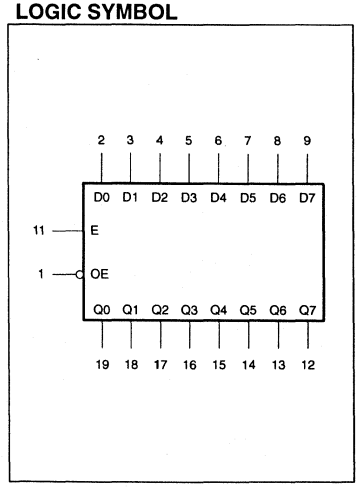
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-pin Plastic Small Outline Large (300mil) (SOL)	–40°C to +85°C	74LVT573D	SOT163-1
20-pin Plastic Shrink Small Outline (SSOP) Type II	–40°C to +85°C	74LVT573DB	SOT399-1
20-pin Plastic Thin Shrink Small Outline (TSSOP) Type I	–40°C to +85°C	74LVT573PW	SOT360-1

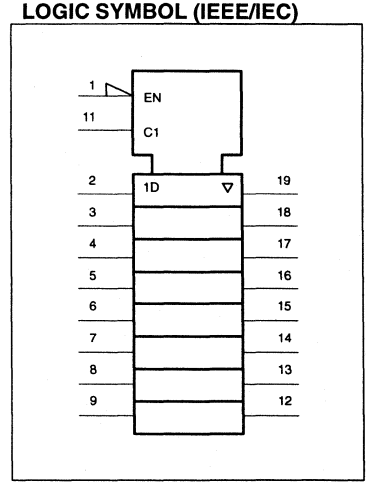
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



3.3V ABT Octal D-type transparent latch (3-State) 74LVT573

PIN DESCRIPTION

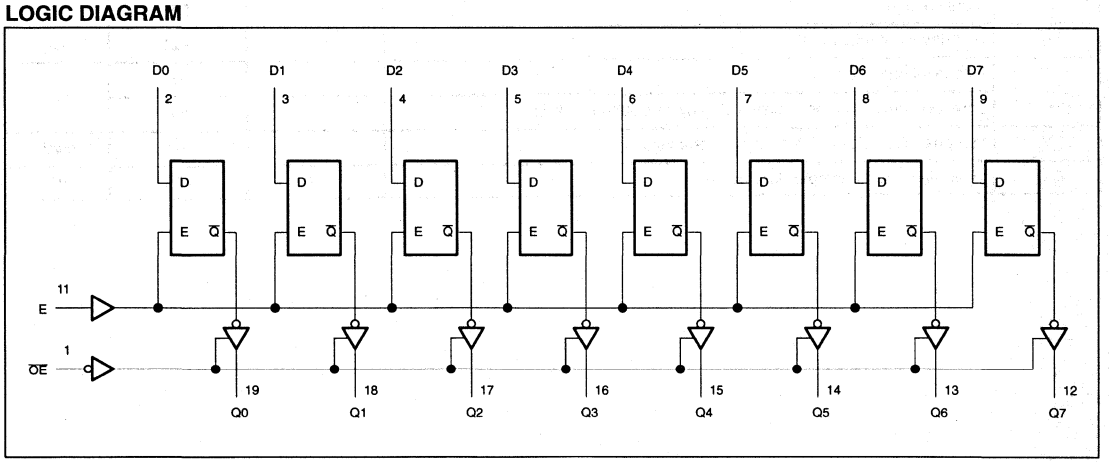
PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active-Low)
2, 3, 4, 5, 6, 7, 8, 9	D0-D7	Data inputs
19, 18, 17, 16, 15, 14, 13, 12	Q0-Q7	Data outputs
11	E	Enable input (active-High)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			INTERNAL	OUTPUTS	OPERATING
$\overline{OE}$	E	Dn	REGISTER	Q0 – Q7	MODE
L L	H H	L H	L H	L H	Enable and read register
L L	↓ ↓	l h	L H	L H	Latch and read register
L	L	X	NC	NC	Hold
H H	L H	X Dn	NC Dn	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC= No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%, f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–0.9	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2	V_{CC}-0.1		V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4	2.5		
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.2		
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.1	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[5]	V_{CC} = 3.6V; I_O = 1mA; V_I = GND or V_{CC}			0.13	0.55	V
I_I	Input leakage current	V_{CC} = 0 or 3.6V; V_I = 5.5V			1	10	µA
		V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		±0.1	±1	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 3.6V; V_I = 0			–1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			1	±100	µA
I_{HOLD}	Bus Hold current D inputs	V_{CC} = 3V; V_I = 0.8V		75	150		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–150		
I_{EX}	Current into an ouptut in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			60	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC}= 3.6V; V_O = 3V; V_I = V_{IL} or V_{IH}			1	5	µA
I_{OZL}	3-State output Low current	V_{CC}= 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			–1	–5	
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.13	0.19	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3	12	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0			0.13	0.19	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specificed voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only
4. Unused pins at V_{CC} or GND.
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ± 0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	2	1.0 1.0	2.5 2.7	4.2 4.3	4.7 5.2	ns
t_{PLH} t_{PHL}	Propagation delay E to Qn	1	1.6 2.5	3.5 4.3	5.6 6.5	6.3 7.2	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	4 5	1.0 1.3	2.8 3.3	5.1 5.5	6.2 6.6	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	4 5	2.0 1.5	3.7 3.0	5.7 4.6	6.7 5.1	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

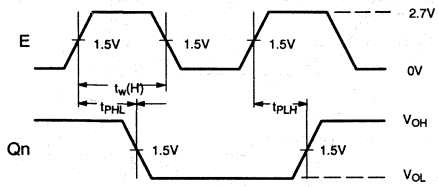
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

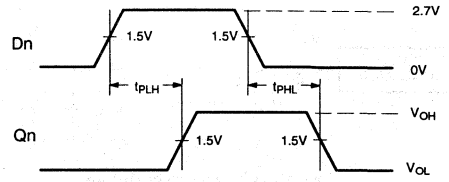
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V ± 0.3V		V_{CC} = 2.7V	
			MIN	MAX	MIN	
$t_S(H)$ $t_S(L)$	Setup time, High or Low, Dn to E	3	0.7 0.7		0.6 0.6	ns
$T_H(H)$ $T_H(L)$	Hold time, High or Low, Dn to E	3	1.6 1.6		1.8 1.8	ns
$T_W(H)$	E pulse width High	1	3.3		3.3	ns

AC WAVEFORMS

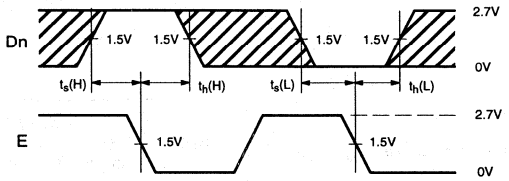
V_M = 1.5V, V_{IN} = GND to 2.7V



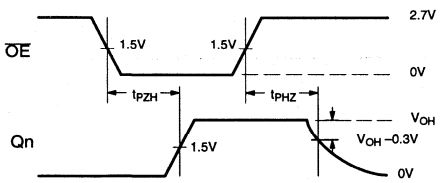
Waveform 1. Propagation Delay, Enable to Output, and Enable Pulse Width



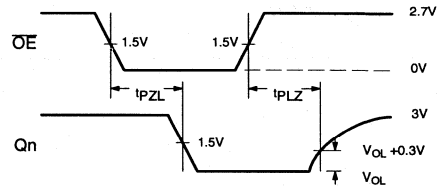
Waveform 2. Propagation Delay for Data to Outputs



Waveform 3. Data Setup and Hold Times



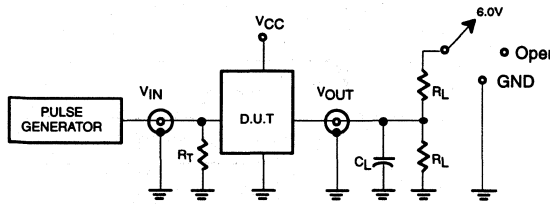
Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



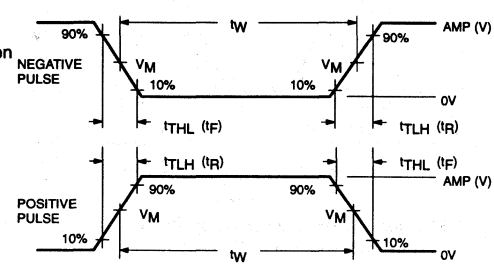
Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

3.3V ABT Octal D-type flip-flop (3-State) 74LVT574

FEATURES

- Inputs and outputs on opposite side of package allow easy interface to microprocessors
- 3-State outputs for bus interfacing
- Common output enable
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Power-up 3-State
- Power-up reset
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT574 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{OE}$) control gates. The state of each D input (one set-up time before the Low-to-High clock transition) is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the clock operation.

When $\overline{OE}$ is Low, the stored data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "off" state, which means they will neither drive nor load the bus.

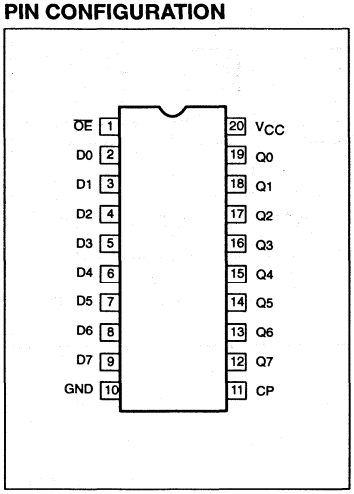
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Qn	C_L = 50pF; V_{CC} = 3.3V	3.6 4.3	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	4	pF
C_{OUT}	Output capacitance	Outputs disabled; $V_{I/O}$ = 0V or 3.0V	8	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	.13	mA

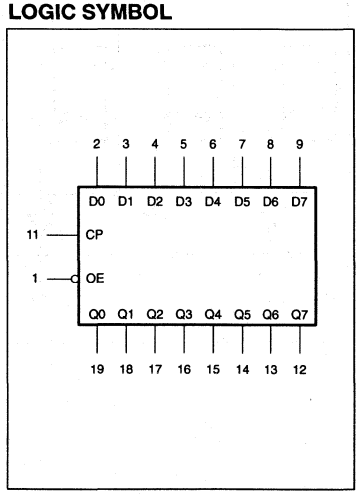
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-Pin Plastic Small Outline Large (300mil) (SOL)	–40°C to +85°C	74LVT574D	SOT163-1
20-Pin Plastic Shrink Small Outline (SSOP) Type II	–40°C to +85°C	74LVT574DB	SOT399-1
20-Pin Plastic Thin Shrink Small Outline (TSSOP) Type I	–40°C to +85°C	74LVT574PW	SOT360-1

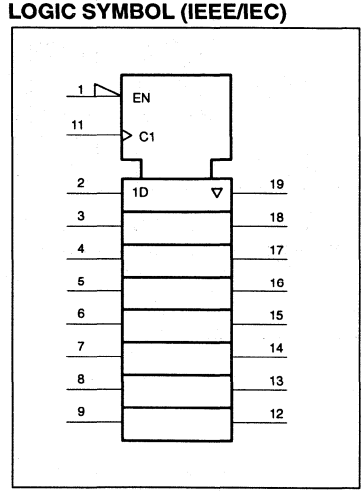
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



3.3V ABT Octal D-type flip-flop (3-State) 74LVT574

PIN DESCRIPTION

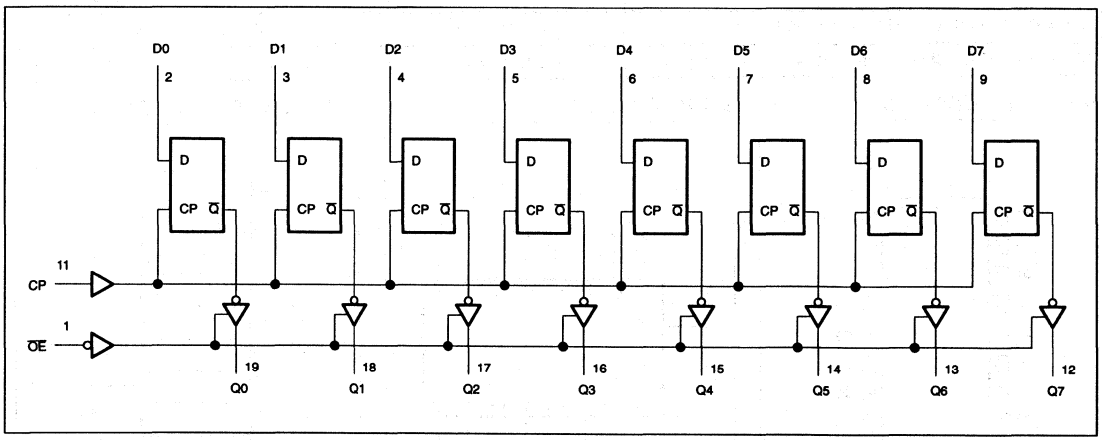
PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active-low)
2, 3, 4, 5, 6, 7, 8, 9	D0-D7	Data inputs
19, 18, 17, 16, 15, 14, 13, 12	Q0-Q7	Data outputs
11	CP	Clock pulse input (active rising edge)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			INTERNAL	OUTPUTS	OPERATING
$\overline{OE}$	CP	Dn	REGISTER	Q0 – Q7	MODE
L	L	X	Q0	Q0	Retain output
L L	↑ ↑	l h	L H	L H	Load and read register
L	L	X	NC	NC	Hold
H	X	X	NC	Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
Q0 = output as it was

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%, f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–0.9	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2	V_{CC}-0.1		V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4	2.5		
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.2		
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.1	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[5]	V_{CC} = 3.6V; I_O = 1mA; V_I = GND or V_{CC}			0.13	0.55	V
I_I	Input leakage current	V_{CC} = 0 or 3.6V; V_I = 5.5V			1	10	µA
		V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		±0.1	±1	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 3.6V; V_I = 0			–1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			1	±100	µA
I_{HOLD}	Bus Hold current D inputs	V_{CC} = 3V; V_I = 0.8V		75	150		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–150		µA
I_{EX}	Current into an ouptut in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			60	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}/OE$ = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC}= 3.6V; V_O = 3V; V_I = V_{IL} or V_{IH}			1	5	µA
I_{OZL}	3-State output Low current	V_{CC}= 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			1	–5	µA
I_{CCH}	Quiescent supply current[3]	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.13	0.19	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3	12	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0			0.13	0.19	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC} -0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specificed voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			V_{CC} = 3.3V ± 0.3V			V_{CC} = 2.7V		
			MIN	TYP[1]	MIN	MIN	MAX	
f_{MAX}	Maximum clock frequency	1	150			150		ns
t_{PLH} t_{PHL}	Propagation delay CP to Qn	1	1.7 2.4	3.6 4.3	5.4 5.9		6.2 6.6	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	3 4	1.0 1.3	2.9 3.4	4.8 5.1		5.9 6.2	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	3 4	1.9 1.7	4.0 3.2	5.5 4.5		5.9 4.5	ns

NOTE:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

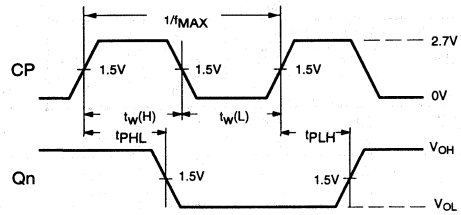
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

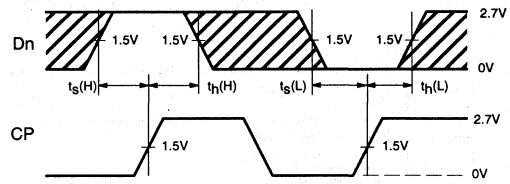
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V ± 0.3V		V_{CC} = 2.7V	
			MIN	MAX	MIN	
$t_S(H)$ $t_S(L)$	Setup time, High or Low, Dn to CP	2	2.0 2.0		2.4 2.4	ns
$T_H(H)$ $T_H(L)$	Hold time, High or Low, Dn to CP	2	0.3 0.3		0 0	ns
$T_W(H)$	CP pulse width High or Low	1	3.3 3.3		3.3 3.3	ns

AC WAVEFORMS

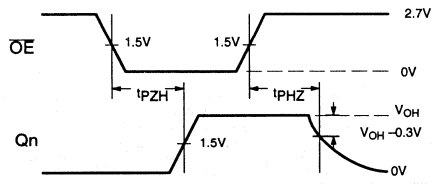
V_M = 1.5V, V_{IN} = GND to 2.7V



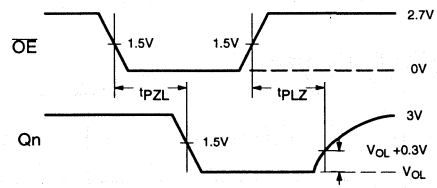
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Data Setup and Hold Times



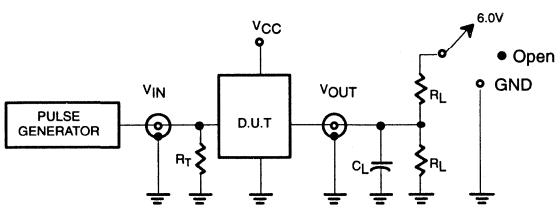
Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



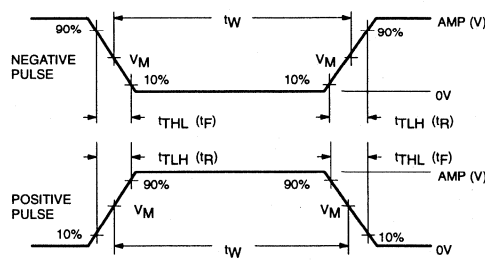
Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

3.3V ABT Octal bus transceiver/register (3-State) 74LVT646

FEATURES

- Combines 74LVT245 and 74LVT574 type functions in one device
- Independent registers for A and B buses
- Multiplexed real–time and stored data
- Output capability: +64mA/–32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- Power-up 3-State
- Power-up reset
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT646 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device consists of bus transceiver circuits with 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers.

Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High.

Output Enable ($\overline{OE}$) and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or both.

The Select (SAB, SBA) pins determine whether data is stored or transferred through the device in real–time. The DIR determines which bus will receive data when the $\overline{OE}$ is active (Low).

In the isolation mode ($\overline{OE}$ = High), data from Bus A may be stored in the B register and/or data from Bus B may be stored in the A register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B may be driven at a time. The examples on the next page demonstrate the four fundamental bus management functions that can be performed with the 74LVT646.

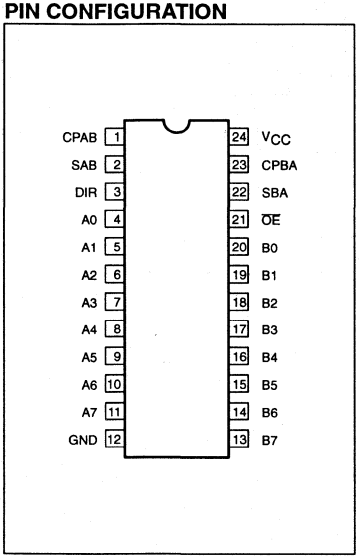
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 3.3V	2.8	ns
C_{IN}	Input capacitance CP, S, $\overline{OE}$, DIR	$V_{I/O}$ = 0V or 3.0V	4.5	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; $V_{I/O}$ = 0V or 3.0V	11	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	0.13	mA

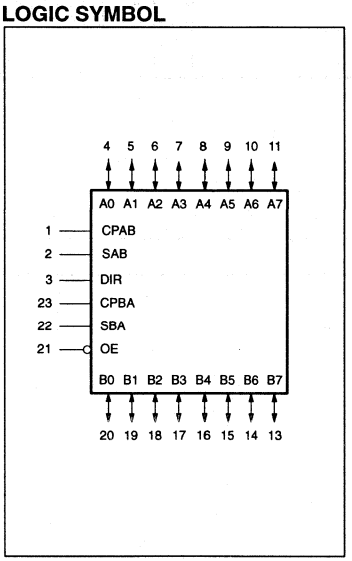
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
24-Pin plastic Small Outline Large (300mil) (SOL)	–40°C to +85°C	74LVT646D	SOT137-1
24-Pin Plastic Shrink Small Outline SSOP Type II	–40°C to +85°C	74LVT646DB	SOT340-1
24-Pin Plastic Thin Shrink Small Outline TSSOP Type I	–40°C to +85°C	74LVT646PW	SOT355-1

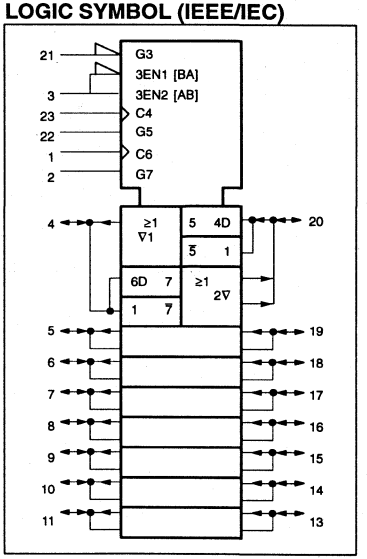
PIN CONFIGURATION



LOGIC SYMBOL



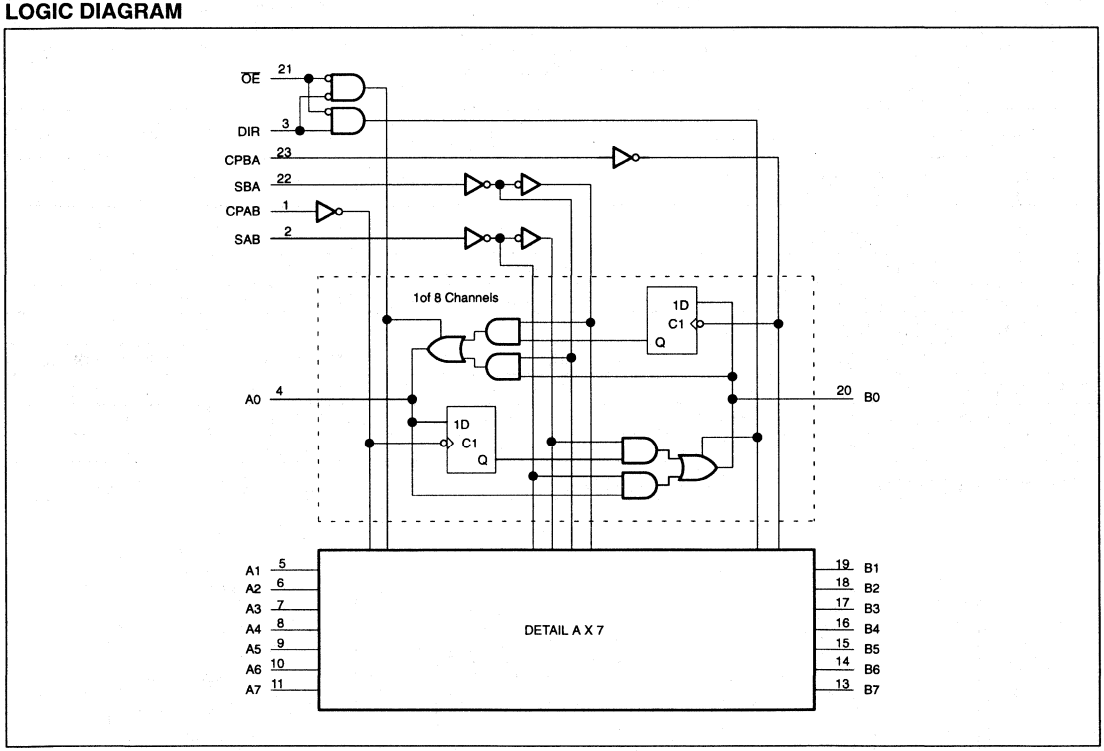
LOGIC SYMBOL (IEEE/IEC)

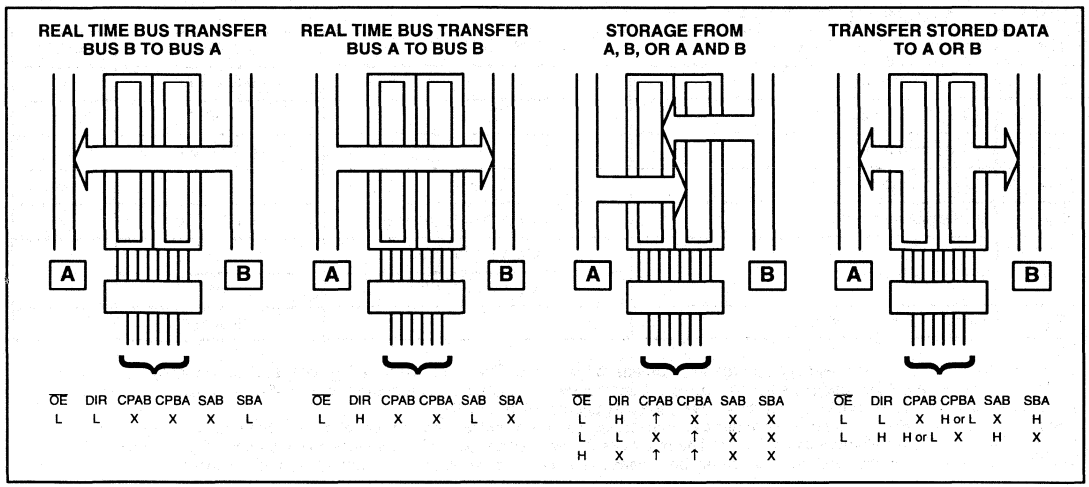


PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 23	CPAB / CPBA	A to B clock input / B to A clock input
2, 22	SAB / SBA	A to B select input / B to A select input
3	DIR	Direction control input
4, 5, 6, 7, 8, 9, 10, 11	A0 – A7	Data inputs/outputs (A side)
20, 19, 18, 17, 16, 15, 14, 13	B0 – B7	Data inputs/outputs (B side)
21	$\overline{OE}$	Output enable input (active-low)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

LOGIC DIAGRAM





FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA	An	Bn	
X	X	↑	X	X	X	Input	Unspecified output*	Store A, B unspecified
X	X	X	↑	X	X	Unspecified output*	Input	Store B, A unspecified
H H	X X	↑ H or L	↑ H or L	X X	X X	Input	Input	Store A and B data Isolation, hold storage
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time B data to A bus Stored B data to A bus
L L	H H	X H or L	X X	L H	X X	Input	Output	Real time A data to B bus Stored A data to B bus

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
* The data output function may be enabled or disabled by various signals at the $\overline{OE}$ input. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%, f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–0.9	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2	V_{CC}-0.1		V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4	2.5		
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.2		
V_{OL}	Low–level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.1	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[5]	V_{CC} = 3.6V; I_O = 1mA; V_I = GND or V_{CC}			0.13	0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		±0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			1	10	
		V_{CC} = 3.6V; V_I = 5.5V	I/O Data pins[4]		1	20	
		V_{CC} = 3.6V; V_I = V_{CC}			0.1	1	
		V_{CC} = 3.6V; V_I = 0			–1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			1	±100	µA
I_{HOLD}	Bus Hold current A or B ports	V_{CC} = 3V; V_I = 0.8V		75	150		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–150		µA
I_{EX}	Current into an ouptut in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			60	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE =Don't care			15	±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.13	0.19	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3	12	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0			0.13	0.19	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specificed voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ± 0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
f_{MAX}	Maximum clock frequency	1	150	180			MHz
t_{PLH} t_{PHL}	Propagation delay CPAB to Bn or CPBA to An	1	1.8 2.1	3.8 3.8	5.7 5.7	6.7 6.4	ns
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	2	1.3 1.0	2.8 2.7	4.7 4.6	5.4 5.3	ns
t_{PLH} t_{PHL}	Propagation delay SAB to Bn or SBA to An	2, 3	1.4 1.4	3.7 3.8	6.2 6.2	7.2 6.8	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}$ to An or Bn	5 6	1.0 1.0	4.0 4.1	5.8 6.0	7.2 7.3	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$ to An or Bn	5 6	2.3 2.2	4.3 3.8	6.5 5.8	6.9 5.9	ns
t_{PZH} t_{PZL}	Output enable time DIR to An or Bn	5 6	1.0 1.2	3.4 3.4	6.5 6.3	7.5 7.1	ns
t_{PHZ} t_{PLZ}	Output disable time DIR to An or Bn	5 6	1.7 1.5	4.1 3.5	7.2 5.8	8.1 6.3	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC SETUP REQUIREMENTS

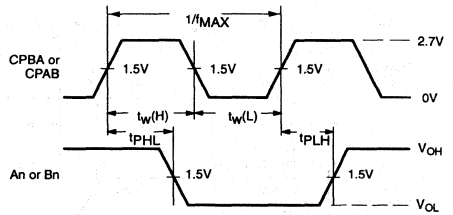
GND = 0V, t_R =2.5ns, t_F = 2.5ns, C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V± 0.3V		V_{CC} = 2.7V	
			Min	Typ	Min	
t_s(H) t_s(L)	Setup time[1] An to CPAB, Bn to CPBA	4	1.5 2.0	1.0 1.0	1.6 2.4	ns
t_h(H) t_h(L)	Hold time[1] An to CPAB, Bn to CPBA	4	0.0 0.0	–1.0 –1.0	0.0 0.0	ns
t_w(H) t_w(L)	Pulse width, High or Low CPAB or CPBA	1	3.3 3.3	1.0 2.0	3.3 3.3	ns

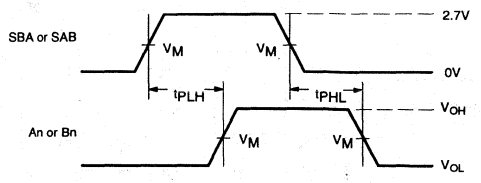
NOTE:
1. This data sheet limit may vary among suppliers.

AC WAVEFORMS

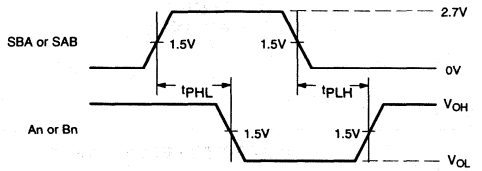
V_M = 1.5V, V_{IN} = GND to 2.7V



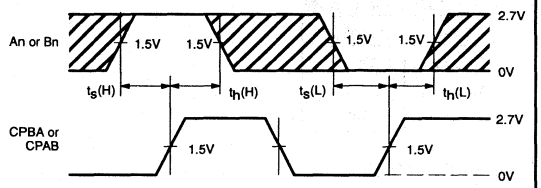
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



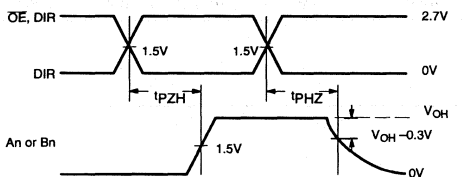
Waveform 2. Propagation Delay, SAB to Bn or SBA to An, An to Bn or Bn to An



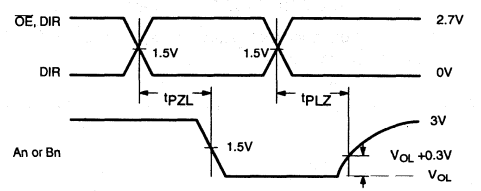
Waveform 3. Propagation Delay, SBA to An or SAB to Bn



Waveform 4. Data Setup and Hold Times



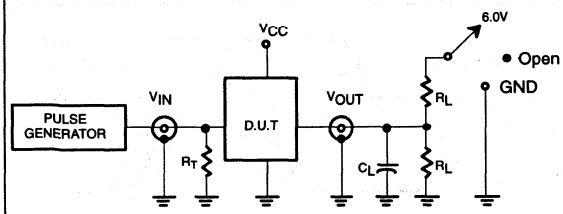
Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level



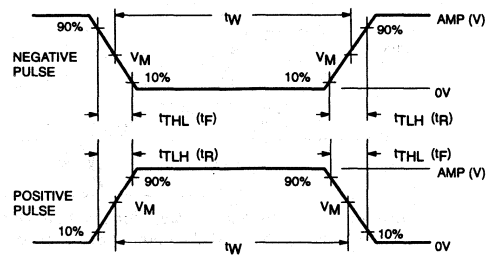
Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

3.3V ABT Octal Transceiver/register, non-inverting (3-State)

74LVT652

FEATURES

- Independent registers for A and B buses
- Multiplexed real-time and stored data
- 3-State outputs
- Output capability: +64mA/–32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Power-up 3-State
- Power-up reset
- Latch–up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT652 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device combines low static and dynamic power dissipation with high speed and high output drive.

The 74LVT652 transceiver/register consists of bus transceiver circuits with 3-State outputs, D–type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable (OEAB, $\overline{OEBA}$) and Select (SAB, SBA) pins are provided for bus management.

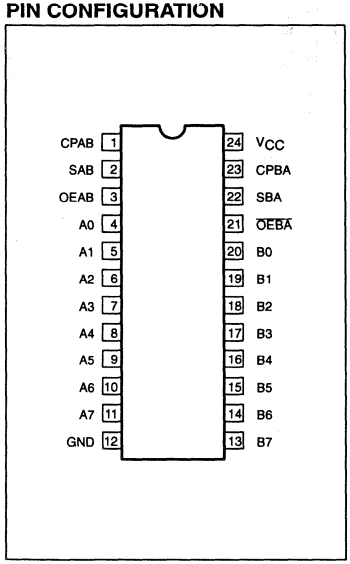
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 3.3V	2.8	ns
C_{IN}	Input capacitance	V_I = 0V or 3V	4.5	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; $V_{I/O}$ = 0V or 3V	11	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	.13	mA

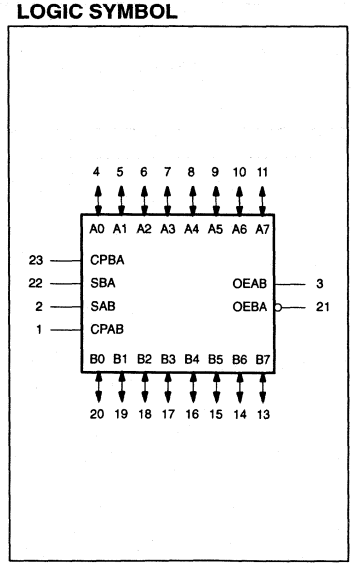
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
24-Pin Plastic Small Outline Large (300mil) (SOL)	–40°C to +85°C	74LVT652D	SOT137-1
24-Pin Plastic Shrink Small Outline (SSOP) Type II	–40°C to +85°C	74LVT652DB	SOT340-1
24-Pin Plastic Thin Shrink Small Outline (TSSOP) Type I	–40°C to +85°C	74LVT652PW	SOT355-1

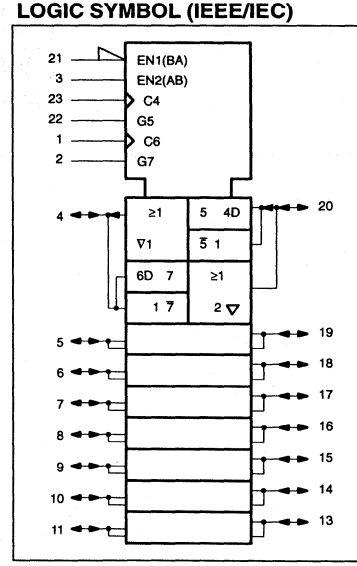
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

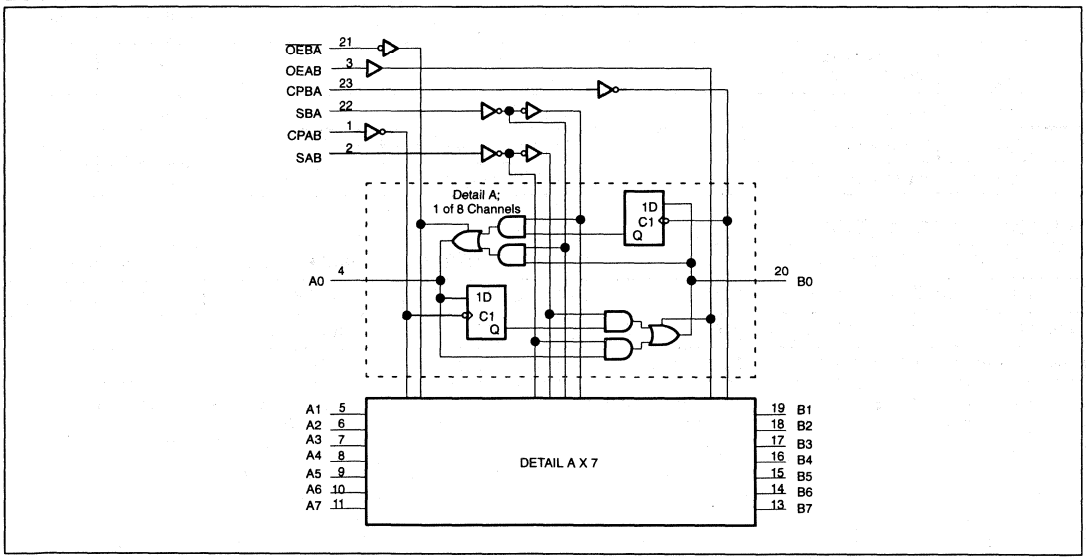


3.3V ABT Octal transceiver/register, non-inverting (3-State) 74LVT652

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 23	CPAB / CPBA	A to B clock input / B to A clock input
2, 22	SAB / SBA	A to B select input / B to A select input
3, 21	OEAB / $\overline{OEBA}$	A to B Output Enable input (active-High) / B to A Output Enable input (active-Low)
4, 5, 6, 7, 8, 9, 10, 11	A0 – A7	Data inputs/outputs (A side)
20, 19, 18, 17, 16, 15, 14, 13	B0 – B7	Data inputs/outputs (B side)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



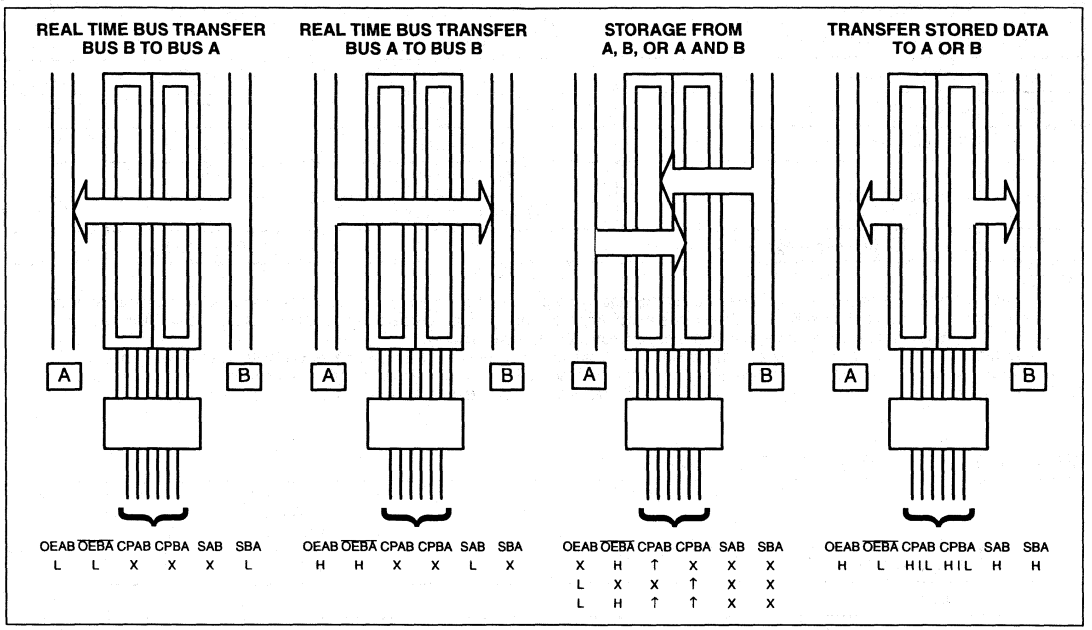
3.3V ABT Octal transceiver/register, non-inverting (3-State)

74LVT652

The following examples demonstrate the four fundamental bus-management functions that can be performed with the 74LVT652.

The select pins determine whether data is stored or transferred through the device in real time.

The output enable pins determine the direction of the data flow.



FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA	An	Bn	
L L	H H	H or L ↑	H or L ↑	X X	X X	Input	Input	Isolation Store A and B data
X H	H H	↑ ↑	H or L ↑	X **	X X	Input	Unspecified** Output*	Store A, Hold B Store A in both registers
L L	X L	H or L ↑	↑ ↑	X X	X **	Unspecified** Output*	Input	Hold A, Store B Store B in both registers
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time B data to A bus Stored B data to A bus
H H	H H	X H or L	X X	L H	X X	Input	Output	Real time A data to B bus Store A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus Stored B data to A bus

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
* The data output function may be enabled or disabled by various signals at the $\overline{OEBA}$ and OEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.
** If both Select controls (SAB and SBA) are Low, then clocks can occur simultaneously. If either Select control is High, the clocks must be staggered in order to load both registers.

ABSOLUTE MAXIMUM RATINGS[1,2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–0.9	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2	V_{CC}-0.1		V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4	2.5		
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.2		
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.1	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[5]	V_{CC} = 3.6V; I_O = 1mA; V_I = GND or V_{CC}			0.13	0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		±0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			1.0	10	
		V_{CC} = 3.6V; V_I = 5.5V	I/O Data pins[4]		1.0	20	
		V_{CC} = 3.6V; V_I = V_{CC}			0.1	1	
		V_{CC} = 3.6V; V_I = 0			–1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			1	±100	µA
I_{HOLD}	Bus Hold current A or B ports	V_{CC} = 3V; V_I = 0.8V		75	150		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–150		µA
I_{EX}	Current into an ouptut in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			60	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			15	±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.13	0.19	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3	12	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0			0.13	0.19	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specificed voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ± 0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
f_{MAX}	Maximum clock frequency	1	150	180			MHz
t_{PLH} t_{PHL}	Propagation delay CPAB to Bn or CPBA to An	1	1.8 2.0	3.7 3.7	6.0 5.7	6.9 6.4	ns
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	2	1.2 1.0	2.8 2.6	4.7 4.6	5.5 5.3	ns
t_{PLH} t_{PHL}	Propagation delay SAB to Bn or SBA to An	3	1.4 1.4	3.7 4.0	6.4 6.2	7.6 6.8	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEBA}$ to An	5 6	1.0 1.0	2.9 3.0	5.8 6.0	7.2 7.3	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEBA}$ to An	5 6	2.2 1.8	3.9 3.2	6.5 5.8	6.9 5.9	ns
t_{PZH} t_{PZL}	Output enable time OEAB to Bn	5 6	1.0 1.2	3.3 3.4	6.5 6.3	7.5 7.1	ns
t_{PHZ} t_{PLZ}	Output disable time OEAB to Bn	5 6	1.7 1.5	4.5 3.8	7.2 5.8	8.1 6.3	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC SETUP REQUIREMENTS

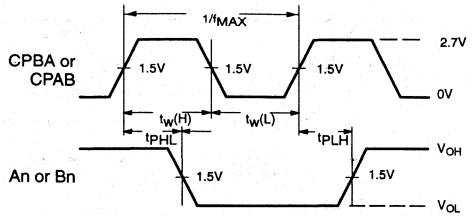
GND = 0V, t_R = 2.5ns, t_F = 2.5ns, C_L = 50pF, R_L = 500Ω, T_{amb} =40 °C to 85 °C

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = -40 to +85°C V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time [1] An to CPAB, Bn to CPBA	4	1.5 2.2	0.9 1.1		1.6 2.5		ns
t_h(H) t_h(L)	Hold time [1] An to CPAB, Bn to CPBA	4	0 0	–1.0 –1.0		0.0 0.0		ns
t_w(H) t_w(L)	Pulse width, High or Low CPAB or CPBA	1	3.3 3.3	1.0 2.0		3.3 3.3		ns

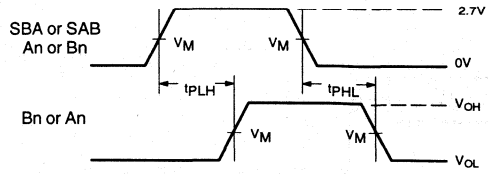
NOTE:
1. This data sheet limit may vary among suppliers.

AC WAVEFORMS

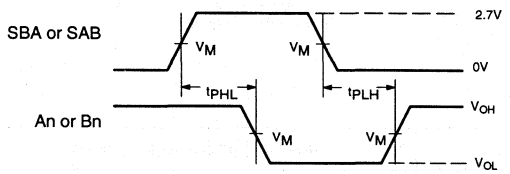
V_M = 1.5V, V_{IN} = GND to 2.7V



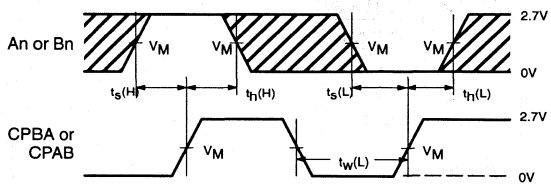
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



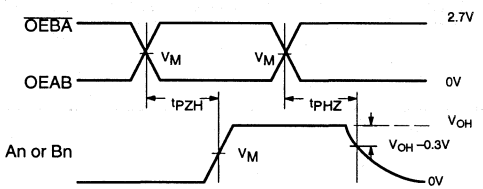
Waveform 2. Propagation Delay, An to Bn or Bn to An, SAB to Bn or SBA to An



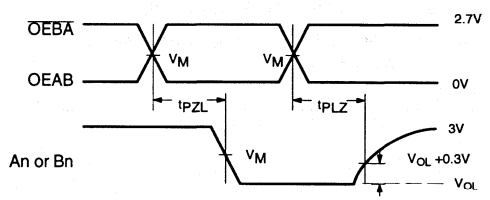
Waveform 3. Propagation Delay, SBA to An or SAB to Bn



Waveform 4. Data Setup and Hold Times



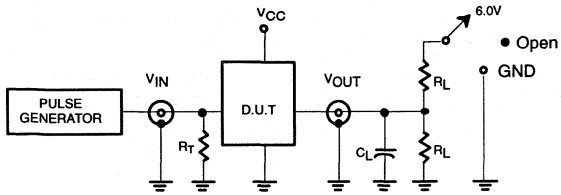
Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level



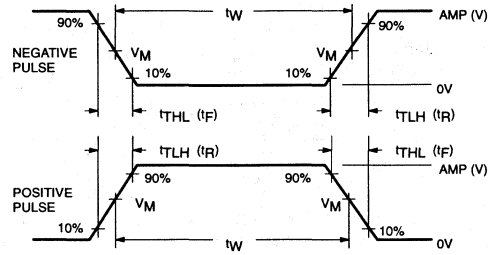
Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

3.3V ABT Octal registered transceiver (3-State) 74LVT2952

FEATURES

- 8-bit registered transceiver
- Independent registers for A and B buses
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Power-up reset
- Power-up 3-State
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT2952 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device combines low static and dynamic power dissipation with high speed and high output drive.

The 74LVT2952 device is an 8-bit registered transceiver. Two 8-bit back-to-back registers store data flowing in both directions between two bidirectional buses.

Data applied to the inputs is entered and stored on the rising edge of the Clock (CPXX) provided that the Clock Enable ($\overline{CEXX}$) is Low. The data is then present at the 3-State output buffers, but is only accessible when the Output Enable ($\overline{OEXX}$) is Low. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

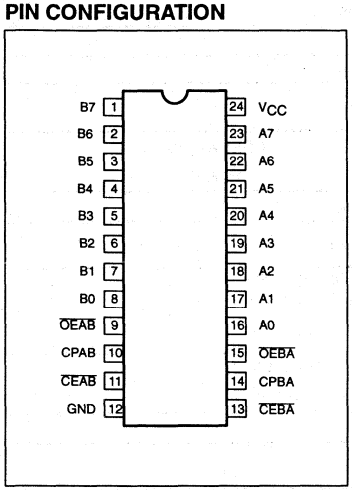
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CPBA to An or CPAB to Bn	C_L = 50pF; V_{CC} = 3.3V	3.1 3.8	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	4	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O}$ = 0V or 3.0V	8	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	0.13	mA

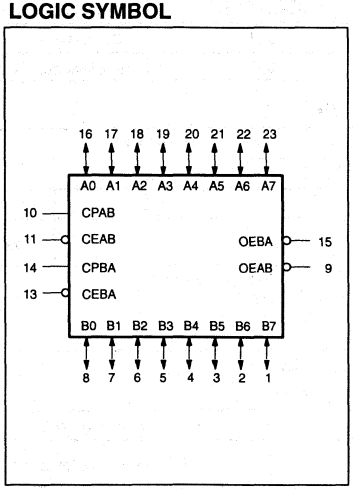
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
24-Pin Plastic Small Outline Large (300mil) (SOL)	–40°C to +85°C	74LVT2952D	SOT137-1
24-Pin Plastic Shrink Small Outline SSOP Type II	–40°C to +85°C	74LVT2952DB	SOT340-1
24-Pin Plastic Thin Small Shrink Outline TSSOP Type I	–40°C to +85°C	74LVT2952PW	SOT355-1

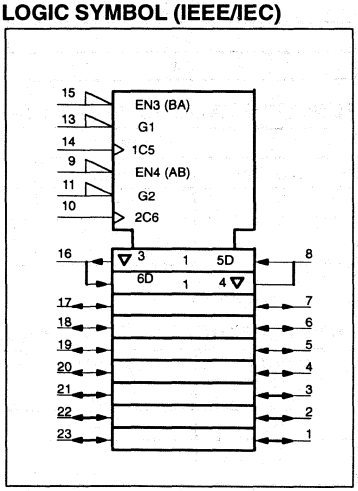
PIN CONFIGURATION



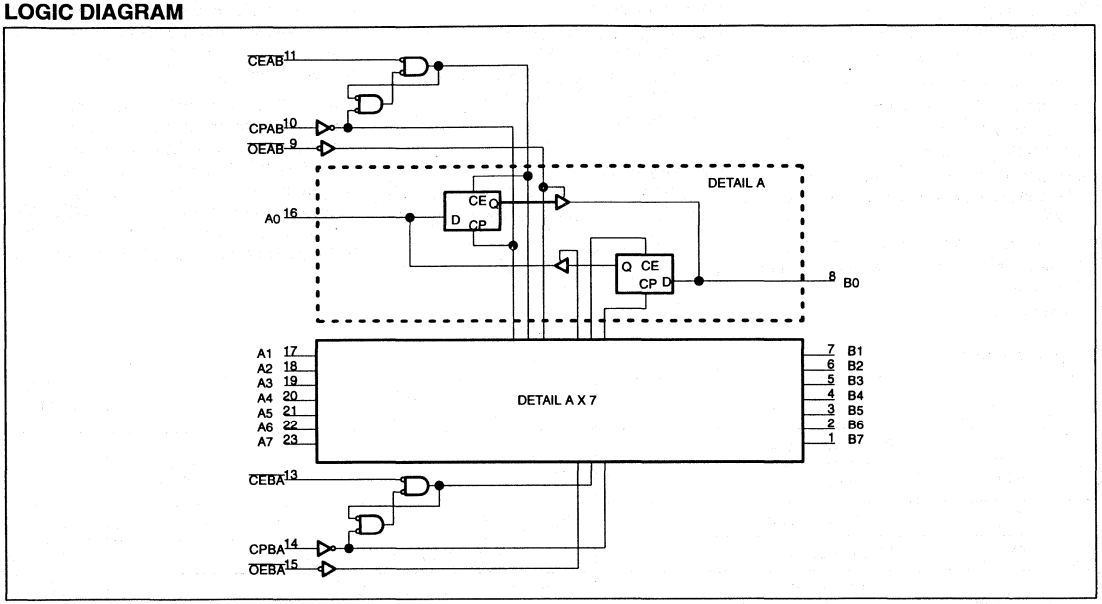
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
10, 14	CPAB / CPBA	Clock input A to B / Clock input B to A
11, 13	$\overline{CEAB}$ / $\overline{CEBA}$	Clock enable input A to B / Clock enable input B to A
16, 17, 18, 19, 20, 21, 22, 23	A0 – A7	Data inputs/outputs (A side)
8, 7, 6, 5, 4, 3, 2, 1	B0 – B7	Data outputs/outputs (B side)
9, 15	$\overline{OEAB}$ / $\overline{OEBA}$	Output enable inputs
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

FUNCTION TABLE for Register An or Bn

INPUTS			INTERNAL	OPERATING
An or Bn	CPXX	$\overline{CEXX}$	Q	MODE
X	X	H	NC	Hold data
L H	↑ ↑	L L	L H	Load data

H = High voltage level
L = Low voltage level
↑ = Low-to-High transition
X = Don't care
XX = AB or BA
NC = No change

FUNCTION TABLE for Output Enable

INPUTS	INTERNAL	An or Bn	OPERATING
$\overline{OEXX}$	Q	OUTPUTS	MODE
H	X	Z	Disable outputs
L L	L H	L H	Enable outputs

H = High voltage level
L = Low voltage level
X = Don't care
XX = AB or BA
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in High state	–64	mA
		Output in Low state	128	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%, f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–0.9	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2	V_{CC}–0.1		V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4	2.5		
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.2		
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.1	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[5]	V_{CC} = 3.6V; I_O = 1mA; V_I = GND or V_{CC}			0.13	0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		±0.1	±1.0	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			1	10	
		V_{CC} = 3.6V; V_I = 5.5V	I/O Data pins[4]		1	20	
		V_{CC} = 3.6V; V_I = V_{CC}			0.1	1.0	
		V_{CC} = 3.6V; V_I = 0			–1	-5.0	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			1	±100	µA
I_{HOLD}	Bus Hold current A or B outputs	V_{CC} = 3.0V; V_I = 0.8V		75	150		µA
		V_{CC} = 3.0V; V_I = 2.0V		–75	–150		µA
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			60	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			±1	±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.13	0.19	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3	12	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0			0.13	0.19	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC} = 0.6V, Other inputs at V_{CC} or GND			0.3	1.5	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at V_{CC} = 0.6V.
3. This parameter is valid for any V_{CC} between 0V and 1.3V with a transition time of up to 10msec. From V_{CC} = 1.3V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ± 0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
f_{MAX}	Maximum clock frequency	1	150	200			MHz
t_{PLH} t_{PHL}	Propagation delay CPBA to An, CPAB to Bn	1	1.3 1.8	3.1 3.8	6.1 6.0	7.1 6.9	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	3 4	1.0 1.2	3.4 3.6	5.6 6.5	6.7 8.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	3 4	1.0 1.6	3.7 3.4	6.3 5.1	6.9 5.3	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

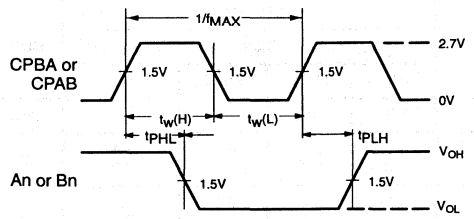
AC SETUP

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

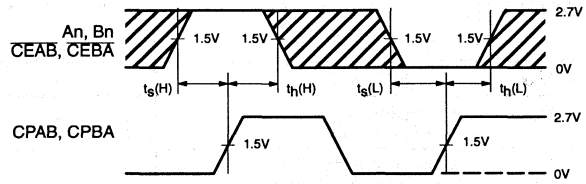
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V ± 0.3V		V_{CC} = 2.7V	
			MIN	TYP[1]	MIN	
t_s(H) t_s(L)	Setup time An to CPAB or Bn to CPBA	2	2.5 2.5	1 1	2.8 3.0	ns
t_n(H) t_n(L)	Hold time An to CPAB ro Bn to CPBA	2	1.5 2.5	–0.5 –0.5	0.7 2.6	ns
t_s(H) t_s(L)	Setup time $\overline{CEAB}$ to CPAB or $\overline{CEBA}$ to CPBA	2	0.9 2.4	0.3 –0.3	0.8 2.7	ns
t_n(H) t_n(L)	Hold time $\overline{CEAB}$ to CPAB or $\overline{CEBA}$ to CPBA	2	1.5 2.5	0.3 0	0.7 2.6	ns
t_W(H) t_W(L)	CPAB or CPBA pulse width High or Low	1	3.3 3.3	1 1	3.3 3.3	ns

AC WAVEFORMS

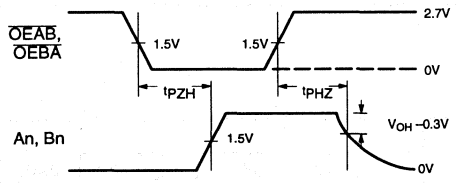
V_M = 1.5V, V_{IN} = GND to 2.7V



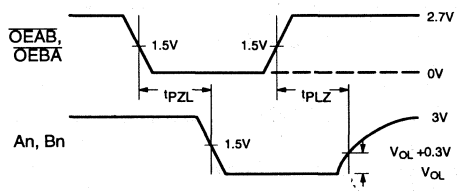
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Data Setup and Hold Times

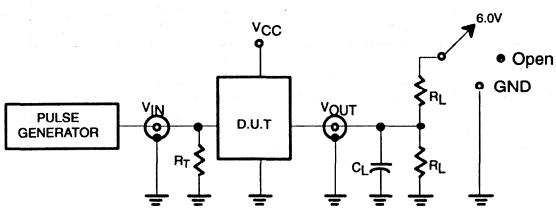


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

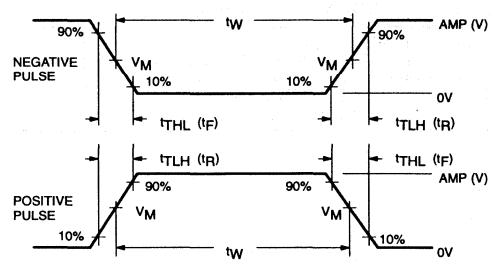


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

DEVICE DATA

LVT16

3.3V ABT 16-Bit Inverting buffers/drivers (3-State) 74LVT16240A

FEATURES

- 16-bit bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT16240A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is an inverting 16-bit buffer that is ideal for driving bus lines. The device features four Output Enables ($1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$), each controlling four of the 3-State outputs.

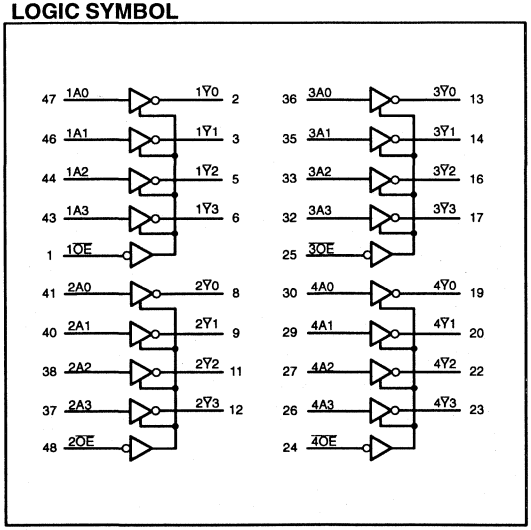
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to n$\overline{Y}$x	C_L = 50pF; V_{CC} = 3.3V		ns
C_{IN}	Input capacitance n$\overline{OE}$	V_I = 0V or 3.0V	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or 3.0V	10	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	100	µA

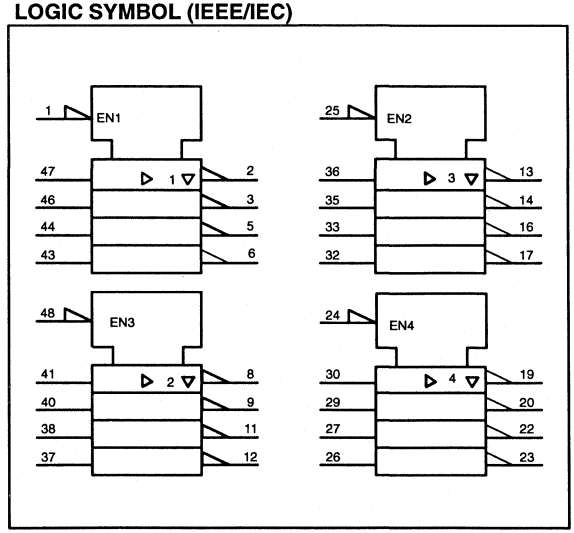
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
48-Pin Plastic Shrink Small Outline (SSOP) Type III	–40°C to +85°C	74LVT16240ADL	SOT370-1
48-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	–40°C to +85°C	74LVT16240ADGG	SOT362-1

LOGIC SYMBOL

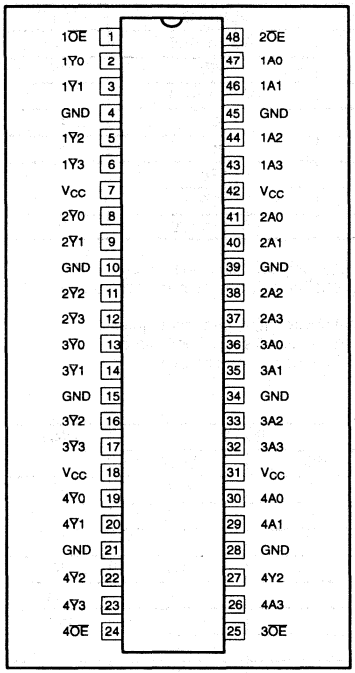


LOGIC SYMBOL (IEEE/IEC)



3.3V ABT 16-Bit Inverting buffers/drivers (3-State) 74LVT16240A

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1A0–1A3 2A0–2A3 3A0–3A3 4A0–4A3	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	1$\overline{Y}$0–1$\overline{Y}$3 2$\overline{Y}$0–2$\overline{Y}$3 3$\overline{Y}$0–3$\overline{Y}$3 4$\overline{Y}$0–4$\overline{Y}$3	Data outputs
1, 48, 25, 24	1$\overline{OE}$, 2$\overline{OE}$, 3$\overline{OE}$, 4$\overline{OE}$	Output enables
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

FUNCTION TABLE

Inputs		Outputs
n$\overline{OE}$	nAx	n$\overline{Y}$x
L	L	H
L	H	L
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High Impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1,2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA				1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2			V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4			
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0			
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA				0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA				0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA				0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA				0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA				0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins			±1.0	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V				10	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]			1	
		V_{CC} = 3.6V; V_I = 0				–5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V				±100	µA
I_{HOLD}	Bus Hold current A inputs	V_{CC} = 3V; V_I = 0.8V		75			µA
		V_{CC} = 3V; V_I = 2.0V		–75			µA
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V				125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$ = Don't care				±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IL} or V_{ZH}				5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{ZH}				–5	
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0				0.12	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0				5.0	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0				0.12	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND				0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.

AC CHARACTERISTICS

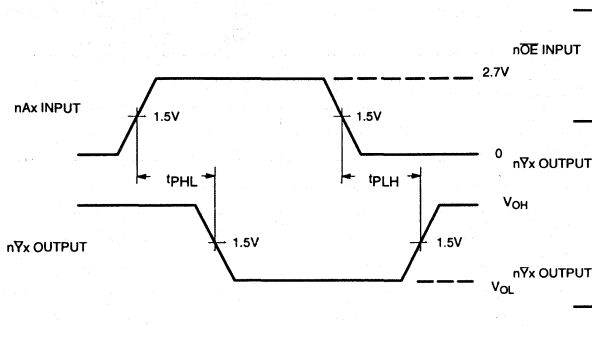
GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS V_{CC} = 3.3V ±0.3V MIN	TYP[1]	MAX	V_{CC} = 2.7V MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to n$\overline{Y}$x	1					ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2					ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2					ns

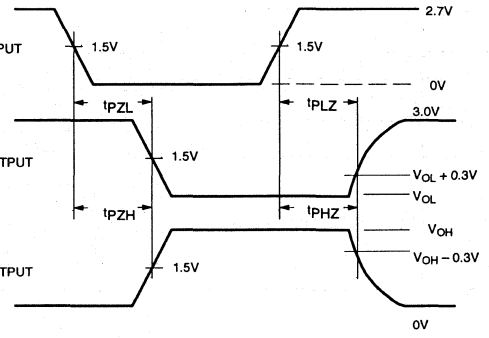
NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 2.7V

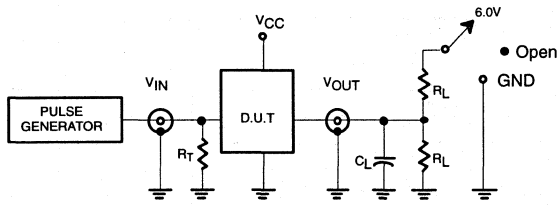


Waveform 1. Waveforms Showing the Input (nAx) to Output (nȲx) Propagation Delays

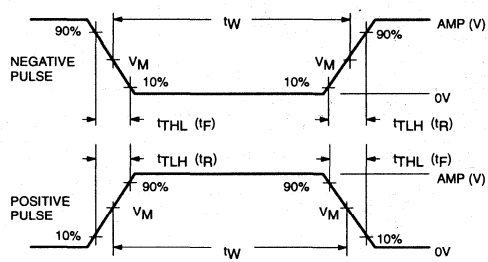


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT16	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

3.3V ABT 16-Bit Inverting buffers/drivers with 30Ω termination resistors (3-State)

74LVT16240A-1

FEATURES

- 16–bit bus interface
- 3-State buffers
- Output capability: +12mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Outputs include series resistance of 30Ω making external termination resistors unnecessary
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT16240A-1 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is an inverting 16-bit bufferthat is ideal for driving bus lines. The device features four Output Enables ($1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$), each controlling four of the 3-State outputs.

The LVT16240A-1 is designed with 30Ω series resistance in both the High and Low states of the output. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus receivers/transmitters.

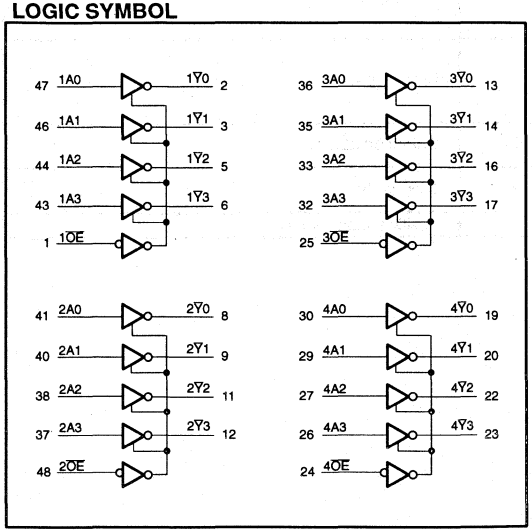
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	C_L = 50pF; V_{CC} = 3.3V		ns
C_{IN}	Input capacitance $n\overline{OE}$	V_I = 0V or 3.0V	4	pF
C_{OUT}	Output capacitance	V_O = 0V or 3.0V	10	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	100	µA

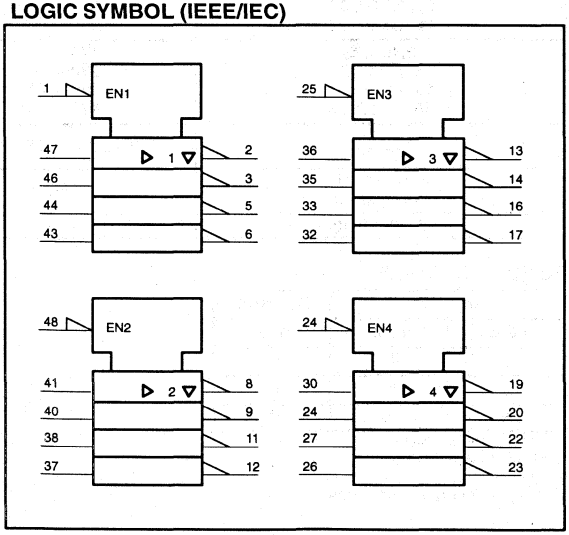
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
48-Pin Plastic Shrink Small Outline (SSOP) Type III	–40°C to +85°C	74LVT16240A-1DL	SOT370-1
48-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	–40°C to +85°C	74LVT16240A-1DGG	SOT362-1

LOGIC SYMBOL

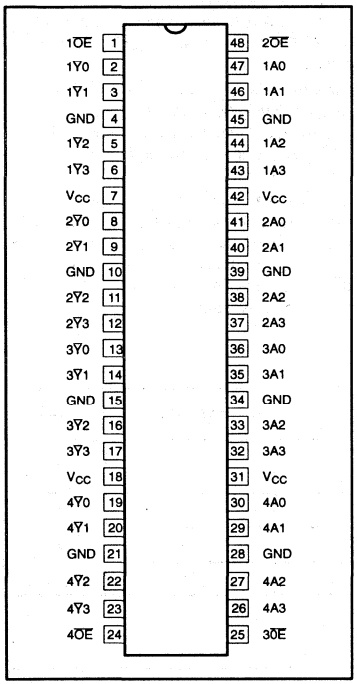


LOGIC SYMBOL (IEEE/IEC)



3.3V ABT 16-Bit Inverting buffers/drivers with 30Ω termination resistors (3-State) — 74LVT16240A-1

PIN CONFIGURATION



PIN DESCRIPTION

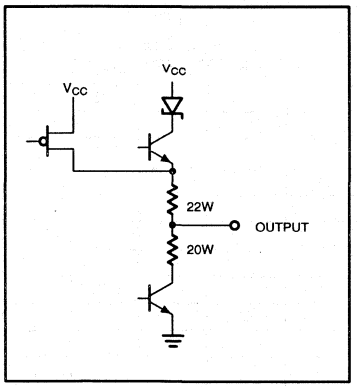
PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1A0 – 1A3 2A0 – 2A3 3A0 – 3A3 4A0 – 4A3	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	1$\overline{Y}$0 – 1$\overline{Y}$3 2$\overline{Y}$0 – 2$\overline{Y}$3 3$\overline{Y}$0 – 3$\overline{Y}$3 4$\overline{Y}$0 – 4$\overline{Y}$3	Data outputs
1, 48 25, 24	1$\overline{OE}$, 2$\overline{OE}$, 3$\overline{OE}$, 4$\overline{OE}$	Output ernables
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

FUNCTION TABLE

Inputs		Outputs
n$\overline{OE}$	nAx	n$\overline{Y}$x
L	L	H
L	H	L
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High Impedance "off" state

SCHEMATIC OF EACH OUTPUT



ABSOLUTE MAXIMUM RATINGS[1,2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
2. The performance capability of a high–performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free–air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA				1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0V; I_{OH} = –12mA		2.0			V
V_{OL}	Low–level output voltage	V_{CC} = 3.0V; I_{OL} = 12mA				0.8	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins			±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V				10	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]			1	
		V_{CC} = 3.6V; V_I = 0				–5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V				±100	µA
I_{HOLD}	Bus Hold current A outputs	V_{CC} = 3.0V; V_I = 0.8V		75			µA
		V_{CC} = 3.0V; V_I = 2.0V		–75			
I_{EX}	Current into an ouptut in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V				125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care				±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IL} or V_{IH}				5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}				–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0				0.12	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0				5	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0				0.12	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND				0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specificed voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.

AC CHARACTERISTICS

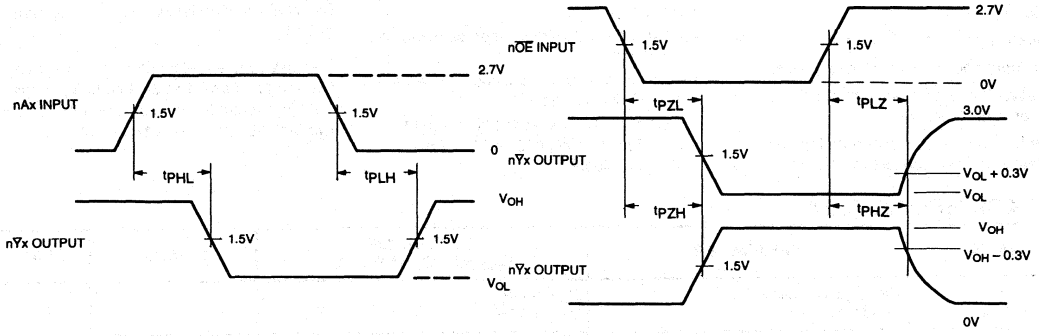
GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS V_{CC} = 3.3V ±0.3V MIN	TYP[1]	MAX	V_{CC} = 2.7V MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	1					ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2					ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2					ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

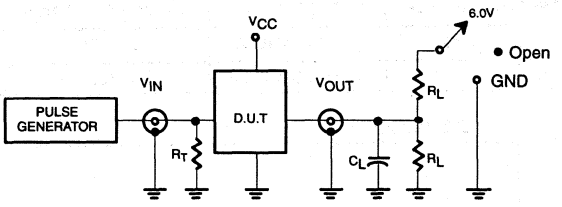
V_M = 1.5V, V_{IN} = GND to 2.7V



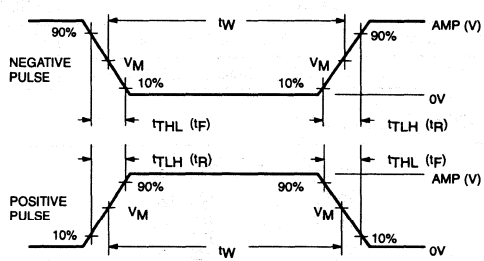
Waveform 1. Waveforms Showing the Input (nAx) to Output (nȲx) Propagation Delays

Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT16	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

3.3V ABT 16-Bit buffers/drivers (3-State) 74LVT16244B

FEATURES

- 16-bit bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT16244B is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is a 16-bit buffer and line driver featuring non-inverting 3-State bus outputs. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer.

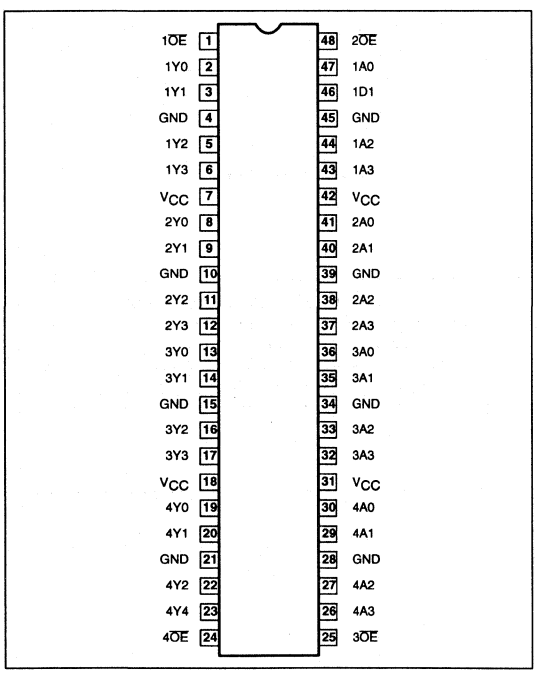
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	C_L = 50pF; V_{CC} = 3.3V		ns
C_{IN}	Input capacitance n$\overline{OE}$	V_I = 0V or 3.0V	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or 3.0V	10	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	100	µA

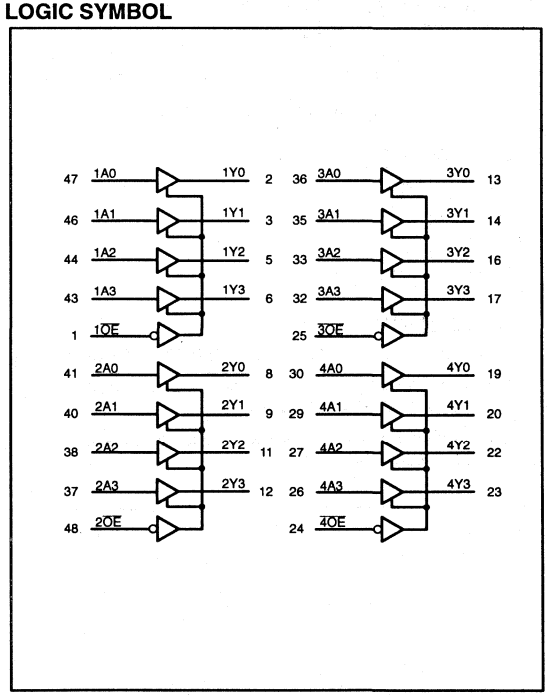
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
48-Pin Plastic Shrink Small Outline (SSOP) Type III	–40°C to +85°C	74LVT16244BDL	SOT370-1
48-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	–40°C to +85°C	74LVT16244BDGG	SOT362-1

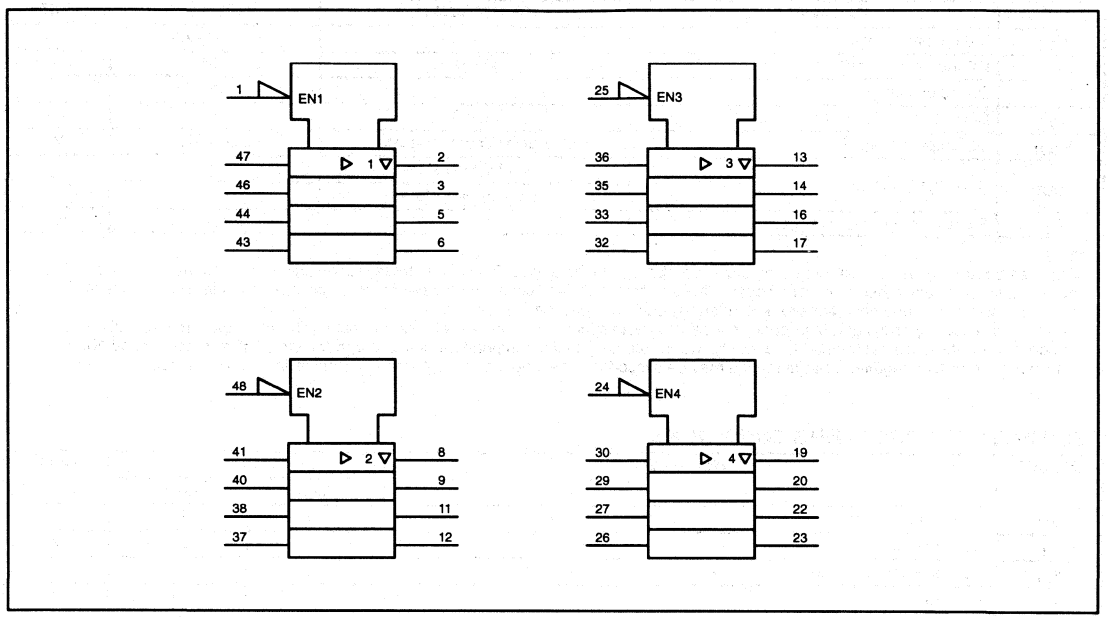
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43 41, 40, 38, 37 36, 35, 33, 32 30, 29, 27, 26	1A0 – 1A3, 2A0 – 2A3, 3A0 – 3A3, 4A0 – 4A3	Data inputs
2, 3, 5, 6 8, 9, 11, 12 13, 14, 16, 17 19, 20, 22, 23	1Y0 – 1Y3, 2Y0 – 2Y3, 3Y0 – 3Y3, 4Y0 – 4Y3	Data outputs
1, 48 25, 24	$1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$	Output enables
4, 10, 15, 21 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		OUTPUTS
$n\overline{OE}$	nAx	nYx
L	L	L
L	H	H
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High Impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1,2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA				–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC} –0.2			V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4			
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0			
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA				0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA				0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA				0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA				0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA				0.55	
		V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins			±1.0	µA
I_I	Input leakage current	V_{CC} = 0 or 3.6V; V_I = 5.5V				10	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]			1	
		V_{CC} = 3.6V; V_I = 0				–5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V				±100	µA
I_{HOLD}	Bus Hold current A inputs	V_{CC} = 3V; V_I = 0.8V		75			µA
		V_{CC} = 3V; V_I = 2.0V		–75			µA
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V				125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care				±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IL} or V_{IH}				5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}				–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0				0.12	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0				5.0	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0				0.12	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND				0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.

AC CHARACTERISTICS

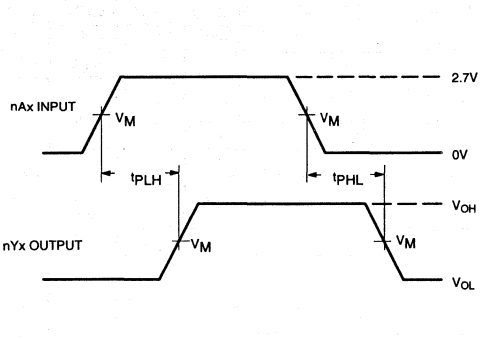
GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS V_{CC} = 3.3V ±0.3V MIN	TYP[1]	MAX	V_{CC} = 2.7V MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	1					ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2					ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2					ns

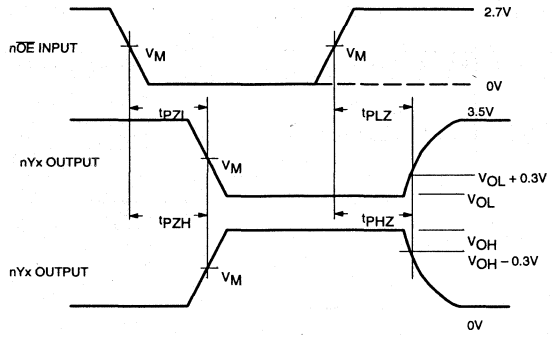
NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

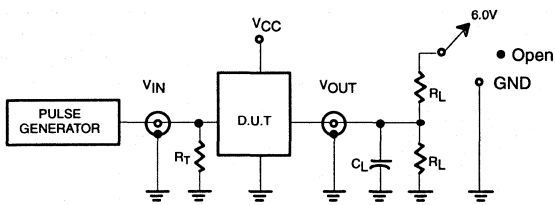


Waveform 1. Waveforms Showing the Input (nAx) to Output (nYx) Propagation Delays

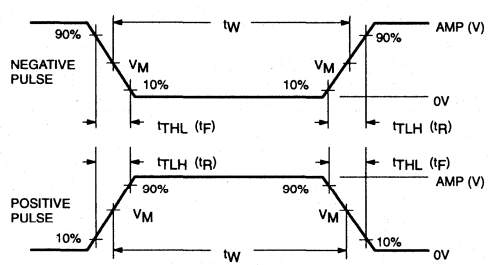


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT16	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

3.3V ABT 16-Bit buffers/drivers with 30Ω termination resistors(3-State)

74LVT16244B-1

FEATURES

- 16-bit bus interface
- 3-State buffers
- Output capability: +12mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Outputs include series resistance of 30Ω making external terminating resistors unnecessary
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT16244B-1 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

The LVT16244B-1 is designed with 30Ω series resistance in both the High and Low states of the output. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus receivers/transmitters.

This device is a 16-bit buffer and line driver featuring non-inverting 3-State bus outputs. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	C_L = 50pF; V_{CC} = 3.3V		ns
C_{IN}	Input capacitance $n\overline{OE}$	V_I = 0V or 3.0V	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or 3.0V	10	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	100	µA

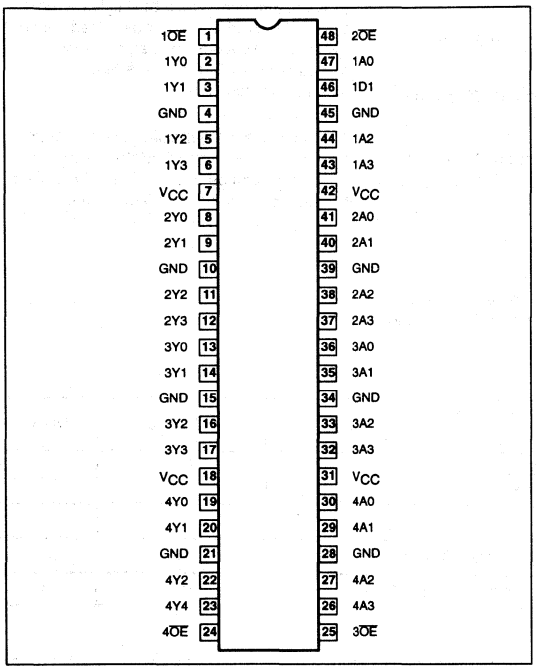
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
48-Pin Plastic Shrink Small Outline (SSOP) Type III	–40°C to +85°C	74LVT16244B-1DL	SOT370-1
48-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	–40°C to +85°C	74LVT16244B-1DGG	SOT362-1

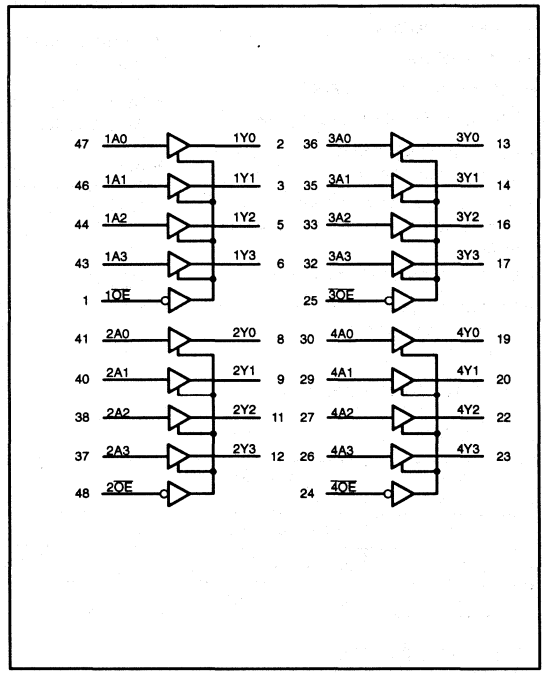
3.3V ABT 16-Bit buffers/drivers with 30Ω termination resistors(3-State)

74LVT16244B-1

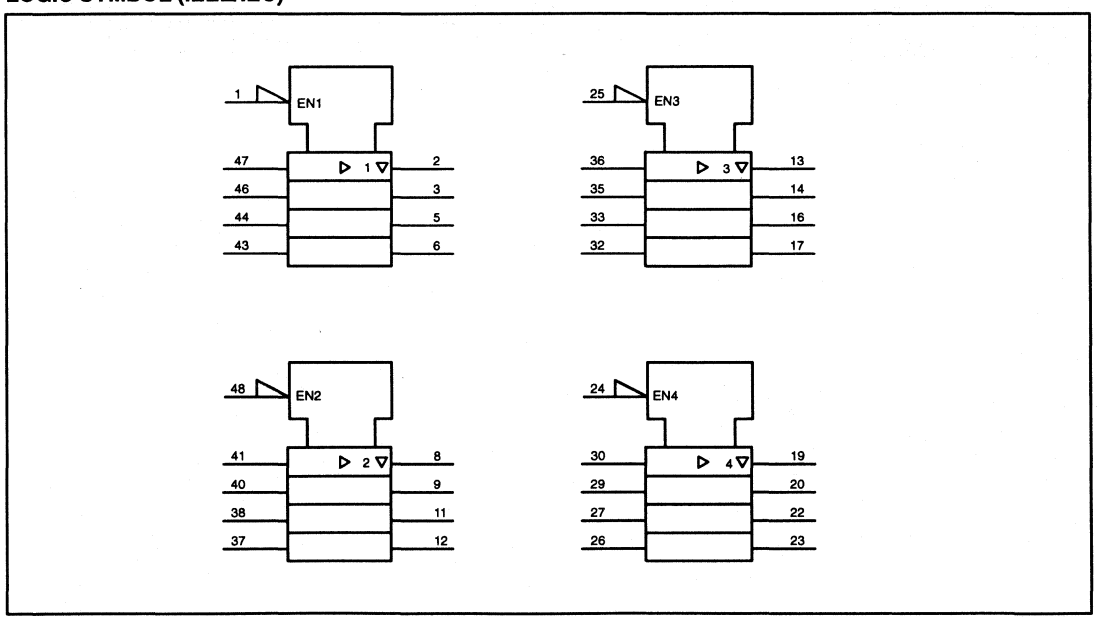
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



3.3V ABT 16-Bit buffers/drivers with 30Ω termination resistors(3-State)

74LVT16244B-1

PIN DESCRIPTION

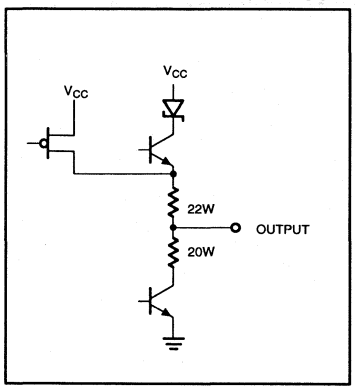
PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43 41, 40, 38, 37 36, 35, 33, 32 30, 29, 27, 26	1A0 – 1A3, 2A0 – 2A3, 3A0 – 3A3, 4A0 – 4A3	Data inputs
2, 3, 5, 6 8, 9, 11, 12 13, 14, 16, 17 19, 20, 22, 23	1Y0 – 1Y3, 2Y0 – 2Y3, 3Y0 – 3Y3, 4Y0 – 4Y3	Data outputs
1, 48 25, 24	$1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$	Output enables
4, 10, 15, 21 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		OUTPUTS
$n\overline{OE}$	nAx	nYx
L	L	L
L	H	H
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High Impedance "off" state

SCHEMATIC OF EACH OUTPUT



ABSOLUTE MAXIMUM RATINGS[1,2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA				–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0V; I_{OH} = –32mA		2.0			V
V_{OL}	Low-level output voltage	V_{CC} = 3.0V; I_{OL} = 12mA				0.8	V
		V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins			±1.0	µA
I_I	Input leakage current	V_{CC} = 0 or 3.6V; V_I = 5.5V				10	µA
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]			1	µA
		V_{CC} = 3.6V; V_I = 0	Data pins[4]			–5	µA
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V				±100	µA
I_{HOLD}	Bus Hold current A inputs	V_{CC} = 3V; V_I = 0.8V		75			µA
		V_{CC} = 3V; V_I = 2.0V		–75			µA
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V				125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care				±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IL} or V_{IH}				5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}				–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0				0.12	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0				5.0	mA
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0				0.12	mA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND				0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.

AC CHARACTERISTICS

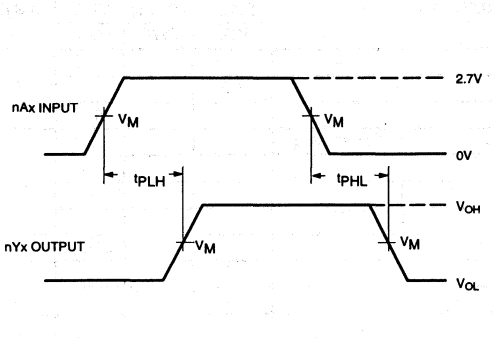
GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS V_{CC} = 3.3V ±0.3V MIN	TYP[1]	MAX	V_{CC} = 2.7V MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	1					ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2					ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2					ns

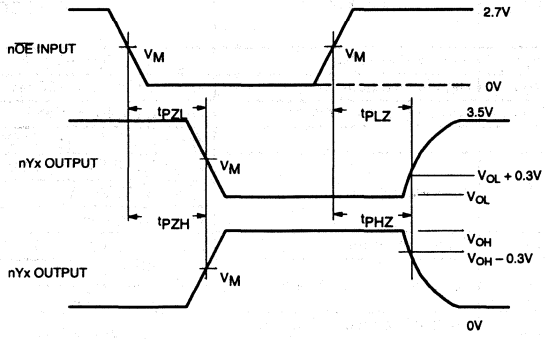
NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

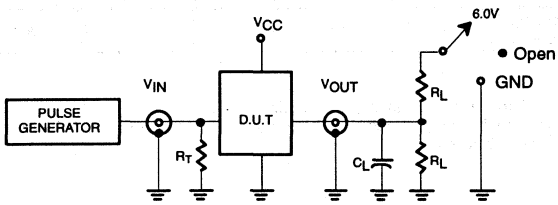


Waveform 1. Waveforms Showing the Input (nAx) to Output (nYx) Propagation Delays

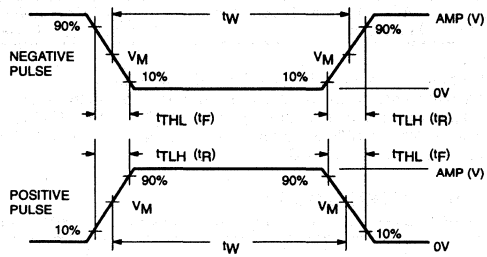


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT16	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

3.3V ABT 16–bit transceiver (3-State) 74LVT16245B

FEATURES

- 16-bit bidirectional bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT16245B is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is an 16-bit transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an Output Enable ($\overline{OE}$) input for easy cascading and a Direction (DIR) input for direction control.

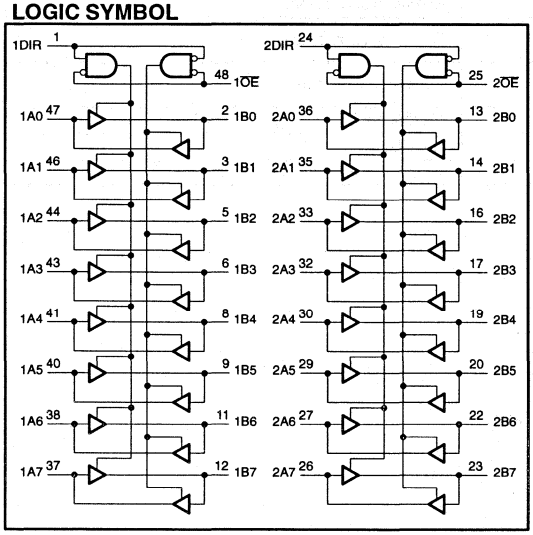
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	C_L = 50pF; V_{CC} = 3.3V	1.9	ns
C_{IN}	Input capacitance DIR, $\overline{OE}$	V_I = 0V or 3.0V	4	pF
$C_{I/O}$	I/O pin capacitance	$V_{I/O}$ = 0V or 3.0V	10	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	100	µA

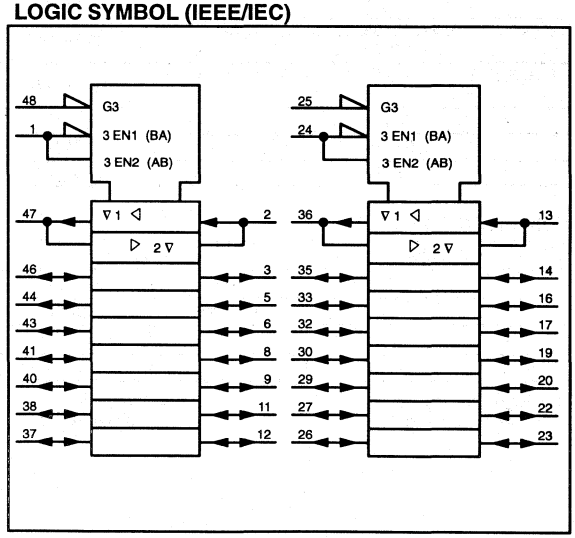
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
48-Pin Plastic Shrink Small Outline (SSOP) Type III	–40°C to +85°C	74LVT16245BDL	SOT370-1
48-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	–40°C to +85°C	74LVT16245BDGG	SOT362-1

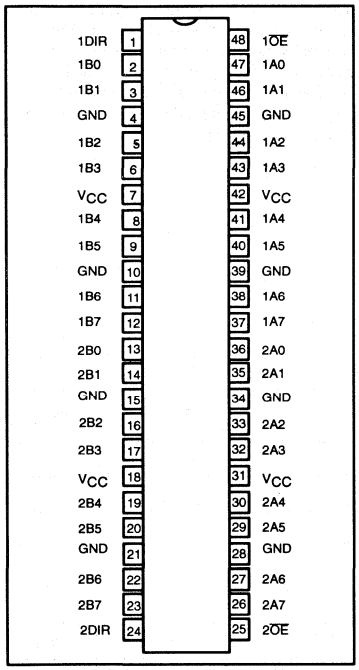
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 24	nDIR	Direction control input
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	nA0 – nA7	Data inputs/outputs (A side)
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	nB0 – nB7	Data inputs/outputs (B side)
25, 48	$n\overline{OE}$	Output enable input (active-Low)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

FUNCTION TABLE

Inputs		Inputs/Outputs	
$n\overline{OE}$	nDIR	nAx	nBx
L	L	nAx = nBx	Inputs
L	H	Inputs	nBx = nAx
H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High Impedence "off" state

ABSOLUTE MAXIMUM RATINGS[1,2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:

2. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
3. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
4. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2	V_{CC}		V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4	2.5		
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.3		
V_{OL}	Low–level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = 5.5V	I/O Data pins[4]		0.1	20	
		V_{CC} = 3.6V; V_I = V_{CC}			0.5	10	
		V_{CC} = 3.6V; V_I = 0			0.1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current A or B outputs	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–140		µA
I_{EX}	Current into an ouptut in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			75	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			40	±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.1	0.12	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			4.7	6	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0			0.1	0.12	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND			0.01	0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specificed voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.

AC CHARACTERISTICS

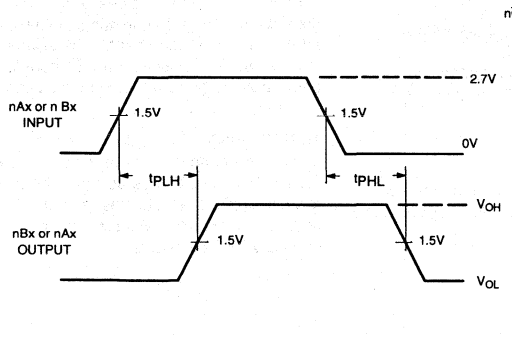
GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS V_{CC} = 3.3V +0.3V MIN	TYP[1]	MAX	V_{CC} = 2.7V MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	1	1.0 1.0	1.9 1.7	3.3 3.3	3.5 3.5	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.0 1.0	2.8 2.8	4.5 4.1	5.3 5.1	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2	1.5 1.5	3.2 3.0	5.1 4.6	5.7 4.6	ns

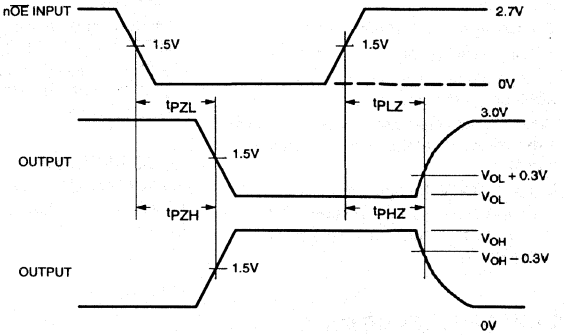
NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 2.7V

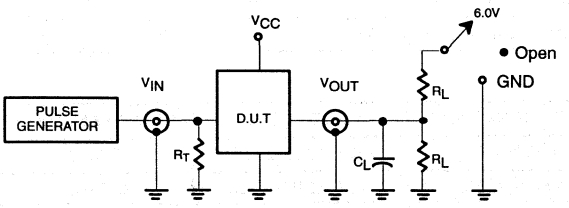


Waveform 1. Waveforms Showing the Input to Output Propagation Delays

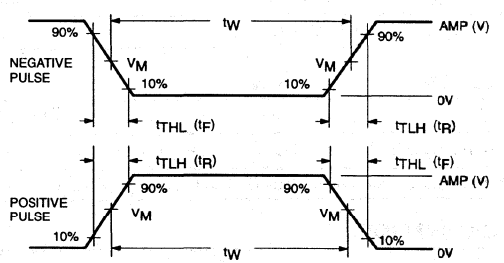


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT16	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

3.3V ABT 16–bit transceiver with 30Ω termination resistors (3-State)

74LVT16245B-1

FEATURES

- 16-bit bidirectional bus interface
- 3-State buffers
- Output capability: +12mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Outputs include series resistance of 30Ω making external termination resistors unnecessary
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT16245B-1 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is a 16-bit transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an Output Enable ($n\overline{OE}$) input for easy cascading and a Direction (nDIR) input for direction control.

The LVT16245B-1 is designed with 30Ω series resistance in both the High and Low states of the output. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus transceivers/transmitters.

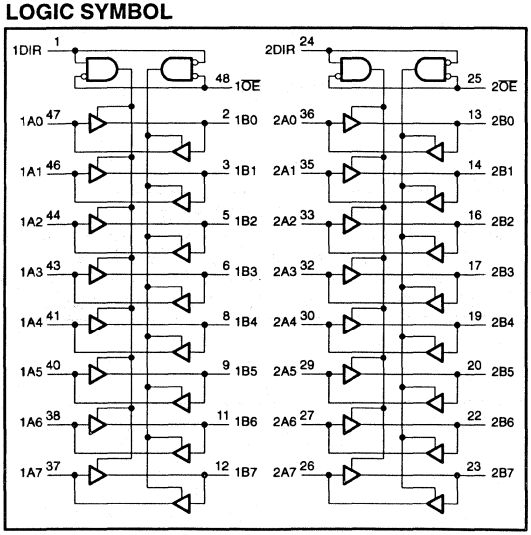
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	C_L = 50pF; V_{CC} = 3.3V		ns
C_{IN}	Input capacitance DIR, $\overline{OE}$	V_I = 0V or 3.0V	4	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O}$ = 0V or 3.0V	10	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	100	µA

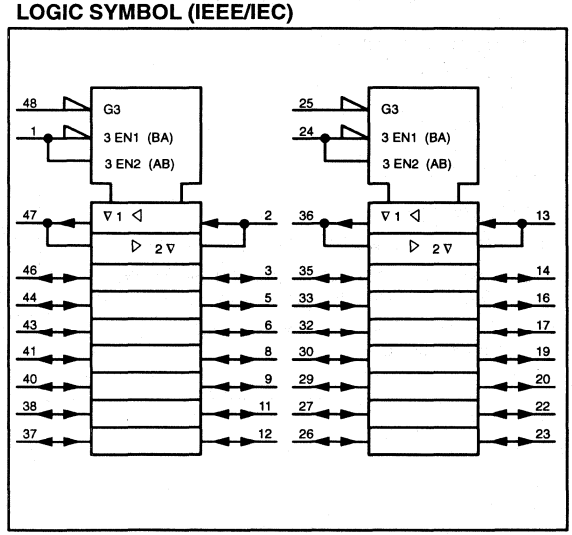
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
48-Pin Plastic Shrink Small Outline (SSOP) Type III	–40°C to +85°C	74LVT16245B-1DL	SOT370-1
48-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	–40°C to +85°C	74LVT16245B-1DGG	SOT362-1

LOGIC SYMBOL



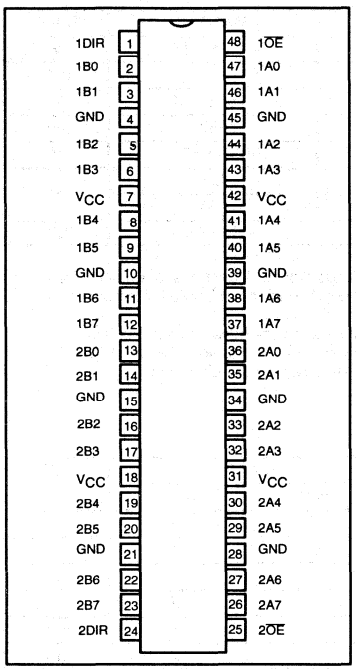
LOGIC SYMBOL (IEEE/IEC)



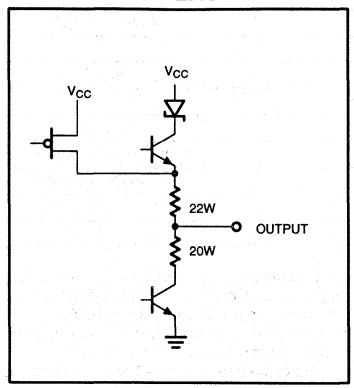
3.3V ABT 16–bit transceiver with 30Ω termination resistors (3-State)

74LVT16245B-1

PIN CONFIGURATION



SCHEMATIC OF EACH OUTPUT



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 24	nDIR	Direction control input
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	nA0 – nA7	Data inputs/outputs (A side)
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	nB0 – nB7	Data inputs/outputs (B side)
25, 48	$\overline{nOE}$	Output enable input (active-Low)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

FUNCTION TABLE

Inputs		Inputs/Outputs	
$\overline{nOE}$	nDIR	nAx	nBx
L	L	nAx = nBx	Inputs
L	H	Inputs	nBx = nAx
H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High Impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1,2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:

2. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
3. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
4. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA				–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 3.0V; I_{OH} = –12mA		2.0			V
V_{OL}	Low-level output voltage	V_{CC} = 3.0V; I_{OL} = 12mA				0.8	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins			±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V	Control pins			10	µA
		V_{CC} = 3.6V; V_I = V_{CC}	I/O Data pins[4]			10	µA
		V_{CC} = 3.6V; V_I = 0	I/O Data pins[4]			-5	µA
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V				±100	µA
I_{HOLD}	Bus Hold current A or B outputs	V_{CC} = 3V; V_I = 0.8V		75			µA
		V_{CC} = 3V; V_I = 2.0V		–75			µA
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V				125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care				±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0				0.12	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0				5	mA
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0				0.12	mA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND				0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for t_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.

AC CHARACTERISTICS

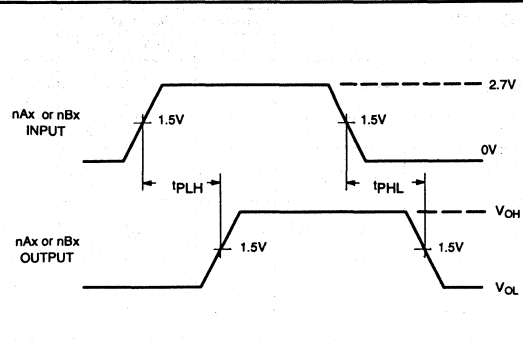
GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to bBx or bBx to nAx	1					ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2					ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2					ns

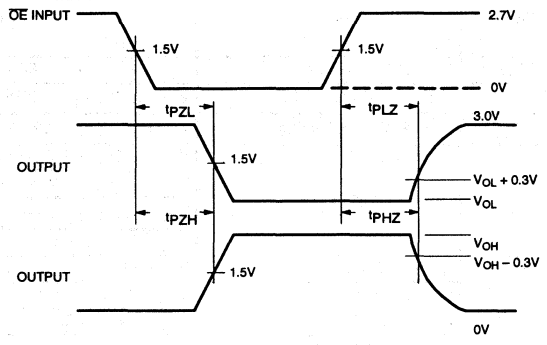
NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 2.7V

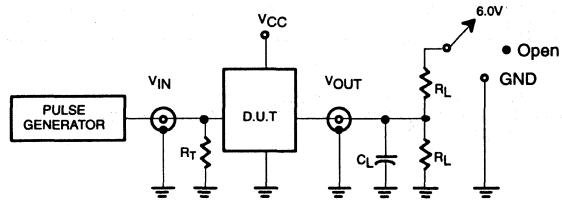


Waveform 1. Waveforms Showing the Input to Output Propagation Delays

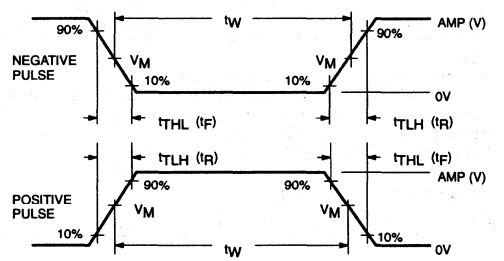


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT16	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

3.3V ABT 16–bit D-type flip-flop

74LVT16273A

FEATURES

- 16-bit D-type edge triggered flip-flops
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT16273A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This part is a 16-bit edge triggered D-type flip-flop with non-inverting high drive outputs. This device can be used as two 8-bit flip-flops or one 16-bit flip-flop. When the clock (CP) goes High, the data on the D inputs is stored and the Q outputs display the stored data.

This device also features a master reset ($\overline{MR}$) that resets all flip-flops to the Low state when $\overline{MR}$ is set to the Low state.

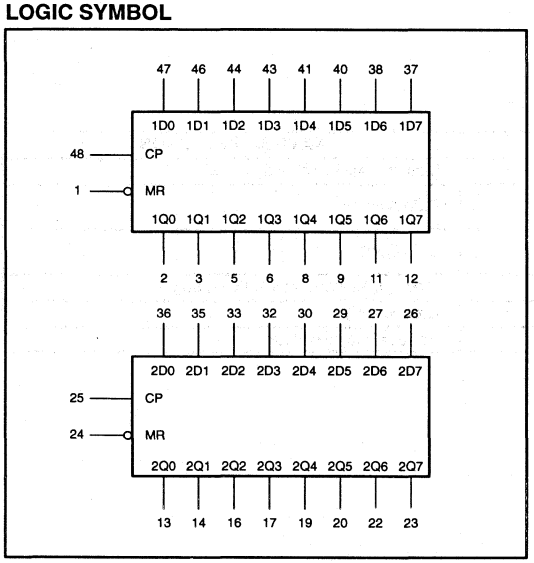
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 3.3V		ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	4	pF
I_{CCH}	Total supply current	Outputs High; V_{CC} = 3.6V	0.13	mA

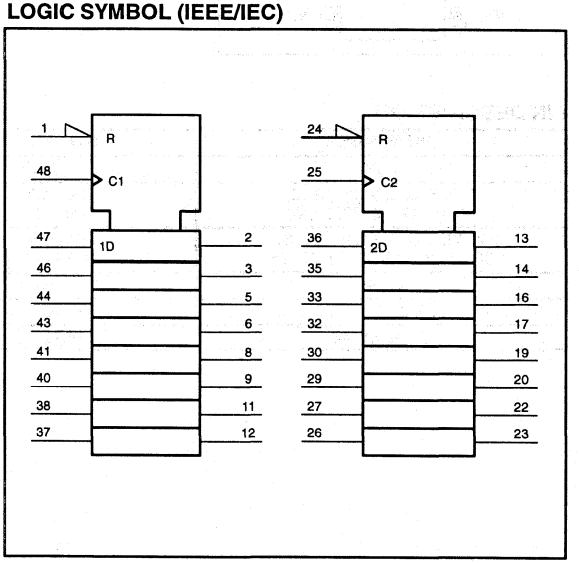
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
48-Pin Plastic Shrink Small Outline (SSOP) Type III	–40°C to +85°C	74LVT16273ADL	SOT370-1
48-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	–40°C to +85°C	74LVT16273ADGG	SOT362-1

LOGIC SYMBOL



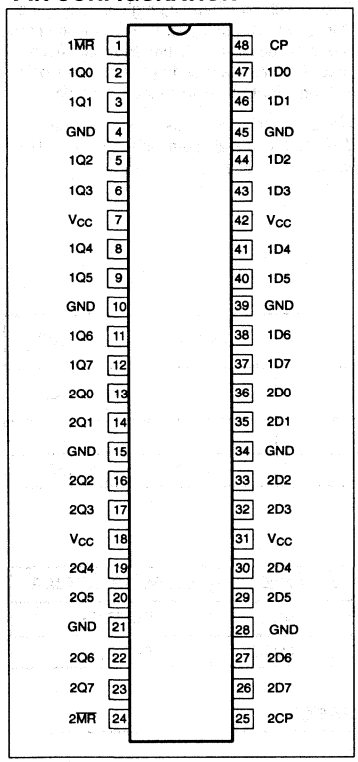
LOGIC SYMBOL (IEEE/IEC)



3.3V ABT 16–bit D-type flip-flop

74LVT16273A

PIN CONFIGURATION



PIN DESCRIPTION

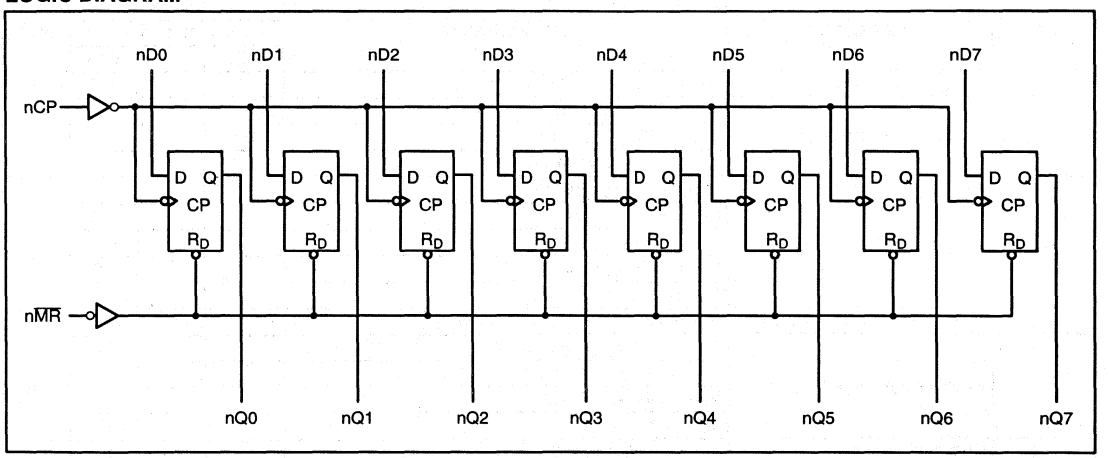
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 24	$1\overline{MR}$, $2\overline{MR}$	Master reset input (active-Low)
2, 3, 5, 6, 8, 9, 11, 12,13, 14, 16, 17, 19, 20, 22, 23	1Q0-1Q7 2Q0-2Q7	Data outputs
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1D0-1D7 2D0-2D-7	Data inputs
25, 48	1CP, 2CP	Clock pulse input (active rising edge)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

FUNCTION TABLE

Inputs			Outputs	operating mode
$n\overline{MR}$	nCP	nDX	nQ0-nQ7	
L	X	X	L	Reset (clear)
H	↑	h	H	Load "1"
H	↑	l	L	Load "0"
H	L	X	Q_0	Retain state

H = High voltage level
h = high voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
Q_0 = Output as it was

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1,2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
2. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
3. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
4. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–24	mA
I_{OL}	Low-level output current		24	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		48	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–55	+125	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C			UNIT
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA				–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2			V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4			
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0			
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA				0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA				0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA				0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA				0.5	
		V_{CC} = 3.0V; I_{OL} = 48mA				0.55	
V_{RST}	Power-up output Low voltage[5]	V_{CC} = 3.6V; I_O = 1mA; V_I = GND or V_{CC}				0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins			±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V				10	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]			1	
		V_{CC} = 3.6V; V_I = 0				-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V				±100	µA
I_{HOLD}	Bus Hold current D inputs	V_{CC} = 3V; V_I = 0.8V		75			µA
		V_{CC} = 3V; V_I = 2.0V		–75			
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V				125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq 1.2V$; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care				±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0				0.12	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0				5	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0				0.12	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND				0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. X = Don't care. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V	
			MIN	TYP	MAX	MAX	
f_{MAX}	Maximum clock frequency	1					MHz
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	1					ns
t_{PHL}	Propagation delay $n\overline{MR}$ to nQx	2					ns

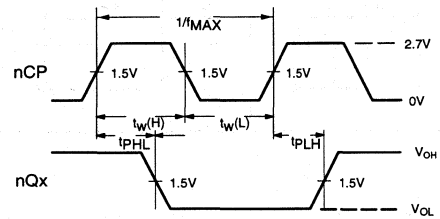
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

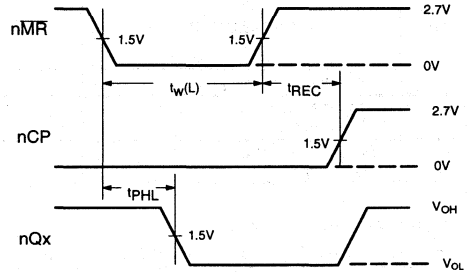
SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V	
			MIN	TYP	MAX	MIN	
$t_S(H)$ $t_S(L)$	Setup time, High or Low nDx to nCP	3					ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low nDx to nCP	3					ns
$t_W(H)$ $t_W(L)$	Clock pulse width High or Low	1					ns
$t_W(L)$	Master Reset pulse width, Low	2					ns
t_{REC}	Recovery time $n\overline{MR}$ to nCP	2					ns

AC WAVEFORMS

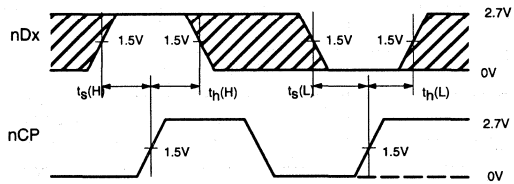
V_M = 1.5V, V_{IN} = GND to 2.7V



Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency

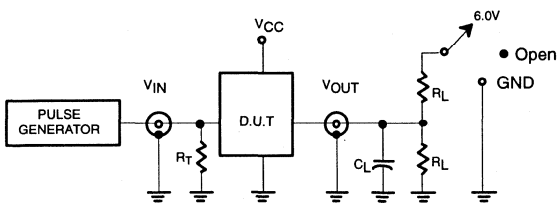


Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

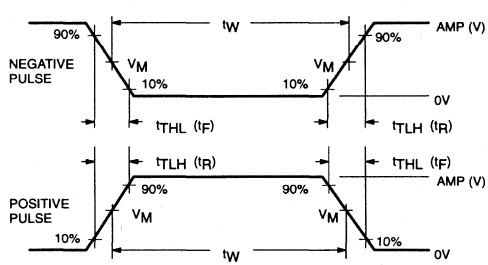


Waveform 3. Data Setup and Hold Times

NOTE: The shaded areas indicate when the input is permitted to change for predictable output performance.



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
ALL	OPEN

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT16	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

3.3V ABT 16-Bit transparent D-type latches (3-State)

74LVT16373A

FEATURES

- 16-bit transparent latch
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT16373A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is a 16-bit transparent D-type latch with non-inverting 3-State bus compatible outputs. The device can be used as two 8-bit latches or one 16-bit latch. When enable (E) input is High, the Q outputs follow the data (D) inputs. When enable is taken Low, the Q outputs are latched at the levels of the D inputs one setup time prior to the High-to-Low transition.

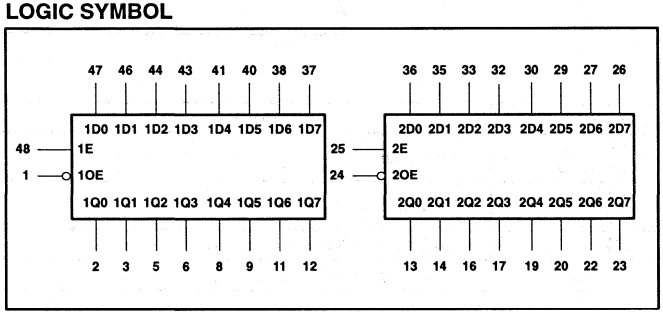
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nDx to nQx	C_L = 50pF; V_{CC} = 3.3V		ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	4	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or 3.0V	10	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	100	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
48-Pin Plastic Shrink Small Outline (SSOP) Type III	–40°C to +85°C	74LVT16373ADL	SOT370-1
48-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	–40°C to +85°C	74LVT16373ADGG	SOT362-1

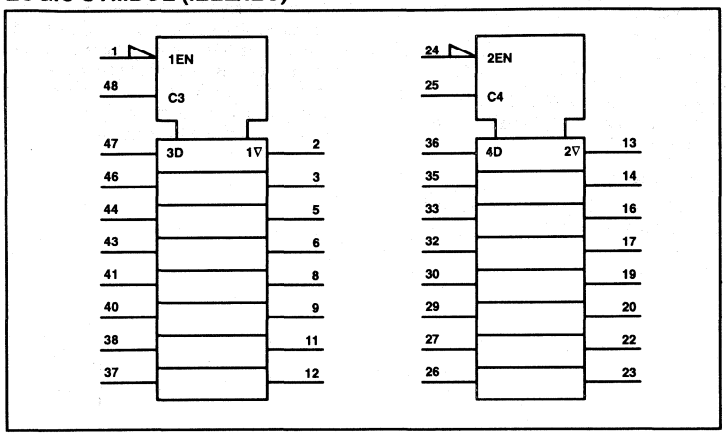
LOGIC SYMBOL



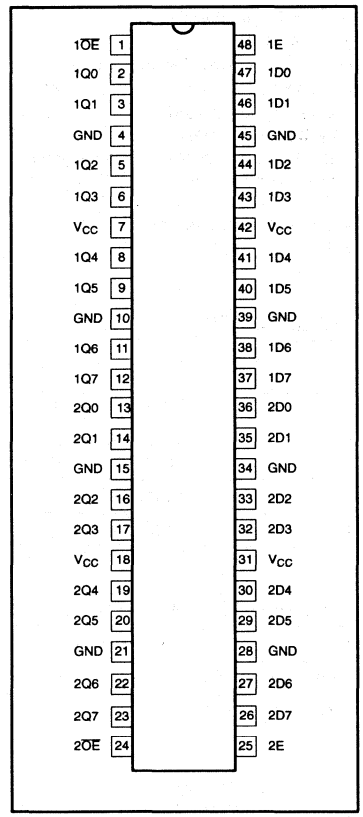
3.3V ABT 16-Bit transparent D-type latches (3-State)

74LVT16373A

LOGIC SYMBOL (IEEE/IEC)



PIN CONFIGURATION



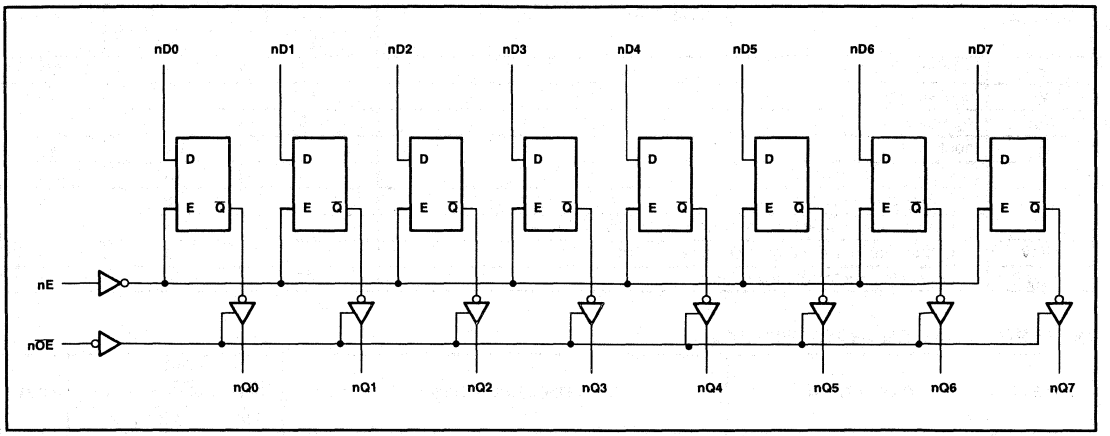
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1D0 – 1D7 2D0 – 2D7	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	1Q0 – 1Q7 2Q0 – 2Q7	Data outputs
1, 24	$1\overline{OE}$, $2\overline{OE}$	Output enable inputs (active-Low)
48, 25	1E, 2E	Enable inputs (active-High)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

3.3V ABT 16-Bit transparent D-type latches (3-State)

74LVT16373A

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$n\overline{OE}$	nE	nDx	REGISTER	nQ0 – nQ7	
L L	H H	L H	L H	L H	Enable and read register
L L	↓ ↓	l h	L H	L H	Latch and read register
L	L	X	NC	NC	Hold
H H	L H	X nDx	NC nDx	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC= No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

ABSOLUTE MAXIMUM RATINGS[1,2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:

6. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
7. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
8. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

3.3V ABT 16-Bit transparent D-type latches (3-State)

74LVT16373A

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA				–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2			V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4			
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0			
V_{OL}	Low–level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA				0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA				0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA				0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA				0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA				0.55	
V_{RST}	Power-up output Low voltage[5]	V_{CC} = 3.6V; I_O = 1mA; V_I = GND or V_{CC}				0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins			±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V				10	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]			1	
		V_{CC} = 3.6V; V_I = 0				-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V				±100	µA
I_{HOLD}	Bus Hold current D inputs	V_{CC} = 3V; V_I = 0.8V		75			µA
		V_{CC} = 3V; V_I = 2.0V		–75			µA
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V				125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care				±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IH} or V_{IL}				5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IH} or V_{IL}				–5	
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0				0.12	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0				5	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0				0.12	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND				0.2	mA

NOTES:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay nDx to nQx	2					ns
t_{PLH} t_{PHL}	Propagation delay nE to nQx	1					ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	4 5					ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	4 5					ns

NOTE:

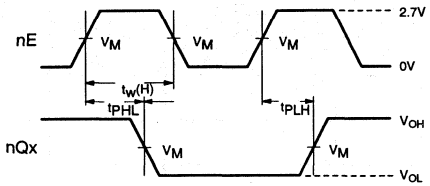
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC SETUP REQUIREMENTS

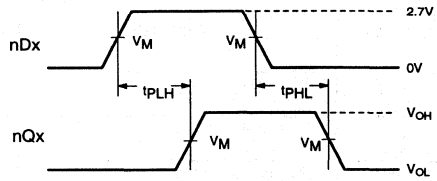
GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			= 3.3V ±0.3V			2.7V	
			MIN	TYP	MAX	MIN	
$t_S(H)$ $t_S(L)$	Setup time nDx to nE	3					ns
$t_h(H)$ $t_h(L)$	Hold time nDx to nE	3					ns
$t_W(H)$	nE pulse width High	1					ns

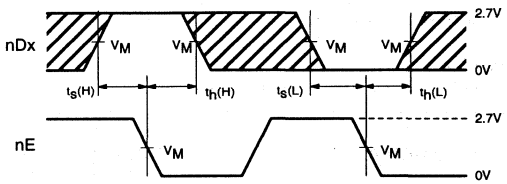
AC WAVEFORMS



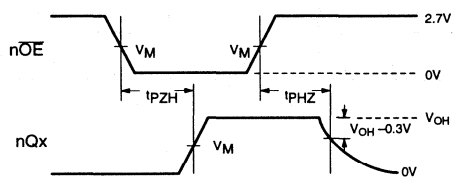
Waveform 1. Propagation Delay, Enable to Output, and Enable Pulse Width



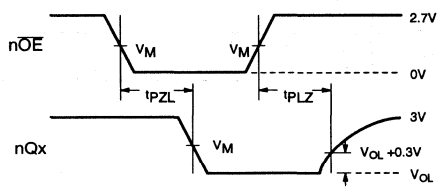
Waveform 2. Propagation Delay for Data to Outputs



Waveform 3. Data Setup and Hold Times



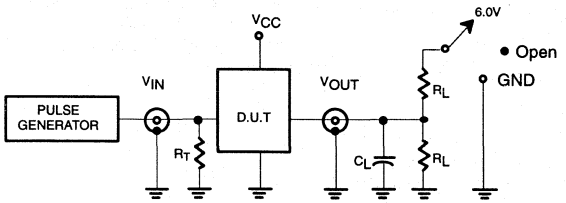
Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



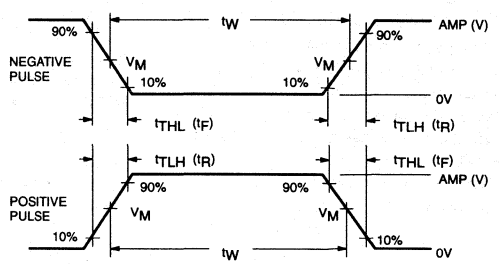
Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT16	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

3.3V ABT 16-bit edge-triggered D-type flip-flops (3-State)

74LVT16374A

FEATURES

- 16-bit edge-triggered flip-flop
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT16374A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is a 16-bit edge-triggered D-type flip-flop featuring non-inverting 3-State outputs. The device can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CP), the Q outputs of the flip-flop take on the logic levels set up at the D inputs.

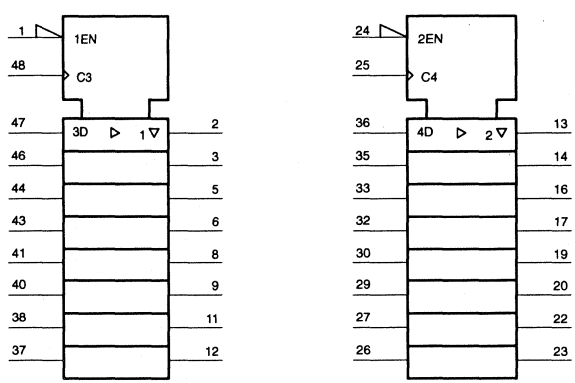
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	C_L = 50pF; V_{CC} = 3.3V		ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	4	pF
C_{OUT}	Output pin capacitance	Outputs disabled; V_O = 0V or 3.0V	10	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	100	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
48-Pin Plastic Shrink Small Outline (SSOP) Type III	–40°C to +85°C	74LVT16374ADL	SOT370-1
48-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	–40°C to +85°C	74LVT16374ADGG	SOT362-1

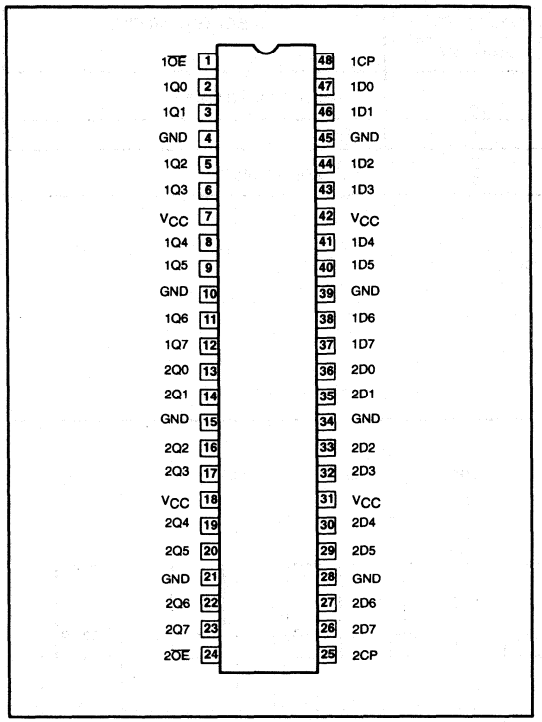
LOGIC SYMBOL (IEEE/IEC)



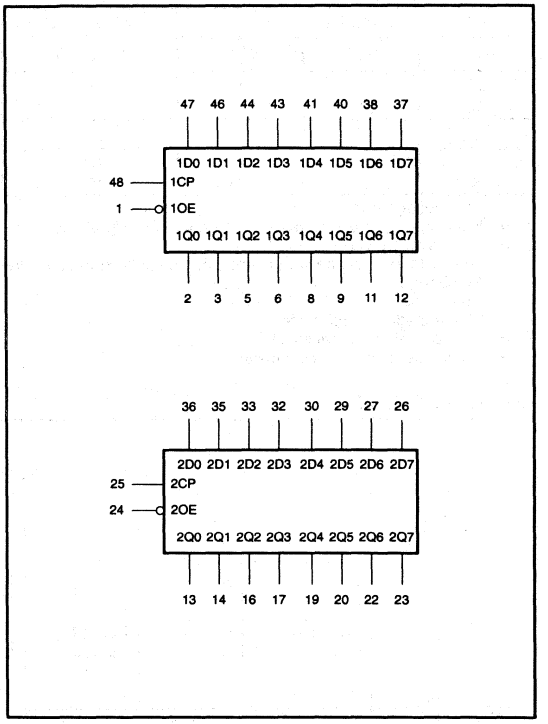
3.3V ABT 16-bit edge-triggered D-type flip-flops (3-State)

74LVT16374A

PIN CONFIGURATION



LOGIC SYMBOL



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
47, 46, 44, 43, 41, 40, 38, 37 36, 35, 33, 32, 30, 29, 27, 26	1D0 – 1D7 2D0 – 2D7	Data inputs
2, 3, 5, 6, 8, 9, 11, 12 13, 14, 16, 17, 19, 20, 22, 23	1Q0 – 1Q7 2Q0 – 2Q7	Data outputs
1, 24	$1\overline{OE}$, $2\overline{OE}$	Output enable inputs (active-Low)
48, 25	1CP, 2CP	Clock pulse inputs (active rising edge)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

3.3V ABT 16-bit edge-triggered D-type flip-flops (3-State)

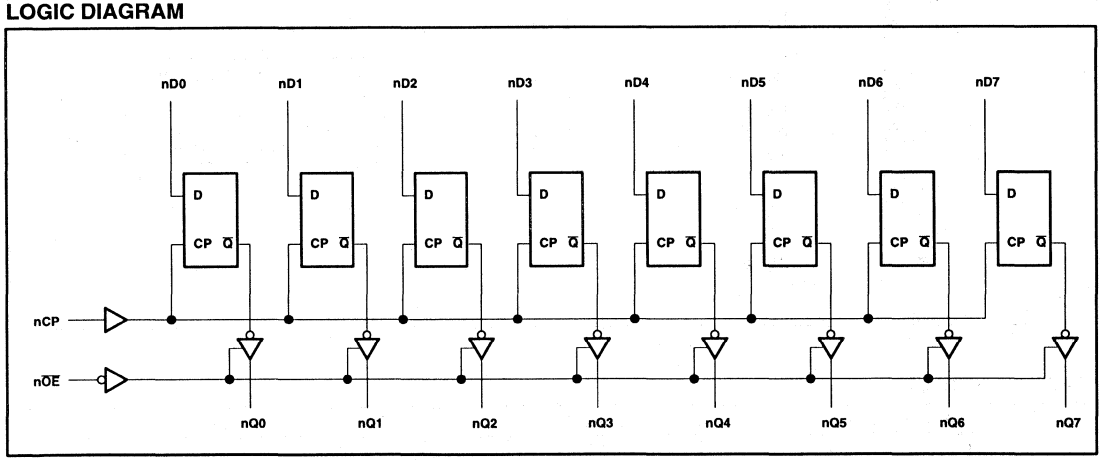
74LVT16374A

FUNCTION TABLE

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$n\overline{OE}$	nCP	nDx	REGISTER	nQ0 – nQ7	
L L	↑ ↑	l h	L H	L H	Load and read register
L	↕	X	NC	NC	Hold
H H	↕ ↑	X nDx	NC nDx	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↕ = Not a Low-to-High clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1,2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
2. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
3. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
4. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

3.3V ABT 16-bit edge-triggered D-type flip-flops (3-State)

74LVT16374A

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C			UNIT
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA				–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2			V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4			
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0			
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA				0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA				0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA				0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA				0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA				0.55	
V_{RST}	Power-up output Low voltage[5]	V_{CC} = 3.6V; I_O = 1mA; V_I = GND or V_{CC}				0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins			±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V				10	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]			1	
		V_{CC} = 3.6V; V_I = 0				-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V				±100	µA
I_{HOLD}	Bus Hold current D inputs	V_{CC} = 3V; V_I = 0.8V		75			µA
		V_{CC} = 3V; V_I = 2.0V		–75			
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V				125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq 1.2V$; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care				±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IH} or V_{IL}				5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IH} or V_{IL}				–5	
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0				0.12	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0				5	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0				0.12	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND				0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
f_{max}	Maximum clock frequency	1					MHz
t_{PLH} t_{PHL}	Propagation delay nCP to nDx	1					ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	3 4					ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	3 4					ns

NOTE:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

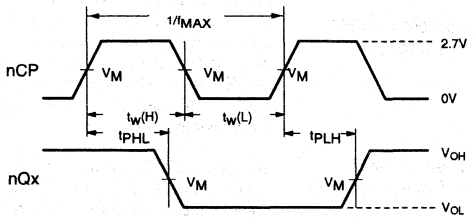
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

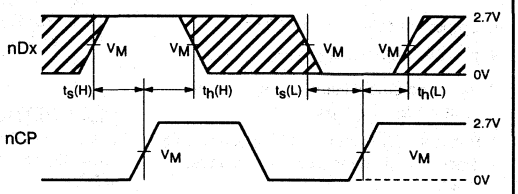
SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ±0.3V			2.7V	
			MIN	TYP	MAX	MIN	
$t_S(H)$ $t_S(L)$	Setup time nDx to nE	3					ns
$t_h(H)$ $t_h(L)$	Hold time nDx to nE	3					ns
$t_W(H)$ tw(L)	nE pulse width High or Low	1					ns

AC WAVEFORMS

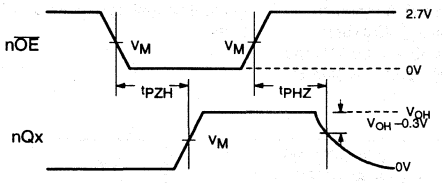
V_M = 1.5V, V_{IN} = GND to 3.0V



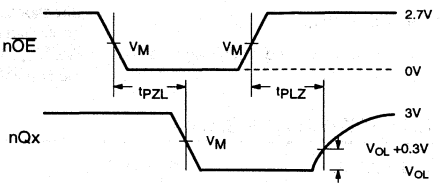
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Data Setup and Hold Times



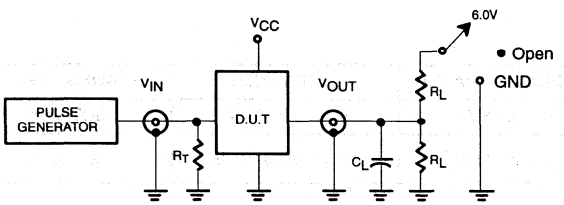
Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



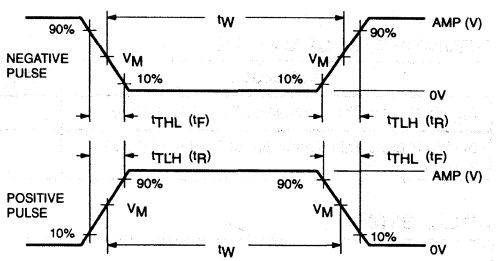
Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT16	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

3.3V ABT18-bit universal bus transceiver (3-State) 74LVT16500A

FEATURES

- 18-bit bidirectional bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT16500A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is an 18-bit universal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable (OEAB and $\overline{OEBA}$), latch enable (LEAB and LEBA), and clock ($\overline{CPAB}$ and $\overline{CPBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is High. When LEAB is Low, the A data is latched if $\overline{CPAB}$ is held at a High or Low logic level. If LEAB is Low, the A-bus data is stored in the latch/flip-flop on the Low-to-High transition of $\overline{CPAB}$. When OEAB is High, the outputs are active. When OEAB is Low, the outputs are in the high-impedance state.

Data flow for B-to-A is similar to that of A-to-B but uses $\overline{OEBA}$, LEBA and $\overline{CPBA}$. The output enables are complimentary (OEAB is active High, and $\overline{OEBA}$ is active Low).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

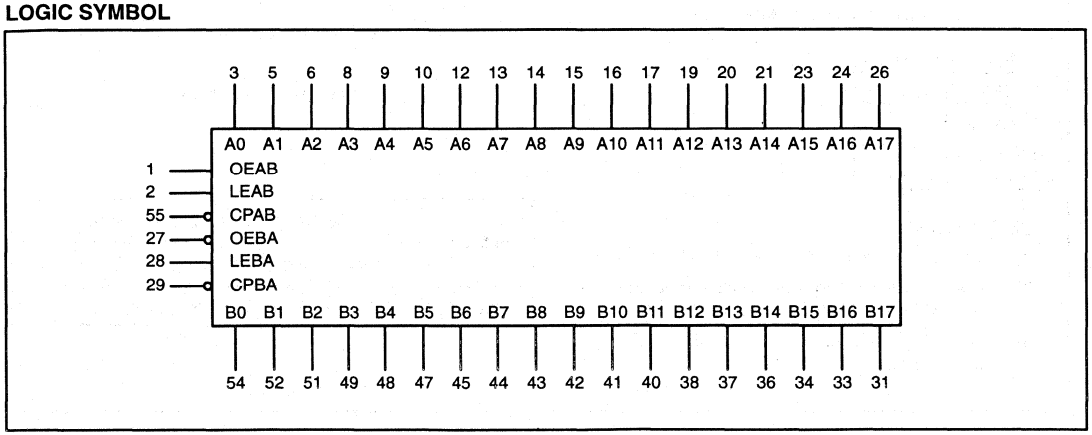
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 3.3V		ns
C_{IN}	Input capacitance (Control pins)	V_I = 0V or 3.0V	4	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O}$ = 0V or 3.0V	10	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	100	µA

ORDERING INFORMATION

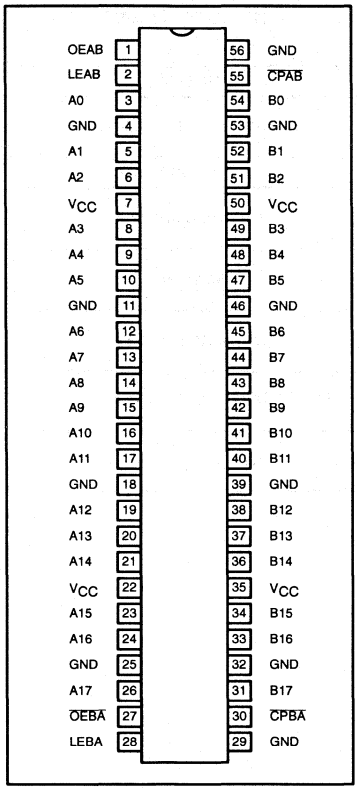
PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
56-Pin Plastic Shrink Small Outline (SSOP) Type III	–40°C to +85°C	74LVT16500ADL	SOT371-1
56-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	–40°C to +85°C	74LVT16500ADGG	SOT364-1

LOGIC SYMBOL

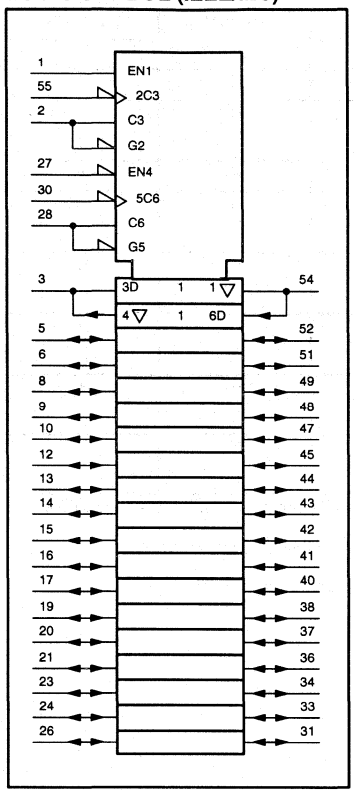


3.3V ABT18-bit universal bus transceiver (3-State) 74LVT16500A

PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	OEAB	A-to-B Output enable input
27	$\overline{OEBA}$	B-to-A Output enable input (active low)
2, 28	LEAB/LEBA	A-to-B/B-to-A Latch enable input
55,30	$\overline{CPAB}$/$\overline{CPBA}$	A-to-B/B-to-A Clock input (active falling edge)
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	A0-A17	Data inputs/outputs (A side)
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	B0-B17	Data inputs/outputs (B side)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

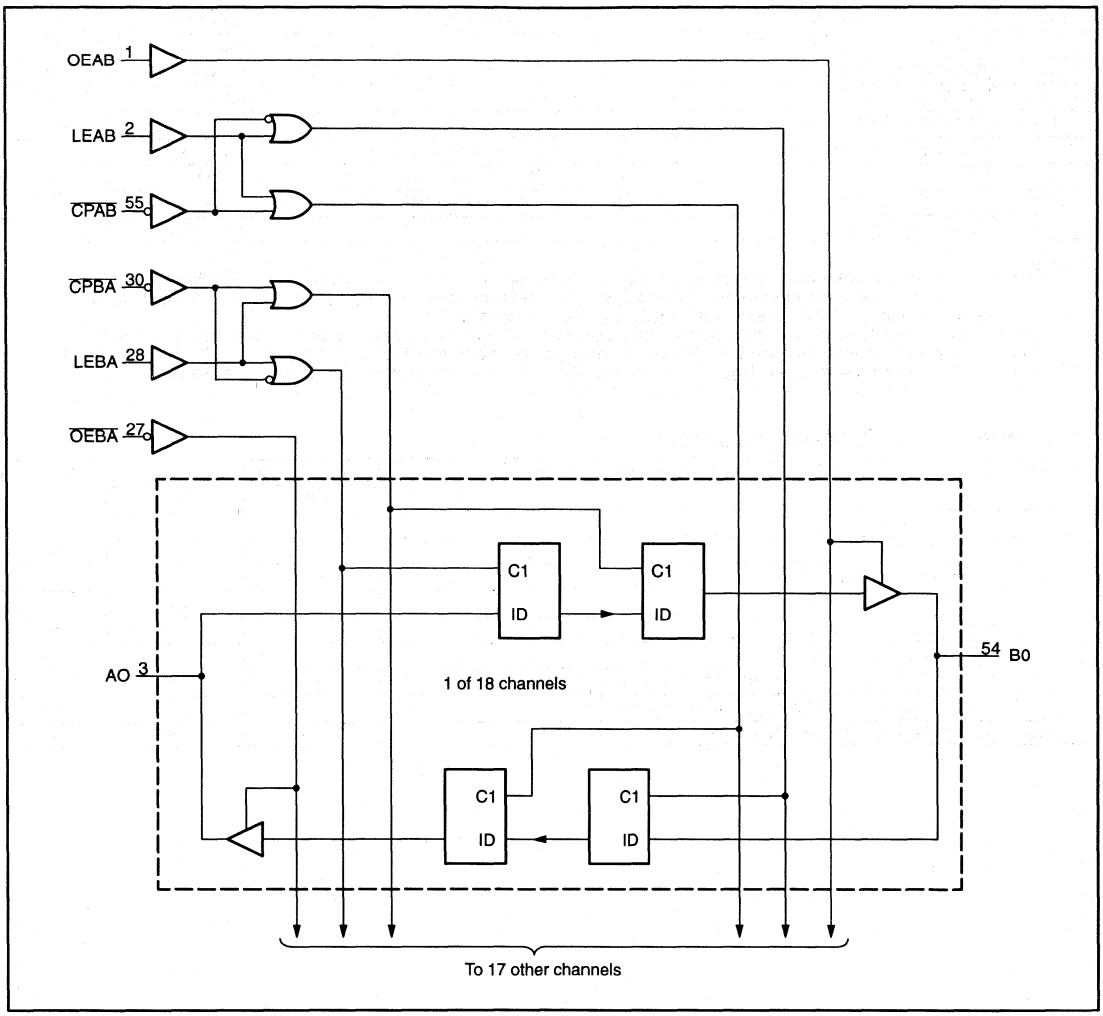
FUNCTION TABLE

INPUTS				Internal Registers	OUTPUTS	OPERATING MODE
OEAB	LEAB	$\overline{CPAB}$	An		Bn	
L	H	X	X	X	Z	Disabled
L	↓	X	h	H	Z	Disabled, Latch data
L	↓	X	l	L	Z	
L	L	H or L	X	NC	Z	Disabled, Hold data
L	L	↓	h	H	Z	Disabled, Clock data
L	L	↓	l	L	Z	
H	H	X	H	H	H	Transparent
H	H	X	L	L	L	
H	↓	X	h	H	H	Latch data & display
H	↓	X	l	L	L	
H	L	↓	h	H	H	Clock data & display
H	L	↓	l	L	L	
H	L	H or L	X	H	H	Hold data & display
H	L	H or L	X	L	L	

NOTE: A-to-B data flow is shown; B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, and $\overline{CPBA}$.

H = High voltage level
h = High voltage level one set-up time prior to the Enable or Clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Enable or Clock transition
NC= No Change
X = Don't care
Z = High Impedance "off" state
↓ = High-to-Low Enable or Clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1,2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA				–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2			V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4			
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0			
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA				0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA				0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA				0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA				0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA				0.55	
V_{RST}	Power-up output low voltage[5]	V_{CC} = 3.6V; I_O = 1mA; V_I = GND or V_{CC}				0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins			±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V				10	
		V_{CC} = 3.6V; V_I = 5.5V	I/O Data pins[4]			20	
		V_{CC} = 3.6V; V_I = V_{CC}				10	
		V_{CC} = 3.6V; V_I = 0				-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V				±100	µA
I_{HOLD}	Bus Hold current A or B outputs	V_{CC} = 3V; V_I = 0.8V		75			µA
		V_{CC} = 3V; V_I = 2.0V		-75			µA
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V				125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care				±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0				0.12	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0				5	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0				0.12	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND				0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
f_{MAX}	Maximum clock frequency	1					MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CPAB}$ to Bn or $\overline{CPBA}$ to An	1					ns
t_{PLH} t_{PHL}	Propagation delay LEAB to Bn or LEBA to An	3					ns
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	2					ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	5 6					ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	5 6					ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

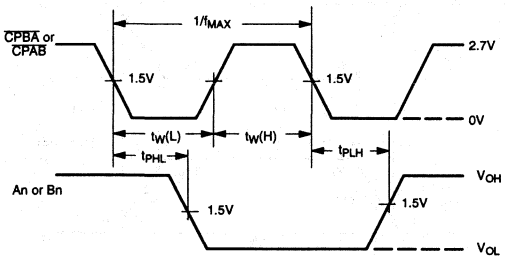
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

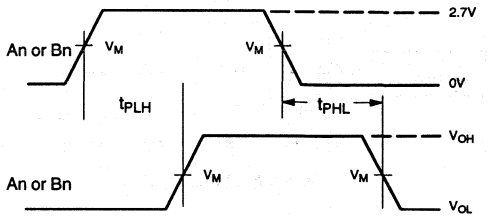
SYMBOL	PARAMETER	WAVEFORM					UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V	
			MIN	TYP	MAX	MIN	
ts(H) ts(L)	Setup time, High or Low An to $\overline{CPAB}$ or Bn to $\overline{CPBA}$	4					ns
th(H) th(L)	Hold time, High or Low An to $\overline{CPAB}$ or Bn to $\overline{CPBA}$	4					ns
ts(H) ts(L)	Setup time, High or Low An to LEAB or Bn to $\overline{CPBA}$	4					ns
th(H) th(L)	Hold time, High or Low An to LEAB or Bn to LEBA	4					ns
tw(H) tw(L)	Pulse width, High or Low $\overline{CPAB}$ or $\overline{CPBA}$	1					ns
tw(H)	LEAB or LEBA pulse width, High	3					ns

AC WAVEFORMS

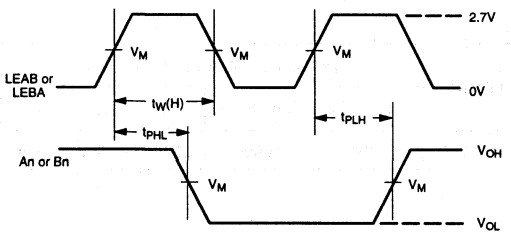
V_M = 1.5V, V_{IN} = GND to 2.7V



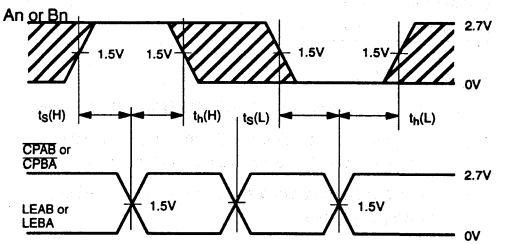
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



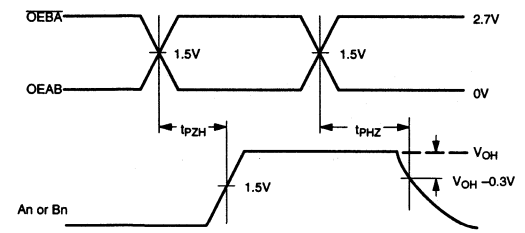
Waveform 2. Propagation Delay, Transparent Mode



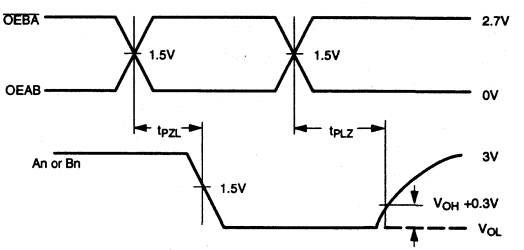
Waveform 3. Propagation Delay, Enable to Output, and Enable Pulse Width



Waveform 4. Data Setup and Hold Times



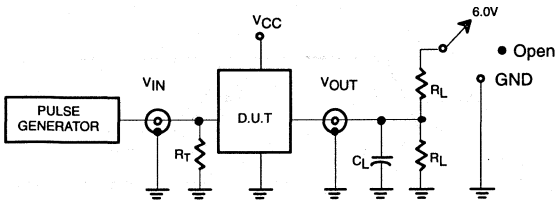
Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level



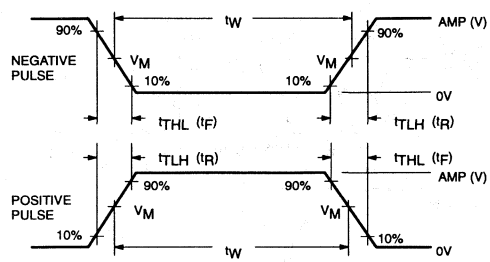
Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

Note: The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT16	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

3.3V ABT18-bit universal bus transceiver (3-State) 74LVT16501A

FEATURES

- 18-bit bidirectional bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT16501A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is an 18-bit universal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable (OEAB and $\overline{OEBA}$), latch enable (LEAB and LEBA), and clock (CPAB and CPBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is High. When LEAB is Low, the A data is latched if CPAB is held at a High or Low logic level. If EAB is Low, the A-bus data is stored in the latch/flip-flop on the Low-to-High transition of CPAB. When OEAB is High, the outputs are active. When OEAB is Low, the outputs are in the high-impedance state.

Data flow for B-to-A is similar to that of A-to-B but uses $\overline{OEBA}$, LEBA and CPBA. The output enables are complimentary (OEAB is active High, and $\overline{OEBA}$ is active Low).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

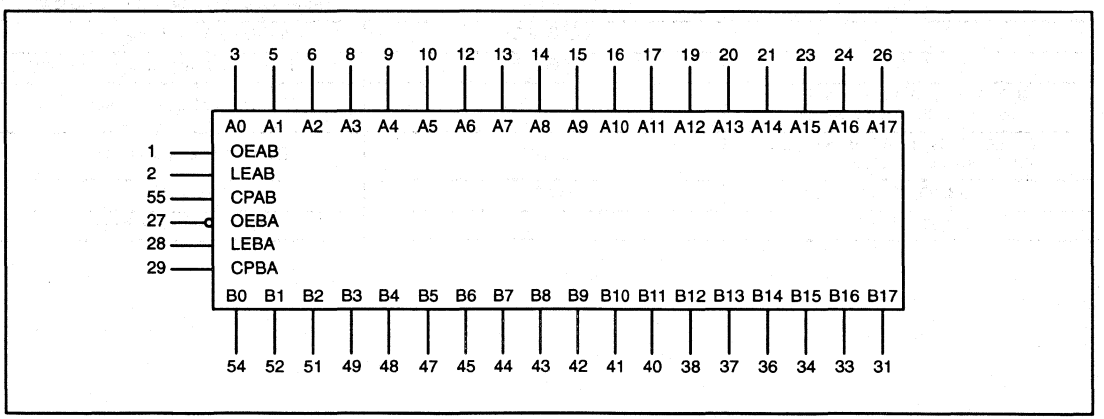
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 3.3V		ns
C_{IN}	Input capacitance (Control pins)	V_I = 0V or 3.0V	4	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O}$ = 0V or 3.0V	10	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	100	µA

ORDERING INFORMATION

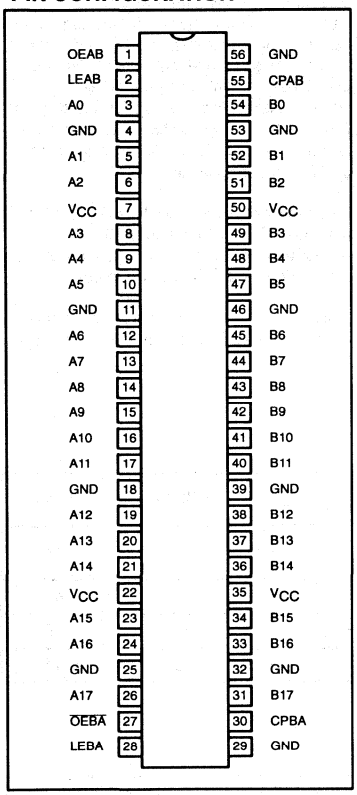
PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
56-Pin Plastic Shrink Small Outline (SSOP) Type III	–40°C to +85°C	74LVT16501ADL	SOT371-1
56-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	–40°C to +85°C	74LVT16501ADGG	SOT364-1

LOGIC SYMBOL

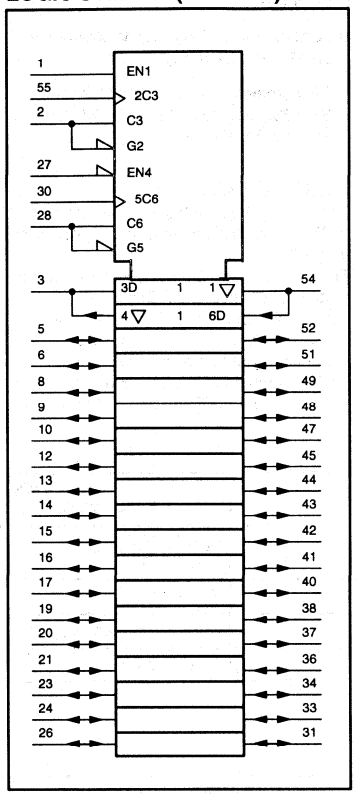


3.3V ABT18-bit universal bus transceiver (3-State) 74LVT16501A

PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	OEAB	A-to-B Output enable input
27	$\overline{\text{OEBA}}$	B-to-A Output enable input (active low)
2, 28	LEAB/LEBA	A-to-B/B-to-A Latch enable input
55,30	CPAB/CPBA	A-to-B/B-to-A Clock input (active rising edge)
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	A0-A17	Data inputs/outputs (A side)
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	B0-B17	Data inputs/outputs (B side)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

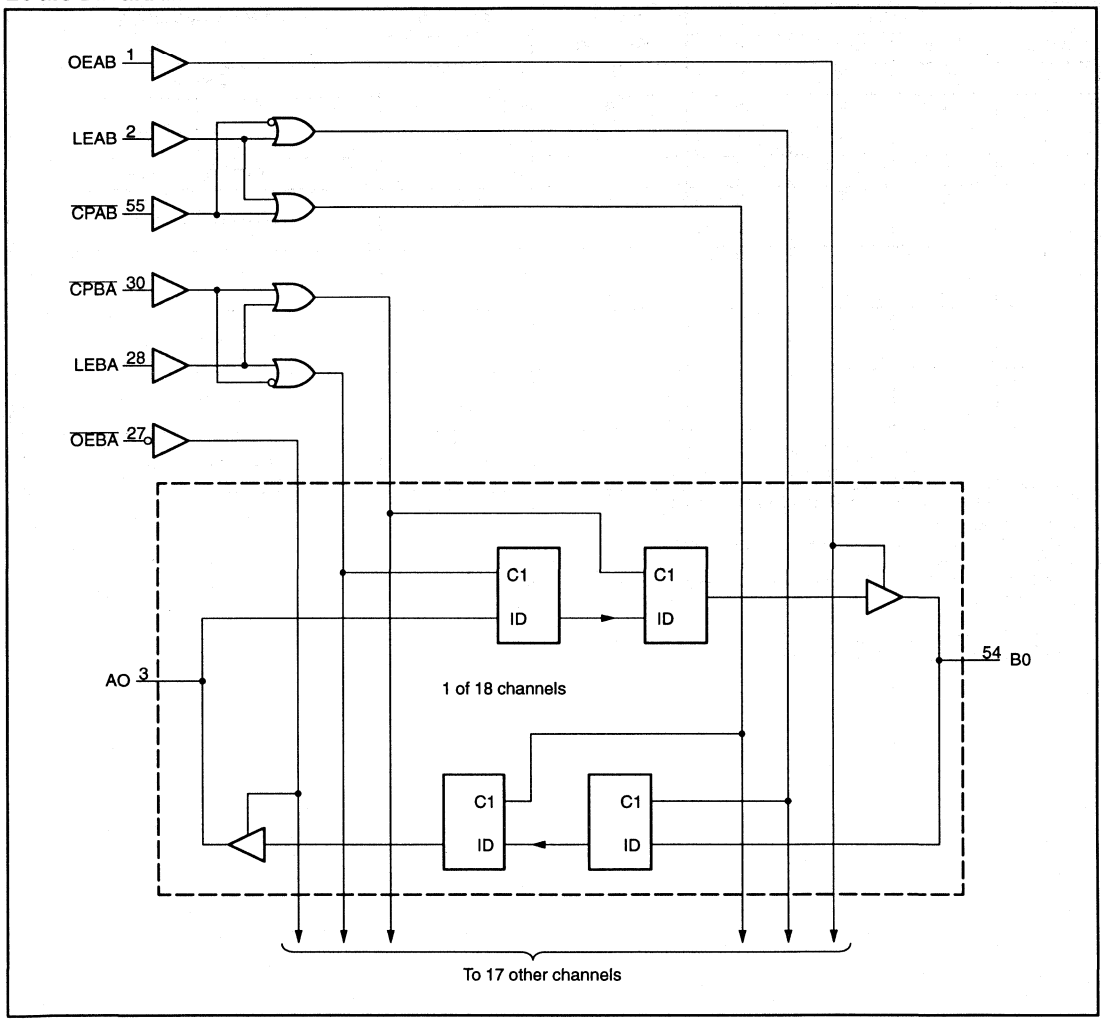
FUNCTION TABLE

INPUTS				Internal Registers	OUTPUTS	OPERATING MODE
OEAB	LEAB	CPAB	An		Bn	
L	H	X	X	X	Z	Disabled
L	↓	X	h	H	Z	Disabled, Latch data
L	↓	X	l	L	Z	
L	L	H or L	X	NC	Z	Disabled, Hold data
L	L	↑	h	H	Z	Disabled, Clock data
L	L	↑	l	L	Z	
H	H	X	H	H	H	Transparent
H	H	X	L	L	L	
H	↓	X	h	H	H	Latch data & display
H	↓	X	l	L	L	
H	L	↑	h	H	H	Clock data & display
H	L	↑	l	L	L	
H	L	H or L	X	H	H	Hold data & display
H	L	H or L	X	L	L	

NOTE: A-to-B data flow is shown; B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, and CPBA.

H = High voltage level
h = High voltage level one set-up time prior to the Enable or Clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Enable or Clock transition
NC= No Change
X = Don't care
Z = High Impedence "off" state
↓ = High-to-Low Enable or Clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1,2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage3		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA				–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2			V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4			
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0			
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA				0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA				0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA				0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA				0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA				0.55	
V_{RST}	Power-up output low voltage[5]	V_{CC} = 3.6V; I_O = 1mA; V_I = GND or V_{CC}				0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins			±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V				10	
		V_{CC} = 3.6V; V_I = 5.5V	I/O Data pins[4]			20	
		V_{CC} = 3.6V; V_I = V_{CC}				10	
		V_{CC} = 3.6V; V_I = 0				-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V				±100	µA
I_{HOLD}	Bus Hold current A or B outputs	V_{CC} = 3V; V_I = 0.8V		75			µA
		V_{CC} = 3V; V_I = 2.0V		–75			µA
I_{EX}	Current into an ouptut in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V				125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care				±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0				0.12	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0				5	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0				0.12	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND				0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specificed voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
f_{MAX}	Maximum clock frequency	1					MHz
t_{PLH} t_{PHL}	Propagation delay CPAB to Bn or CPBA to An	1					ns
t_{PLH} t_{PHL}	Propagation delay LEAB to Bn or LEBA to An	3					ns
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	2					ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	5 6					ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	5 6					ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

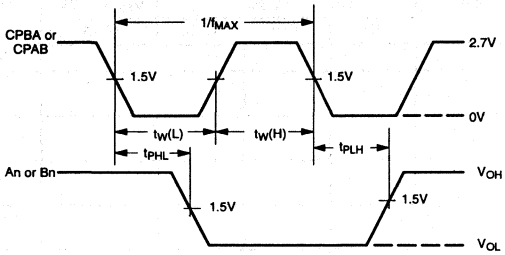
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

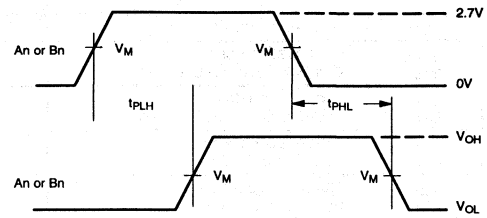
SYMBOL	PARAMETER	WAVEFORM					UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V	
			MIN	TYP	MAX	MIN	
ts(H) ts(L)	Setup time, High or Low An to CPAB or Bn to CPBA	4					ns
th(H) th(L)	Hold time, High or Low An to CPAB or Bn to CPBA	4					ns
ts(H) ts(L)	Setup time, High or Low An to LEAB or Bn to CPBA	4					ns
th(H) th(L)	Hold time, High or Low An to LEAB or Bn to LEBA	4					ns
tw(H) tw(L)	Pulse width, High or Low CPAB or CPBA	1					ns
tw(H)	LEAB or LEBA pulse width, High	3					ns

AC WAVEFORMS

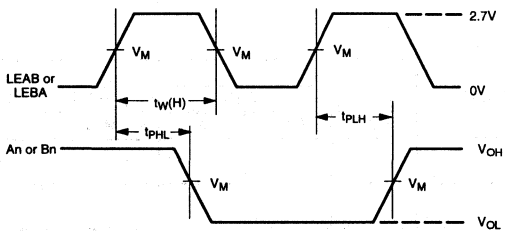
V_M = 1.5V, V_{IN} = GND to 2.7V



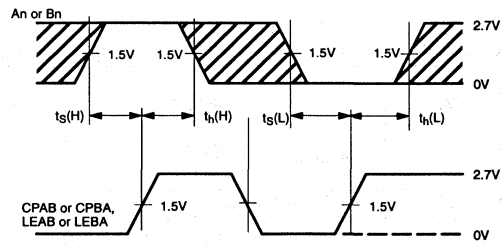
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



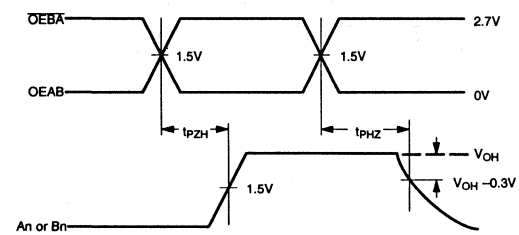
Waveform 2. Propagation Delay, Transparent Mode



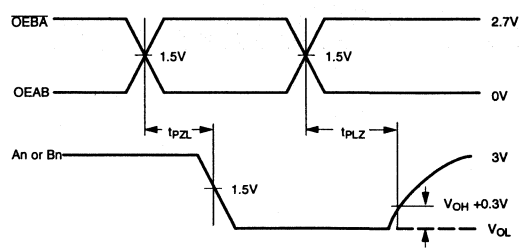
Waveform 3. Propagation Delay, Enable to Output, and Enable Pulse Width



Waveform 4. Data Setup and Hold Times



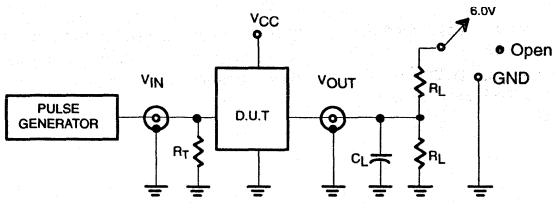
Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level



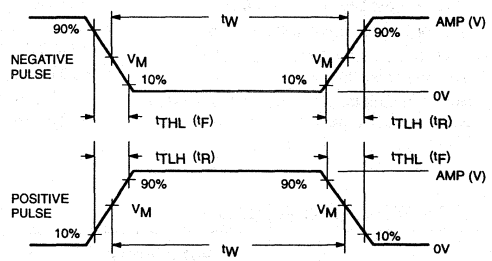
Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

Note: The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT16	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

3.3V ABT 16-bit buffer/driver 3-State — 74LVT16541A

FEATURES

- 16-bit universal bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT16541A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device can be used as two octal buffers or one 16-bit buffer. The device is ideal for driving bus lines.

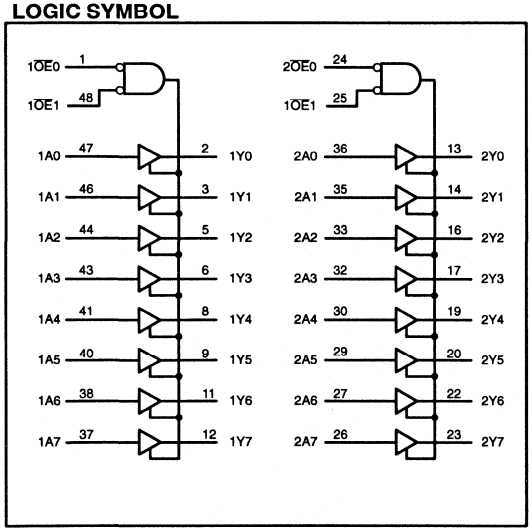
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	C_L = 50pF; V_{CC} = 3.3V		ns
C_{IN}	Input capacitance $n\overline{O}Ex$	V_I = 0V or 3.0V	4	pF
C_{OUT}	Output pin capacitance	Outputs disabled; V_O = 0V or 3.0V	10	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	100	µA

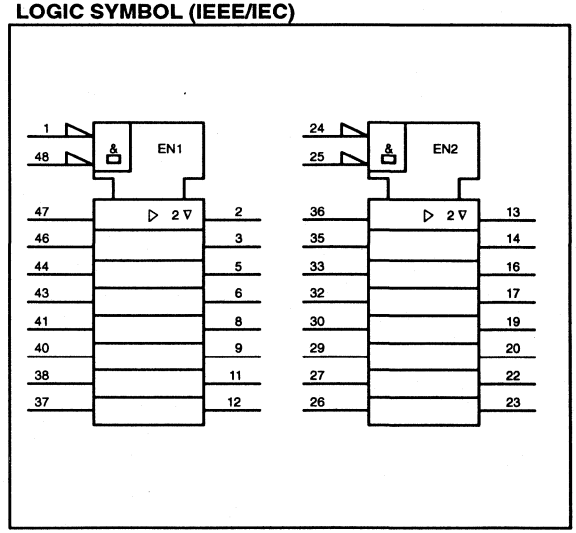
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
48-Pin Plastic Shrink Small Outline (SSOP) Type III	–40°C to +85°C	74LVT16541ADL	SOT370-1
48-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	–40°C to +85°C	74LVT16541ADGG	SOT362-1

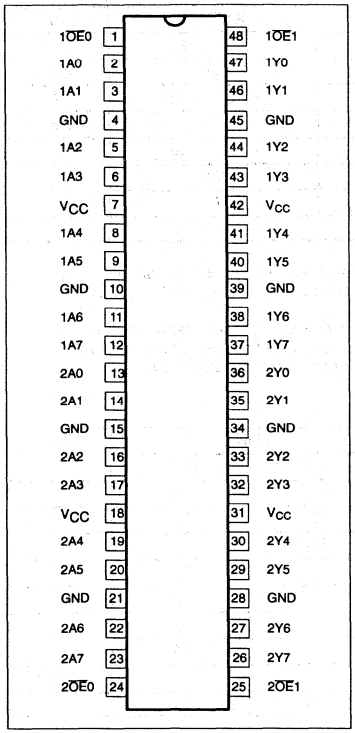
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1A0–1A7 2A0–2A7	Data inputs
2, 3, 5, 6, 8, 9, 11, 12,13, 14, 16, 17, 19, 20, 22, 23	1Y0–1Y7 2Y0–2Y7	Data outputs
1, 48 24, 25	1$\overline{OE}$0, 1$\overline{OE}$1, 2$\overline{OE}$0, 2$\overline{OE}$1	Output enables
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			OUTPUTS
n$\overline{OE}$0	n$\overline{OE}$1	nAx	nYx
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High Impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1,2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA				–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2			V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4			
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0			
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA				0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA				0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA				0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA				0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA				0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins			±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V				10	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]			1	
		V_{CC} = 3.6V; V_I = 0				-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V				±100	µA
I_{HOLD}	Bus Hold current A inputs	V_{CC} = 3V; V_I = 0.8V		75			µA
		V_{CC} = 3V; V_I = 2.0V		–75			µA
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V				125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care				±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IL} or V_{IH}				5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}				–5	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.13	0.12	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3.5	5	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0			0.13	0.12	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND				0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.

AC CHARACTERISTICS

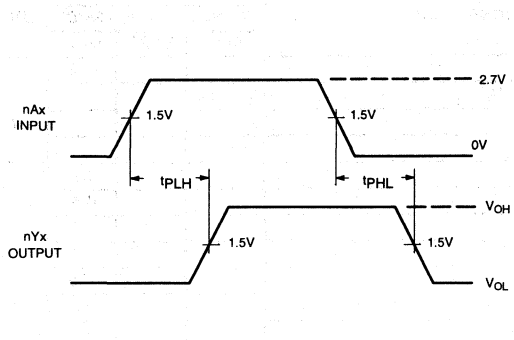
GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS V_{CC} = 3.3V ±0.3V MIN	TYP[1]	MAX	V_{CC} = 2.7V MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	1					ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2					ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	2					ns

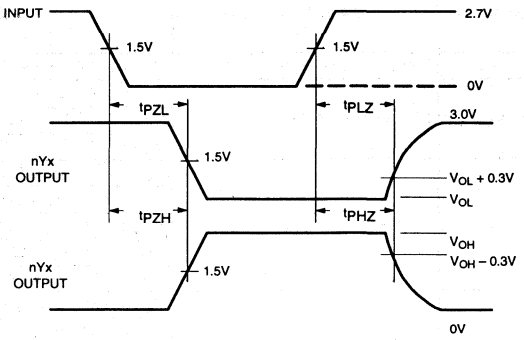
NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 2.7V

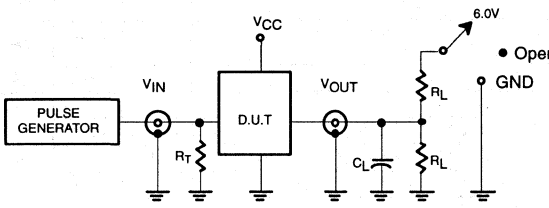


Waveform 1. Waveforms Showing the Input to Output Propagation Delays

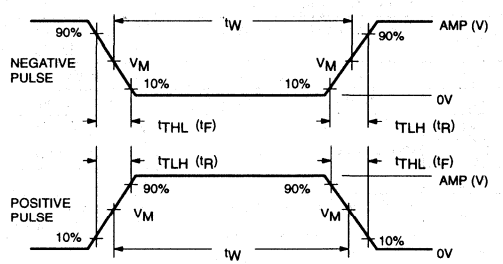


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT16	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

3.3V ABT 16-bit registered transceiver (3-State) 74LVT16543A

FEATURES

- 16-bit universal bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT16543A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

Separate latch-enable ($n\overline{LEAB}$) and output-enable ($n\overline{OEAB}$ or $n\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($n\overline{CEAB}$) input must be Low in order to enter data from A or to output data from B. If $n\overline{CEAB}$ is Low and $n\overline{LEAB}$ is Low, the latches are transparent; a subsequent Low-to-High transition of $n\overline{LEAB}$ puts the A latches in the storage mode. With $n\overline{CEAB}$ and $n\overline{OEAB}$ both Low, the 3-State B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the $n\overline{CEBA}$, $n\overline{LEBA}$, and $n\overline{OEBA}$ inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

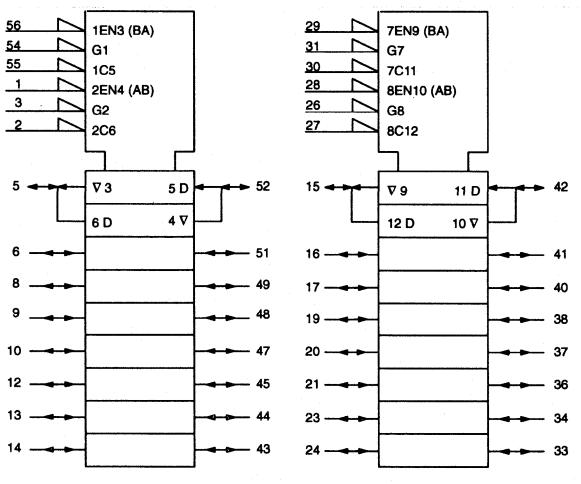
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	C_L = 50pF; V_{CC} = 3.3V		ns
C_{IN}	Input capacitance control pins	V_I = 0V or 3.0V	4	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O}$ = 0V or 3.0V	10	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	100	µA

ORDERING INFORMATION

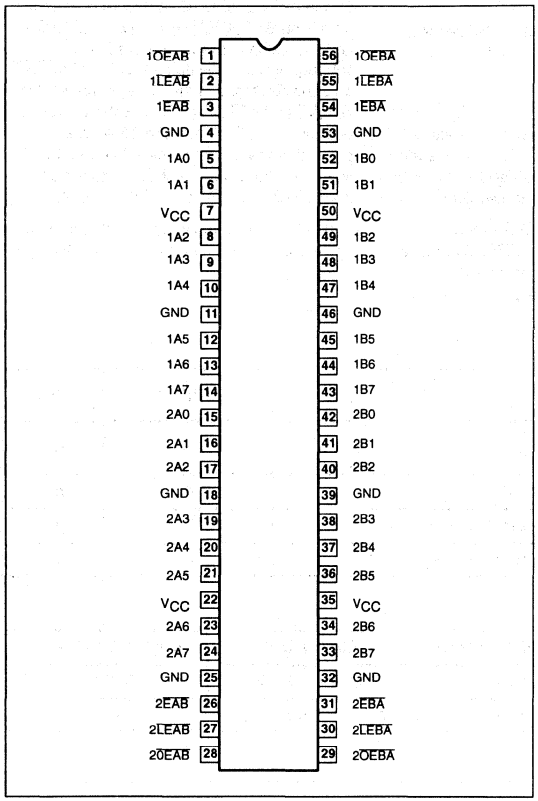
PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
56-Pin Plastic Shrink Small Outline (SSOP) Type III	–40°C to +85°C	74LVT16543ADL	SOT371-1
56-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	–40°C to +85°C	74LVT16543ADGG	SOT364-1

LOGIC SYMBOL (IEEE/IEC)

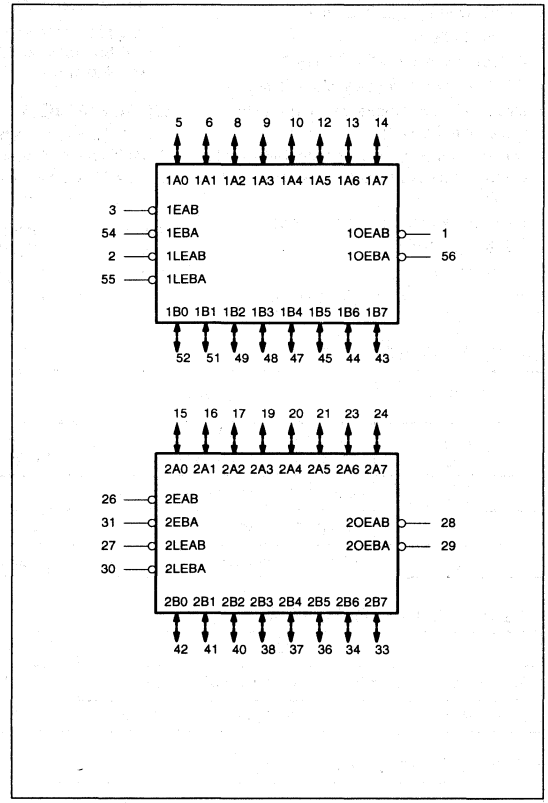


3.3V ABT 16-bit registered transceiver (3-State) 74LVT16543A

PIN CONFIGURATION



LOGIC SYMBOL



3.3V ABT 16-bit registered transceiver (3-State) 74LVT16543A

FUNCTIONAL DESCRIPTION

The 74ABT16543A contains two sets of eight D-type latches, with separate control pins for each set. Using data flow from A to B as an example, when the A-to-B Enable ($n\overline{EAB}$) input and the A-to-B Latch Enable ($n\overline{LEAB}$) input are Low, the A-to-B path is transparent.

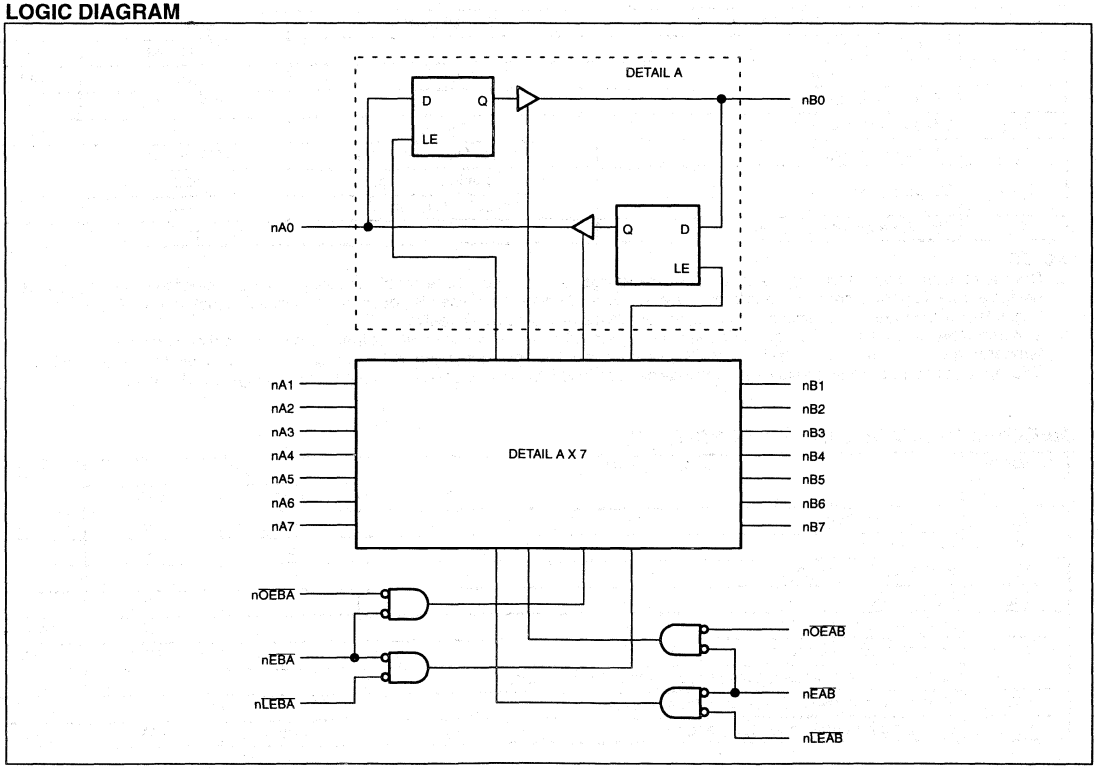
A subsequent Low-to-High transition of the $n\overline{LEAB}$ signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With $n\overline{EAB}$ and $n\overline{OEAB}$ both Low, the 3-State B output buffers are active and display the data present at the outputs of the A latches.

Control of data flow from B to A is similar, but using the $n\overline{EBA}$, $n\overline{LEBA}$, and $n\overline{OEBA}$ inputs.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24	1A0 – 1A7, 2A0 – 2A7	A Data inputs/outputs
52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40,38, 37, 36, 34, 33	1B0 – 1B7, 2B0 – 2B7	B Data inputs/outputs
1, 56 28, 29	$1\overline{OEAB}$, $1\overline{OEBA}$, $2\overline{OEAB}$, $2\overline{OEBA}$	A to B / B to A Output Enable inputs (active-Low)
3, 54 26, 31	$1\overline{EAB}$, $1\overline{EBA}$, $2\overline{EAB}$, $2\overline{EBA}$	A to B / B to A Enable inputs (active-Low)
2, 55 27, 30	$1\overline{LEAB}$, $1\overline{LEBA}$, $2\overline{LEAB}$, $2\overline{LEBA}$	A to B / B to A Latch Enable inputs (active-Low)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
$n\overline{OEXX}$	$n\overline{EXX}$	$n\overline{LEXX}$	nAx or nBx	nBx or nAx	
H	X	X	X	Z	Disabled
X	H	X	X	Z	Disabled
L L	↑ ↑	L L	h l	Z Z	Disabled + Latch
L L	L L	↑ ↑	h l	H L	Latch + Display
L L	L L	L L	H L	H L	Transparent
L	L	H	X	NC	Hold

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High transition of $n\overline{LEXX}$ or $n\overline{EXX}$ (XX = AB or BA)
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High transition of $n\overline{LEXX}$ or $n\overline{EXX}$ (XX = AB or BA)
X = Don't care
↑ = Low-to-High transition of $n\overline{LEXX}$ or $n\overline{EXX}$ (XX = AB or BA)
NC= No change
Z = High impedance or "off" state

ABSOLUTE MAXIMUM RATINGS[2,3]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[4]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[4]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
2. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
3. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
4. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA				–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2			V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4			
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0			
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA				0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA				0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA				0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA				0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA				0.55	
V_{RST}	Power-up output low voltage[5]	V_{CC} = 3.6V; I_O = 1mA; V_I = GND or V_{CC}			0.13	0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins			±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V				10	
		V_{CC} = 3.6V; V_I = 5.5V	I/O Data pins[4]			20	
		V_{CC} = 3.6V; V_I = V_{CC}				10	
		V_{CC} = 3.6V; V_I = 0				-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V				±100	µA
I_{HOLD}	Bus Hold current A or B outputs	V_{CC} = 3V; V_I = 0.8V		75			µA
		V_{CC} = 3V; V_I = 2.0V		–75			µA
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V				125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care				±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0				0.12	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0				5	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0				0.12	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND				0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and .
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	2					ns
t_{PLH} t_{PHL}	Propagation delay n$\overline{LEBA}$ to nAx, n$\overline{LEAB}$ to nBx	1 2					ns
t_{PZH} t_{PZL}	Output enable time n$\overline{OEBA}$ to nAx, n$\overline{OEAB}$ to nBx	4 5					ns
t_{PHZ} t_{PLZ}	Output disable time n$\overline{OEBA}$ to nAx, n$\overline{OEAB}$ to nBx	4 5					ns
t_{PZH} t_{PZL}	Output enable time n$\overline{EBA}$ to nAx, n$\overline{EAB}$ to nBx	4 5					ns
t_{PHZ} t_{PLZ}	Output disable time n$\overline{EBA}$ to nAx, n$\overline{EAB}$ to nBx	4 5					ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

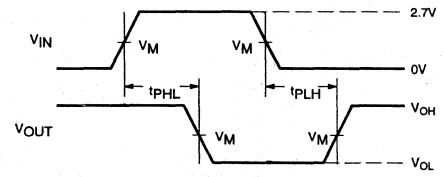
AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

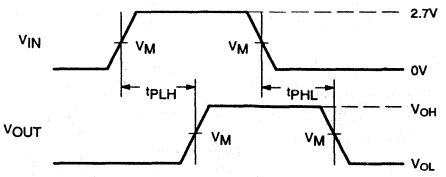
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V ±0.3V		V_{CC} = 2.7V	
			MIN	MAX	MIN	
t_s(H) t_s(L)	Setup time nAx to n$\overline{LEAB}$, nBx to n$\overline{LEBA}$	3				ns
t_h(H) t_h(L)	Hold time nAx to n$\overline{LEAB}$, nBx to n$\overline{LEBA}$	3				ns
t_s(H) t_s(L)	Setup time nAx to n$\overline{EAB}$, nBx to n$\overline{EBA}$	3				ns
t_h(H) t_h(L)	Hold time nAx to n$\overline{EAB}$, nBx to n$\overline{EBA}$	3				ns
t_W(L)	Latch enable pulse width, Low	3				ns

AC WAVEFORMS

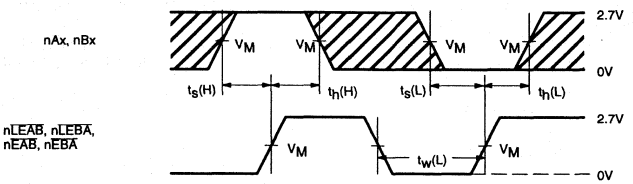
V_M = 1.5V, V_{IN} = GND to 3.0V



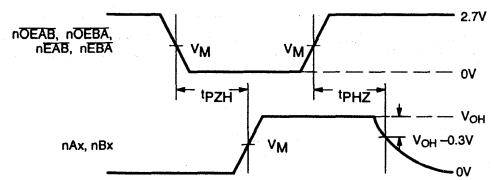
Waveform 1. Propagation Delay For Inverting Output



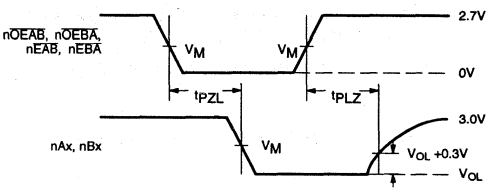
Waveform 2. Propagation Delay For Non-Inverting Output



Waveform 3. Data Setup and Hold Times and Latch Enable Pulse Width



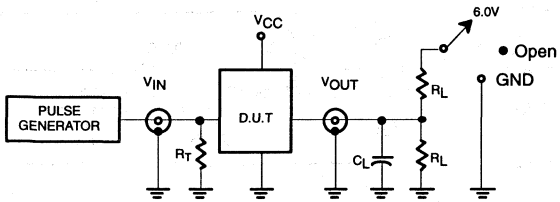
Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



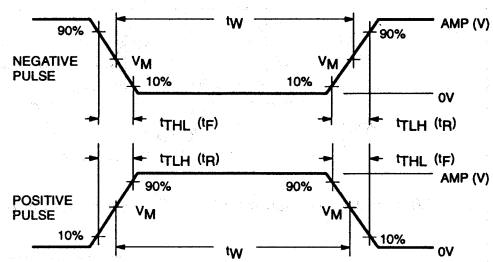
Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT16	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

3.3V ABT 16-bit bus transceiver (3-State) 74LVT16646A

FEATURES

- 16-bit universal bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Power-up reset
- Power-up 3-State
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT16646A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is a 16-bit transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an Output Enable ($\overline{OE}$) input for easy cascading and a Direction (DIR) input for direction control.

Data on the A or B bus is clocked into the registers on the Low to High transition of the appropriate clock (CPAB or CPBA). The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode data).

QUICK REFERENCE DATA

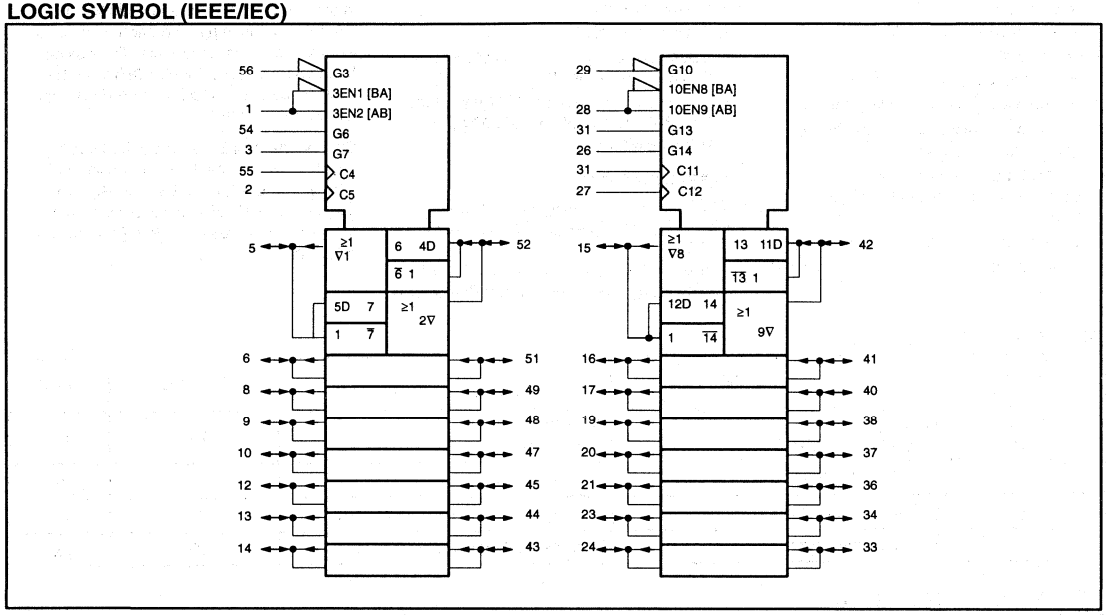
SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	C_L = 50pF; V_{CC} = 3.3V	2.4	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	4	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O}$ = 0V or 3.0V	10	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	100	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
56-Pin Plastic Shrink Small Outline (SSOP) Type III	–40°C to +85°C	74LVT16646ADL	SOT371-1
56-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	–40°C to +85°C	74LVT16646ADGG	SOT364-1

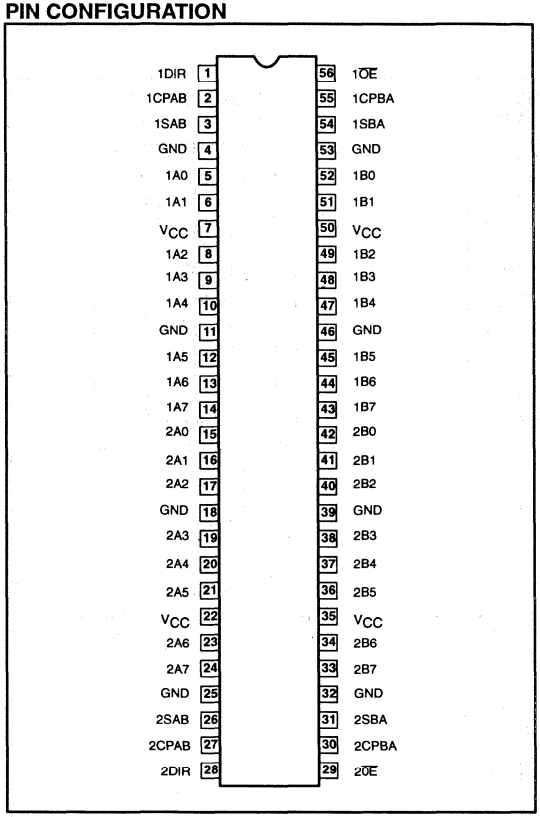
3.3V ABT 16-bit bus transceiver (3-State) 74LVT16646A

LOGIC SYMBOL (IEEE/IEC)

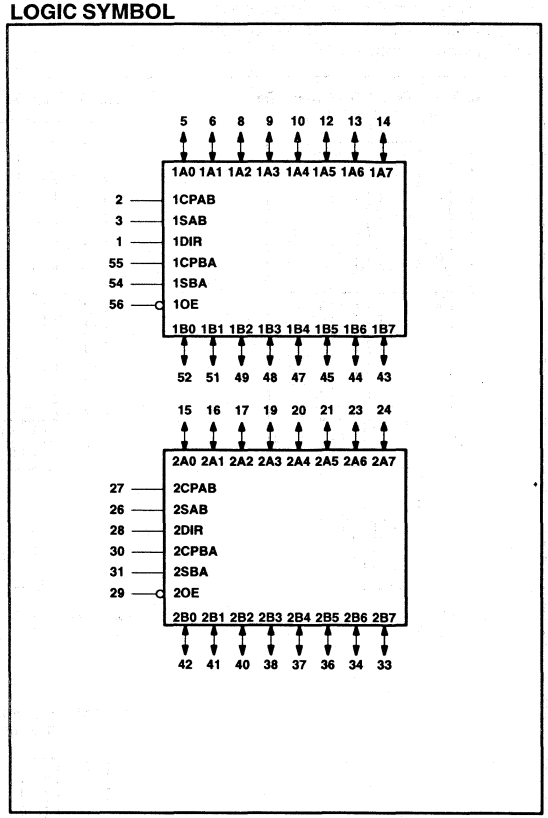


3.3V ABT 16-bit bus transceiver (3-State) 74LVT16646A

PIN CONFIGURATION



LOGIC SYMBOL

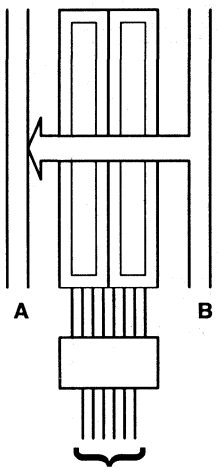


PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 55, 27, 30	1CPAB, 1CPBA, 2CPAB, 2CPBA	Clock input A to B / Clock input B to A
3, 54, 26, 31	1SAB, 1SBA, 2SAB, 2SBA	Select input A to B / Select input B to A
1, 28	1DIR, 2DIR	Direction control inputs
5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24	1A0 – 1A7, 2A0 – 2A7	Data inputs/outputs (A side)
52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33	1B0 – 1B7, 2B0 – 2B7	Data inputs/outputs (B side)
56, 29	$1\overline{OE}$, $2\overline{OE}$	Output enable inputs
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

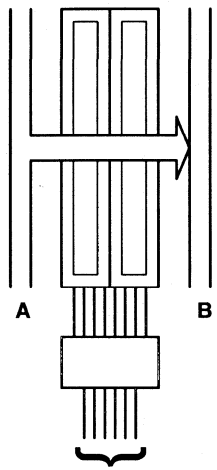
The following examples demonstrate the four fundamental bus-management functions that can be performed with the 74LVT16646A.

REAL TIME BUS TRANSFER BUS B TO BUS A



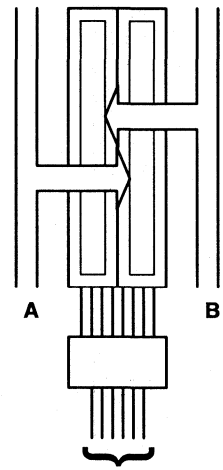
$n\overline{OE}$	nDIR	nCPAB	nCPBA	nSAB	nSBA
L	L	X	X	X	L

REAL TIME BUS TRANSFER BUS A TO BUS B



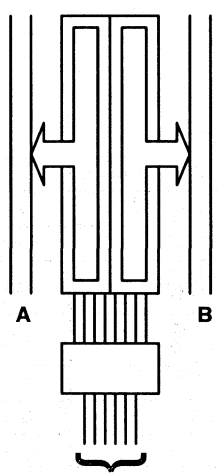
$n\overline{OE}$	nDIR	nCPAB	nCPBA	nSAB	nSBA
L	H	X	X	L	X

STORAGE FROM A, B, OR A AND B



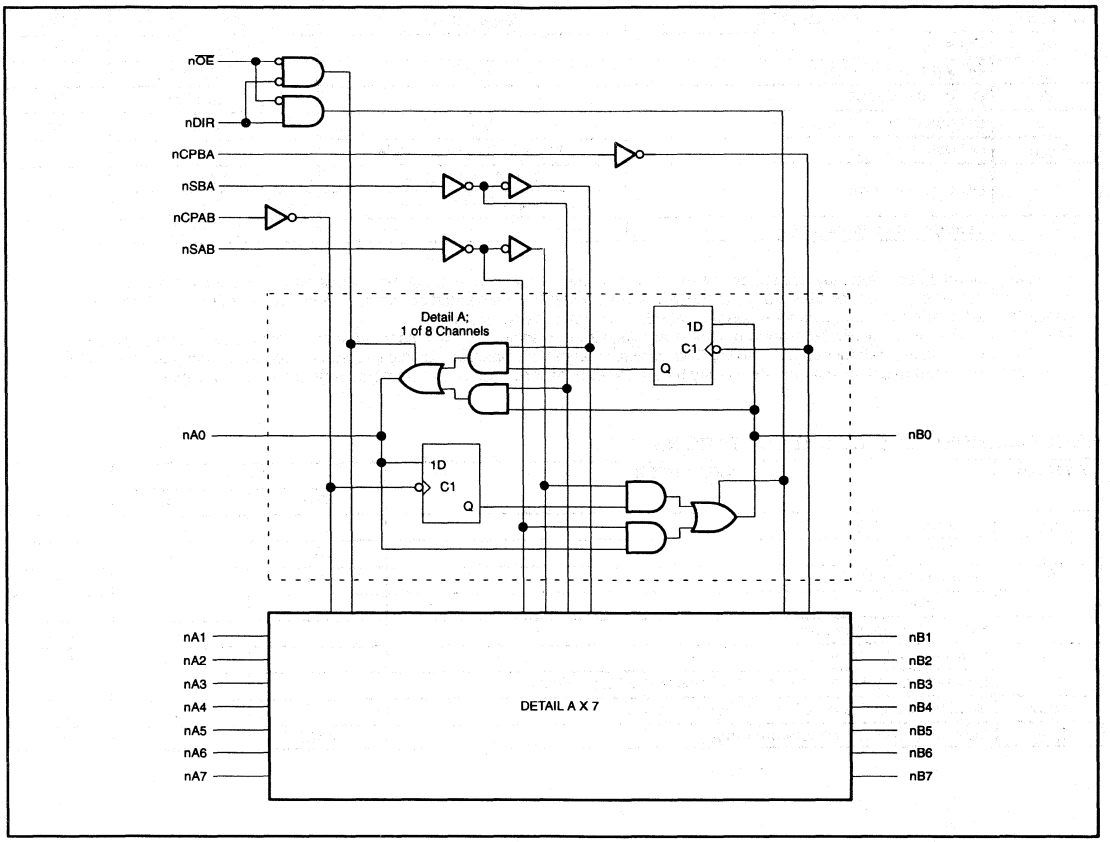
$n\overline{OE}$	nDIR	nCPAB	nCPBA	nSAB	nSBA
L	H	↑	X	X	X
L	L	X	↑	X	X
H	X	↑	↑	X	X

TRANSFER STORED DATA TO A OR B



$n\overline{OE}$	nDIR	nCPAB	nCPBA	nSAB	nSBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
$n\overline{OE}$	nDIR	nCPAB	nCPBA	nSAB	nSBA	nAx	nBx	
X	X	↑	X	X	X	Input	Unspecified output*	Store A, B unspecified
X	X	X	↑	X	X	Unspecified output*	Input	Store B, A unspecified
H H	X X	↑ H or L	↑ H or L	X X	X X	Input	Input	Store A and B data Isolation, hold storage
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time B data to A bus Stored B data to A bus
L L	H H	X H or L	X X	L H	X X	Input	Output	Real time A data to B bus Stored A data to B bus

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
* The data output function may be enabled or disabled by various signals at the $n\overline{OE}$ input. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

ABSOLUTE MAXIMUM RATINGS[1,2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2	V_{CC}		V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4	2.5		
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.3		
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			.07	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			.03	0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[5]	V_{CC} = 3.6V; I_O = 1mA; V_I = GND or V_{CC}				0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.1	10	
		V_{CC} = 3.6V; V_I = 5.5V	I/O Data pins[4]		0.1	20	
		V_{CC} = 3.6V; V_I = V_{CC}			0.5	10	
		V_{CC} = 3.6V; V_I = 0			0.1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current A or B outputs	V_{CC} = 3V; V_I = 0.8V		75	130		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–140		µA
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			50	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq 1.2V$; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}/OE$ = Don't care			35	±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.1	0.12	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			4.9	6	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0			0.1	0.12	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a. transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = −40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
f_{MAX}	Maximum clock frequency	1	150				MHz
t_{PLH} t_{PHL}	Propagation delay nCPAB to nBx or nCPBA to nAx	1	1.5 1.5	2.7 2.4	4.5 4.5	5.3 5.2	ns
t_{PLH} t_{PHL}	Propagation delay nSAB to nBx or nSBA to nAx	2	1.0 1.0	2.5 2.8	4.9 4.9	5.7 5.7	ns
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	2,3	0.5 0.5	1.6 1.9	3.7 3.7	4.3 4.4	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	5 6	1.0 1.0	2.7 2.5	4.3 4.4	5.1 5.2	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	5 6	1.5 1.5	3.2 2.9	5.2 4.6	5.5 4.7	ns
t_{PZH} t_{PZL}	Output Enable time nDIR to nAx or nBx	5 6	1.0 1.0	2.9 2.8	4.5 4.6	5.3 5.3	ns
t_{PHZ} t_{PLZ}	Output Disable time nDIR to nAx or nBx	5 6	1.0 1.0	3.1 2.9	5.7 5.2	6.6 5.7	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

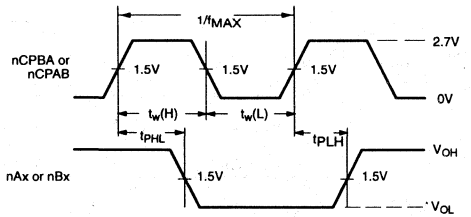
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω; T_{amb} = −40°C to +85°C.

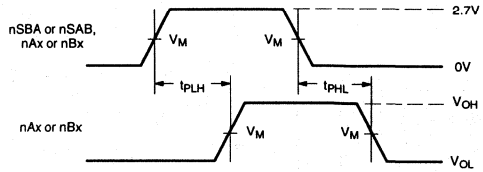
SYMBOL	PARAMETER	WAVEFORM					UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V	
			MIN	TYP	MAX	MIN	
ts(H) ts(L)	Setup time, High or Low nAx to nCPAB or nBx to nCPBA	4	1.0 1.9	0.6 0.4		1.1 2.4	ns
th(H) th(L)	Hold time, High or Low nAx to nCPAB or nBx to nCPBA	4	1.0 1.0	0.4 0.5		1.0 1.0	ns
tw(H) tw(L)	Pulse width, High or Low nCPAB or nCPBA	1	2.6 2.8	2.2 2.4		2.6 2.8	ns

AC WAVEFORMS

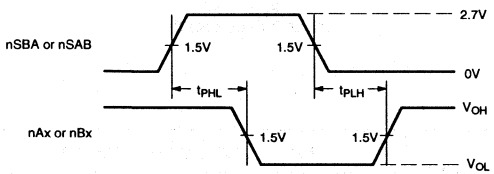
V_M = 1.5V, V_{IN} = GND to 2.7V



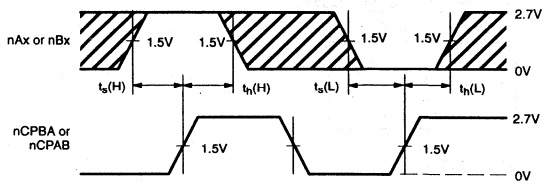
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



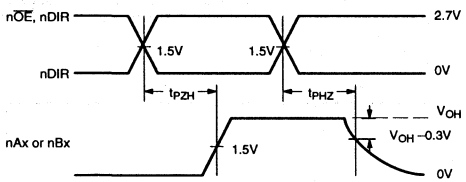
Waveform 2. Propagation Delay, Select to Outputs, A to B or B to A (non-inverting)



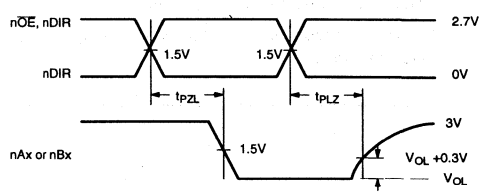
Waveform 3. Propagation Delay, Select to Outputs (inverting)



Waveform 4. Data Setup and Hold Times



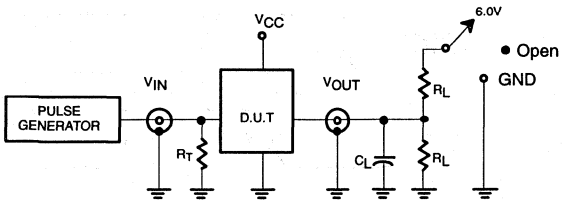
Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level



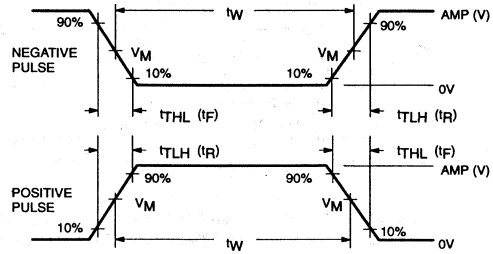
Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT16	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

3.3V ABT 16-bit bus transceiver and registers (3-State)

74LVT16652A

FEATURES

- 16–bit bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT16652A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

Complimentary output-enable (OEAB and $\overline{OEBA}$) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A Low-input level selects real-time data, and a High input level selects stored data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data.

Data on the A or B bus, or both, can be stored in the internal flip-flops by Low-to-High transitions at the appropriate clock (CPAB or CPBA) inputs regardless of the levels on the select-control or output-enable inputs. When SAB and SBA are in real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{OEBA}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last level configuration.

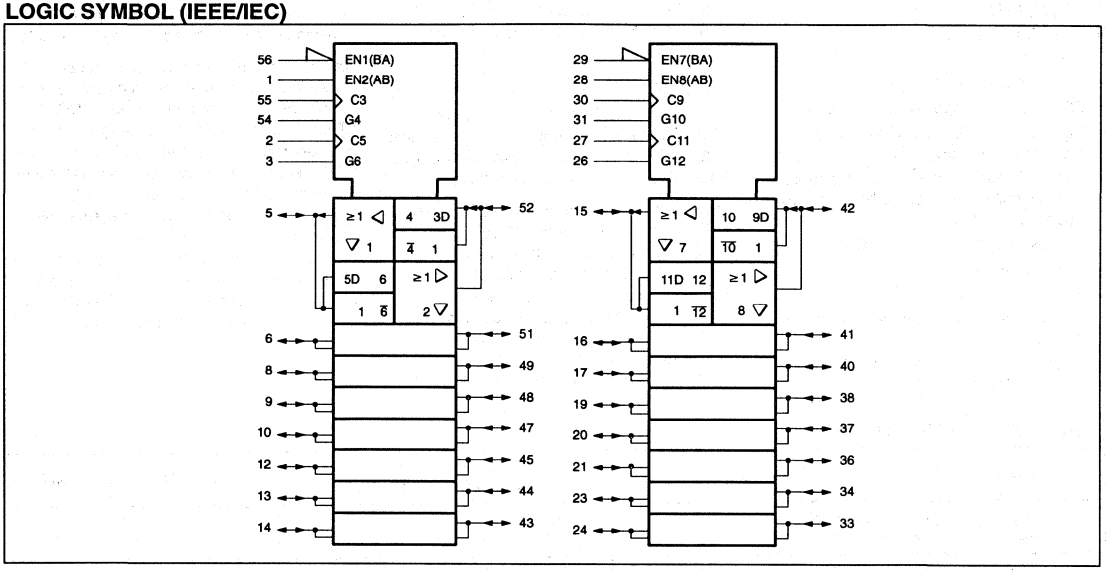
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	C_L = 50pF; V_{CC} = 3.3V		ns
C_{IN}	Input capacitance Control pins	V_I = 0V or 3.0V	4	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; V_I = 0V or 3.0V	10	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	100	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
56-Pin Plastic Shrink Small Outline (SSOP) Type III	–40°C to +85°C	74LVT16652ADL	SOT371-1
56-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	–40°C to +85°C	74LVT16652ADGG	SOT364-1

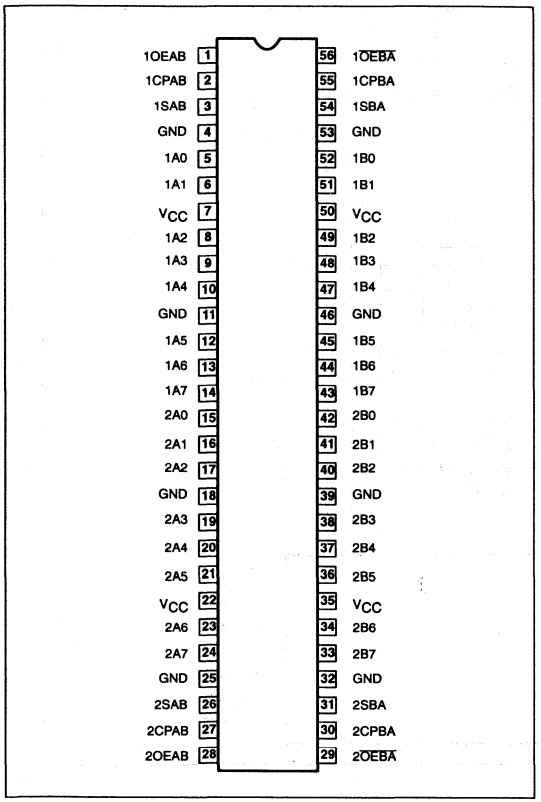
LOGIC SYMBOL (IEEE/IEC)



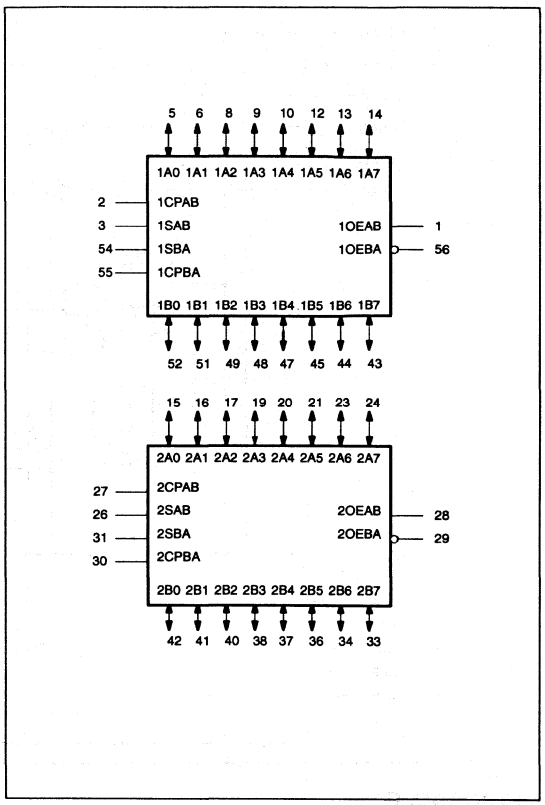
3.3V ABT 16-bit bus transceiver and registers (3-State)

74LVT16652A

PIN CONFIGURATION



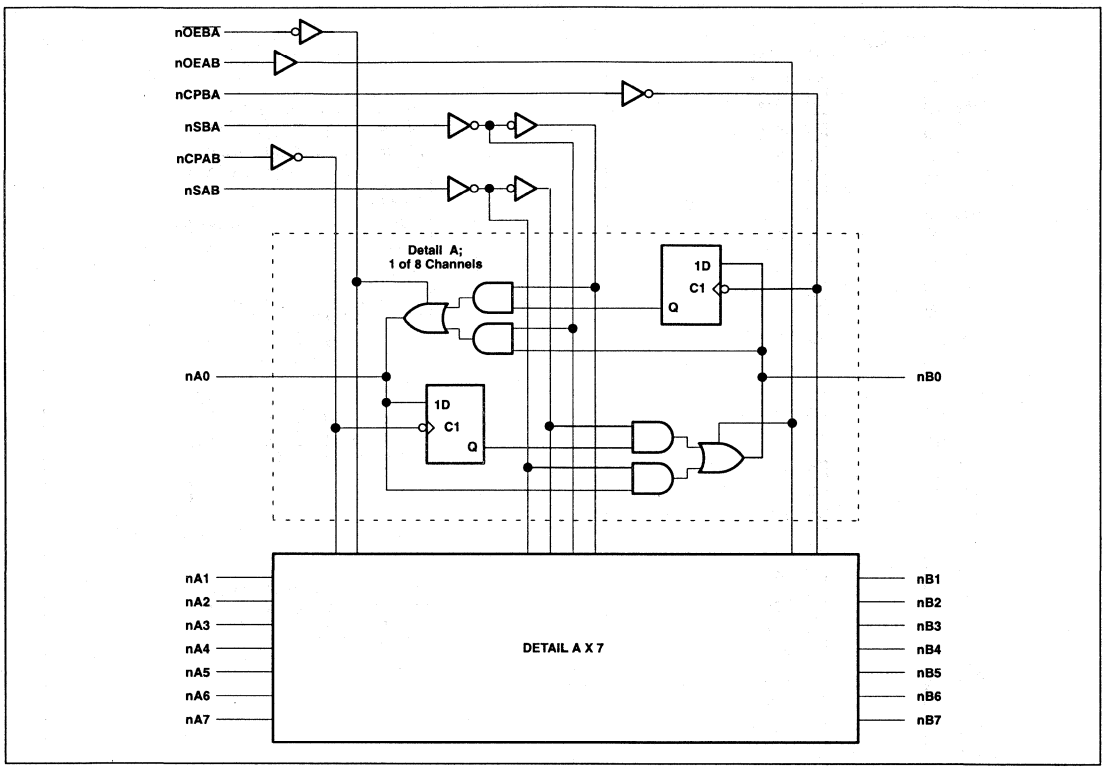
LOGIC SYMBOL



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 55, 27, 30	1CPAB, 1CPBA, 2CPAB, 2CPBA	Clock input A to B / Clock input B to A
3, 54, 26, 31	1SAB, 1SBA, 2SAB, 2SBA	Select input A to B / Select input B to A
5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24	1A0 – 1A7, 2A0 – 2A7	Data inputs/outputs (A side)
52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33	1B0 – 1B7, 2B0 – 2B7	Data inputs/outputs (B side)
1, 56, 28, 29	1OEAB, 1$\overline{\text{OEBA}}$, 2OEAB, 2$\overline{\text{OEBA}}$	Output enable inputs
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
nOEAB	$\overline{nOEBA}$	nCPAB	nCPBA	nSAB	nSBA	nAx	nBx	
L L	H H	H or L ↑	H or L ↑	X X	X X	Input	Input	Isolation Store A and B data
X H	H H	↑ ↑	H or L ↑	X **	X X	Input	Unspecified output*	Store A, Hold B Store A in both registers
L L	X L	H or L ↑	↑ ↑	X X	X **	Unspecified output*	Input	Hold A, Store B Store B in both registers
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time B data to A bus Stored B data to A bus
H H	H H	X H or L	X X	L H	X X	Input	Output	Real time A data to B bus Store A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus Stored B data to A bus

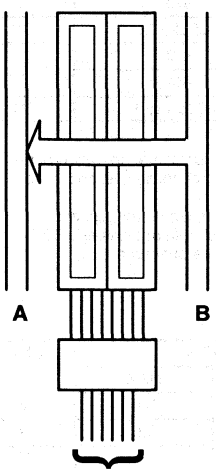
H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
* The data output function may be enabled or disabled by various signals at the $\overline{nOEBA}$ and nOEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.
** If both Select controls (nSAB and nSBA) are Low, then clocks can occur simultaneously. If either Select control is High, the clocks must be staggered in order to load both registers.

3.3V ABT 16-bit bus transceiver and registers (3-State)

74LVT16652A

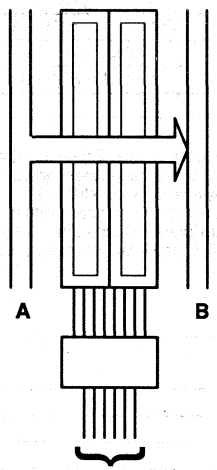
The following examples demonstrate the four fundamental bus-management functions that can be performed with the 74ABT16652.The select pins determine whether data is stored or transferred through the device in real time. The output enable pins determine the direction of the data flow.

REAL TIME BUS TRANSFER BUS B TO BUS A



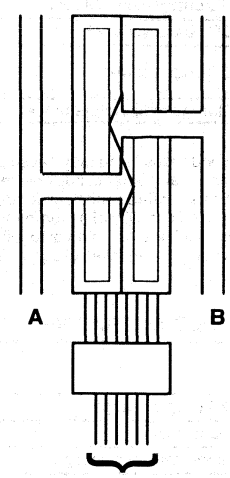
nOEAB	nOEBA	nCPAB	nCPBA	nSAB	nSBA
L	L	X	X	X	L

REAL TIME BUS TRANSFER BUS A TO BUS B



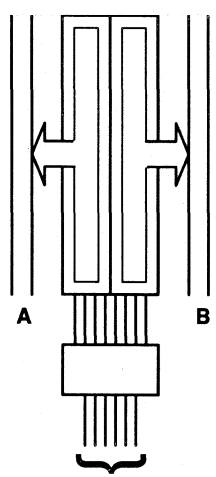
nOEAB	nOEBA	nCPAB	nCPBA	nSAB	nSBA
H	H	X	X	L	X

STORAGE FROM A, B, OR A AND B



nOEAB	nOEBA	nCPAB	nCPBA	nSAB	nSBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

TRANSFER STORED DATA TO A OR B



nOEAB	nOEBA	nCPAB	nCPBA	nSAB	nSBA
H	L	H|L	H|L	H	H

ABSOLUTE MAXIMUM RATINGS[1,2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA				–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2			V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4			
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0			
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA				0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA				0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA				0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA				0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA				0.55	
V_{RST}	Power-up output low voltage[5]	V_{CC} = 3.6V; I_O = 1mA; V_I = GND or V_{CC}				0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins			±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V				10	
		V_{CC} = 3.6V; V_I = 5.5V	I/O Data pins[4]			20	
		V_{CC} = 3.6V; V_I = V_{CC}				10	
		V_{CC} = 3.6V; V_I = 0				-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V				±100	µA
I_{HOLD}	Bus Hold current A or B outputs	V_{CC} = 3V; V_I = 0.8V		75			µA
		V_{CC} = 3V; V_I = 2.0V		–75			µA
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V				125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care				±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0				0.12	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0				2	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0				0.12	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND				0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ± 0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
f_{MAX}	Maximum clock frequency	1	150	180			MHz
t_{PLH} t_{PHL}	Propagation delay nCPAB to nBx or nCPBA to nAx	1	1.8 2.0	3.7 3.7	6.0 5.7	6.9 6.4	ns
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	2	1.2 1.0	2.8 2.6	4.7 4.6	5.5 5.3	ns
t_{PLH} t_{PHL}	Propagation delay nSAB to nBx or nSBA to nAx	3	1.4 1.4	3.7 4.0	6.4 6.2	7.6 6.8	ns
t_{PZH} t_{PZL}	Output enable time $n\overline{OEBA}$ to nAx	5 6	1.0 1.0	2.9 3.0	5.8 6.0	7.2 7.3	ns
t_{PHZ} t_{PLZ}	Output disable time $n\overline{OEBA}$ to nAx	5 6	2.2 1.8	3.9 3.2	6.5 5.8	6.9 5.9	ns
t_{PZH} t_{PZL}	Output enable time nOEAB to nBx	5 6	1.0 1.2	3.3 3.4	6.5 6.3	7.5 7.1	ns
t_{PHZ} t_{PLZ}	Output disable time nOEAB to nBx	5 6	1.7 1.5	4.5 3.8	7.2 5.8	8.1 6.3	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC SETUP REQUIREMENTS

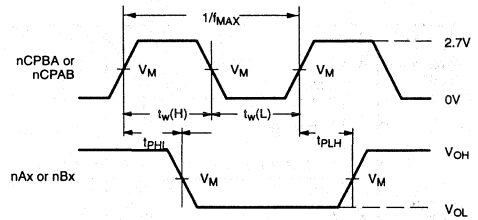
GND = 0V, t_R = 2.5ns, t_F = 2.5ns, C_L = 50pF, R_L = 500Ω, T_{amb} = –40 °C to +85 °C

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V	
			Min	Typ	Max	Min	
t_s(H) t_s(L)	Setup time [1] nAx to nCPAB, nBx to nCPBA	4	1.5 2.2	0.9 1.1		1.6 2.5	ns
t_h(H) t_h(L)	Hold time [1] nAx to nCPAB, nBx to nCPBA	4	0 0	–1.0 –1.0		0.0 0.0	ns
t_w(H) t_w(L)	Pulse width, High or Low nCPAB or nCPBA	1	3.3 3.3	1.0 2.0		3.3 3.3	ns

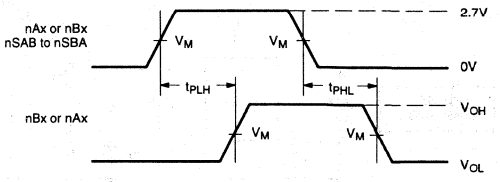
NOTE:
1. This data sheet limit may vary among suppliers.

AC WAVEFORMS

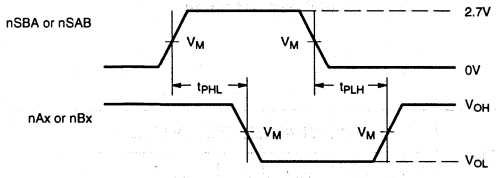
V_M = 1.5V, V_{IN} = GND to 3.0V



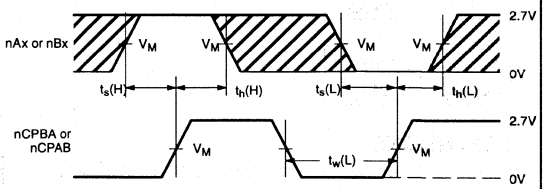
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



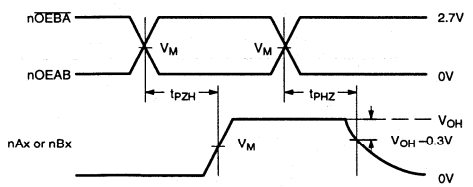
Waveform 2. Propagation Delay, nAx to nBx or nBx to nAx, nSAB to Bn or nSBA to An



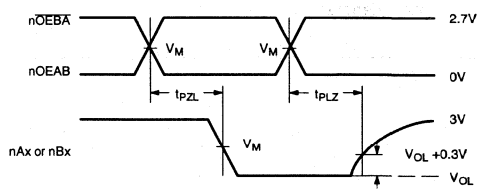
Waveform 3. Propagation Delay, SBA to nAx or SAB to nBx



Waveform 4. Data Setup and Hold Times



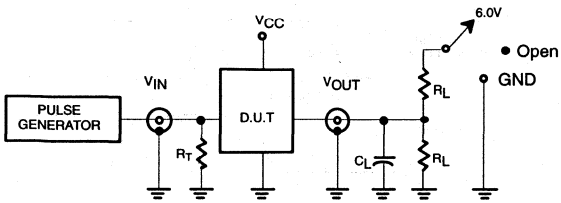
Waveform 5. 3–State Output Enable Time to High Level and Output Disable Time from High Level



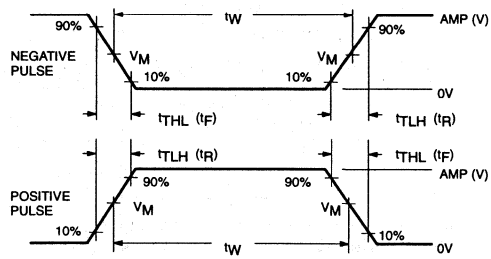
Waveform 6. 3–State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT16	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

DEVICE DATA
PLDs

3 Volt zero standby power universal PAL devices

P3C18V8Z35/P3C18V8ZI

DESCRIPTION

The P3C18V8Z is a universal PAL-type device designed to operate specifically in a low voltage environment (3.3V). Per JEDEC, the P3C18V8Z can support a regulated operating supply voltage, 3.0 to 3.6V and an unregulated (battery) operating supply voltage, 2.7 to 3.6V, at 21 and 18 MHz, respectively. The PAL device is available in the commercial temperature range, P3C18V8Z35, and the industrial temperature range, P3C18V8ZI.

These devices offer virtually zero standby power (20µA typical) as well as very low power consumption during operation (23mA worst case in combinatorial configuration). The P3C18V8Z automatically powers down when the inputs or the clock are idle for greater than one full clock cycle. The device will automatically power up from a standby mode once any input or the clock is activated. This input transition detection circuitry makes these devices ideal for power sensitive applications — especially those which are battery operated or backed up.

All the P3C18V8Z devices are available in plastic DIP, PLCC and Plastic Small Outline (SOL) packages. A ceramic DIP with a window for erasure is available for prototyping.

The P3C18V8Z is a two level logic element comprised of 10 inputs, 74 AND gates (logic and control product terms) and 8 Output Macro Cells (OMCs). Each OMC can be configured as a dedicated input, a combinatorial I/O or a registered output with internal feedback. Each OMC has individual direction control (from the AND array) and programmable output polarity. The dedicated clock and OE pins can be configured as inputs for strictly combinatorial applications. Two product terms control the asynchronous Reset and the synchronous Preset functions.

Power up Reset and Register Preload functions have also been incorporated into the P3C18V8Z to facilitate state machine design and testing.

The Output Macro Cell feature of the P3C18V8Z devices provides the flexibility to emulate all 20 pin common PAL and GAL functions, thus providing reduced documentation, inventory and manufacturing costs. The P3C18V8Z is also pin and fuse map compatible with all the Philips 5 Volt P3C18V8Z devices.

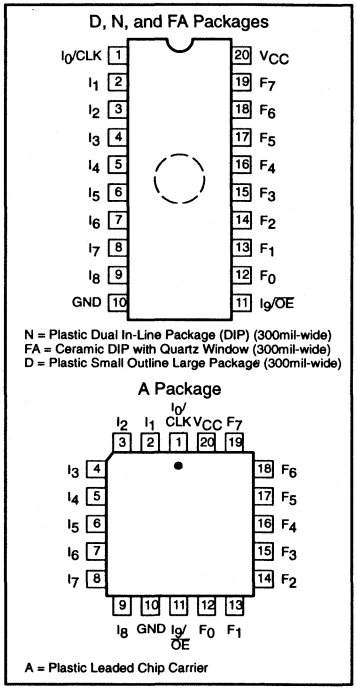
FEATURES

- 20-pin Universal Programmable Array Logic (PAL), operational over low voltage ranges
  - 3.0 to 3.6V (35ns T_{PD}/21 MHz f_{MAX})
  - 2.7 to 3.6V (40ns T_{PD}/18 MHz f_{MAX})
- Virtually zero-standby-power and very low dynamic power
  - 20µA standby (typ.)
  - 0.8 mA/MHz (worst case)
- Functional replacement for Series 16 PALs and GALs
  - Highly flexible Output Macro Cell
- Available in DIP, PLCC and SOL (Small Outline) packages
- High performance EPROM CMOS cell technology
  - 100% testable prior to programming
  - Low cost OTP plastic packages
  - Erasable/reconfigurable (ceramic package)
- Design support provided by most popular third party programmable Logic CAD tools

APPLICATIONS

- Laptop, notebook and palm top computers
- Portable communications equipment
- Battery power/backed instruments
- Industrial automation/control

PIN CONFIGURATIONS



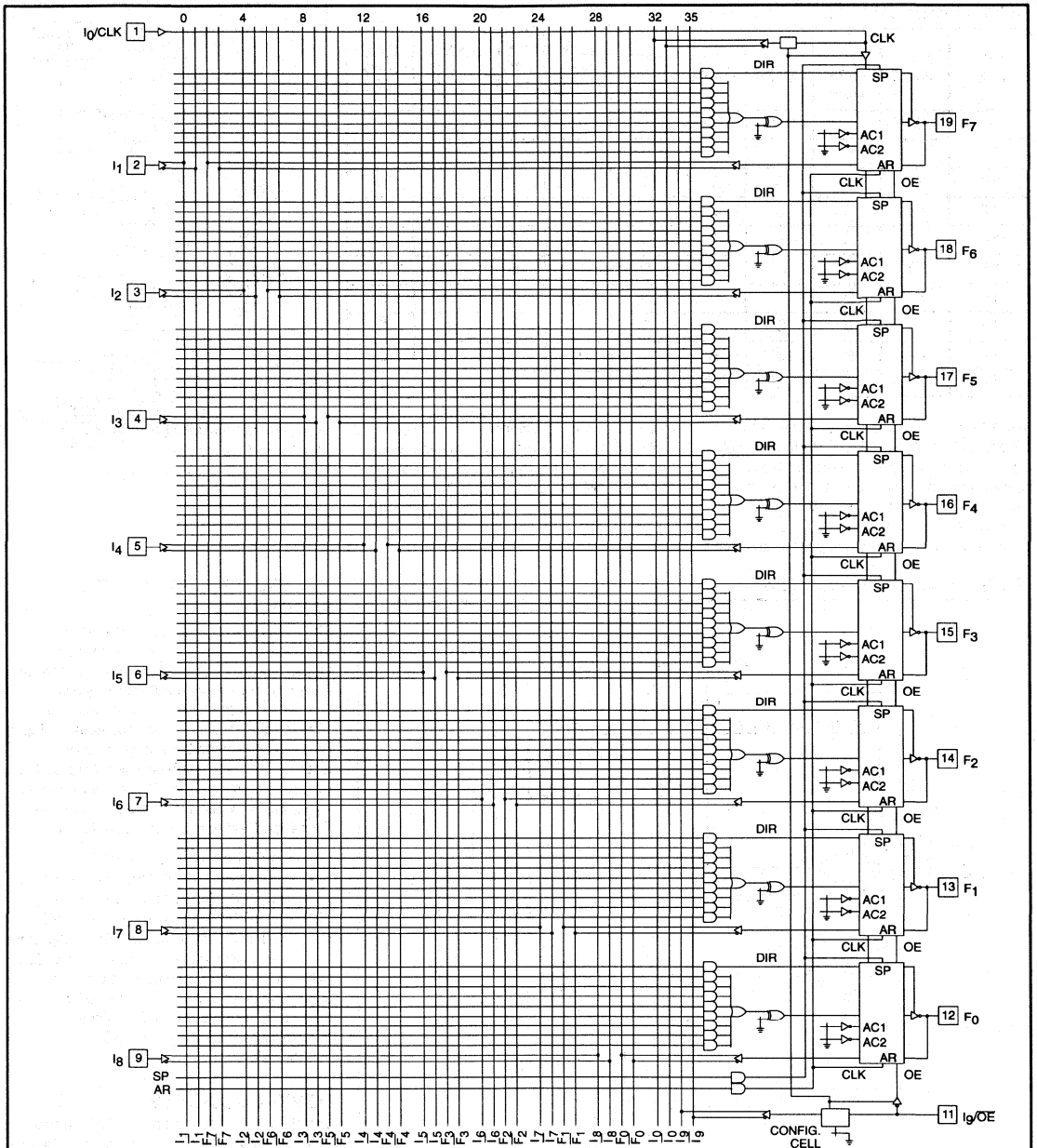
PIN DESCRIPTIONS

I	Dedicated Input
F	Output/Input Macrocell
CLK	Clock Input
$\overline{OE}$	Output Enable
V_{CC}	Supply Voltage
GND	Ground

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-Pin (300mil-wide) Plastic Dual In-Line Package	Commercial	P3C18V8Z35N	0408B
20-Pin (300mil-wide) Ceramic Dual In-Line Package with quartz window		P3C18V8Z35FA	0584B
20-Pin (350mil square) Plastic Leaded Chip Carrier Package		P3C18V8Z35A	0400E
20-Pin (300mil-wide) Plastic Small Outline Large Package		P3C18V8Z35D	0172D
20-Pin (300mil-wide) Plastic Dual In-Line Package	Industrial	P3C18V8ZIN	0408B
20-Pin (300mil-wide) Ceramic Dual In-Line Package with quartz window		P3C18V8ZIFA	0584B
20-Pin (350mil square) Plastic Leaded Chip Carrier Package		P3C18V8ZIA	0400E
20-Pin (300mil-wide) Plastic Small Outline Large Package		P3C18V8ZID	0172D

LOGIC DIAGRAM



NOTES:
In the unprogrammed or virgin state:

All cells are in a conductive state.
All AND gate locations are pulled to a logic "0" (Low).
Output polarity is inverting.

Pins 1 and 11 are configured as Inputs 0 and 9, respectively, via the configuration cell. The clock and $\overline{OE}$ functions are disabled.
All output macro cells (OMC) are configured as bidirectional I/O, with the outputs disabled via the direction term.
Denotes a programmable cell location.

3 Volt zero standby power universal PAL devices

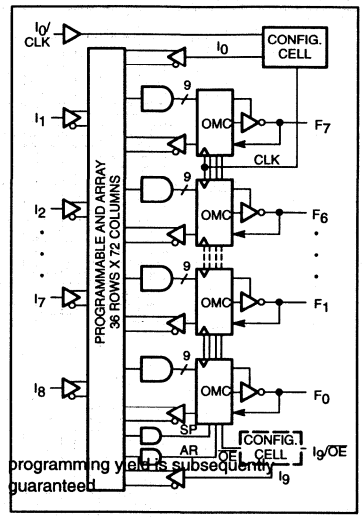
P3C18V8Z35/P3C18V8ZI

PAL DEVICE TO P3C18V8Z OUTPUT PIN CONFIGURATION CROSS REFERENCE

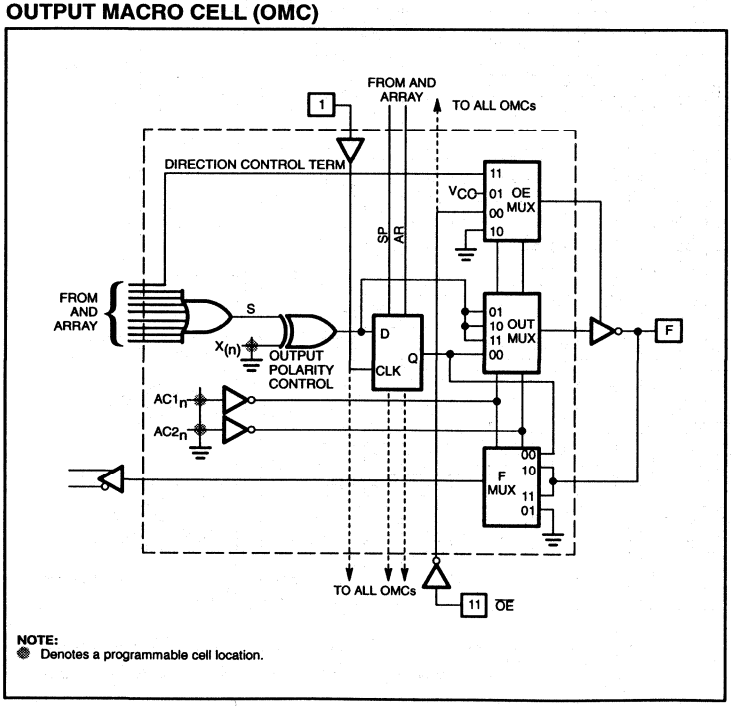
PIN NO.	P3C 18V8Z	16L8 16H8 16P8 16P8	16R4 16RP4	16R6 16RP6	16R8 16RP8	16L2 16H2 16P2	14L4 14H4 14P4	12L6 12H6 12P6	10L8 10H8 10P8
1	I_0/CLK	I	CLK	CLK	CLK	I	I	I	I
19	F7	B	B	B	D	I	I	I	O
18	F6	B	B	D	D	I	I	O	O
17	F5	B	D	D	D	I	O	O	O
16	F4	B	D	D	D	O	O	O	O
15	F3	B	D	D	D	O	O	O	O
14	F2	B	D	D	D	I	O	O	O
13	F1	B	B	D	D	I	I	O	O
12	F0	B	B	B	D	I	I	I	O
11	I_9/$\overline{OE}$	I	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	I	I	I	I

The Philips Semiconductors' state-of-the-art Floating-Gate CMOS EPROM process yields bipolar equivalent performance at less than one-quarter the power consumption. The erasable nature of the EPROM process enables Philips Semiconductors to functionally test the devices prior to shipment to the customer. Additionally, this allows Philips Semiconductors to extensively stress test, as well as ensure the threshold voltage of each individual EPROM cell. 100% programming yield is subsequently guaranteed.

FUNCTIONAL DIAGRAM



OUTPUT MACRO CELL (OMC)



NOTE:
● Denotes a programmable cell location.

THE OUTPUT MACRO CELL (OMC)

The P3C18V8Z series devices have 8 individually programmable Output Macro Cells. The 72 AND inputs (or product terms) from the programmable AND array are connected to the 8 OMCs in groups of 9. Eight of the AND terms are dedicated to logic functions; the ninth is for asynchronous direction control, which enables/disables the respective bidirectional I/O pin. Two product terms are dedicated for the Synchronous Preset and Asynchronous Reset functions.

Each OMC can be independently programmed via 16 architecture control bits, $AC1_n$ and $AC2_n$ (one pair per macro cell). Similarly, each OMC has a programmable output polarity control bit (Xn). By configuring the pair of architecture control bits according to the configuration cell table, 4 different configurations may be implemented. Note that the configuration cell is automatically programmed based on the OMC configuration.

DESIGN SECURITY

The P3C18V8Z series devices have a programmable security fuse that controls the access to the data programmed in the device. By using this programmable feature, proprietary designs implemented in the device cannot be copied or retrieved.

CONFIGURATION CELL

A single configuration cell controls the functions of Pins 1 and 11. Refer to Functional Diagram. When the configuration cell is programmed, Pin 1 is a dedicated clock and Pin 11 is dedicated for output enable. When the configuration cell is unprogrammed, Pins 1 and 11 are both dedicated inputs. Note that the output enable for all registered OMCs is common—from Pin 11 only. Output enable control of the bidirectional I/O OMCs is provided from the AND array via the direction product term.

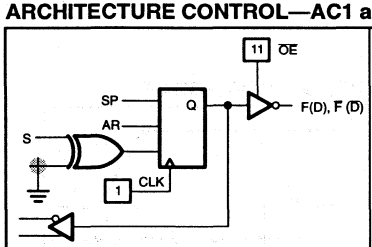
If any one OMC is configured as registered, the configuration cell will be automatically configured (via the design software) to ensure that the clock and output enable functions are enabled on Pins 1 and 11, respectively. If none of the OMCs are registered, the configuration cell will be programmed such that Pins 1 and 11 are dedicated inputs. The programming codes are as follows:

Pin 1 = CLK, Pin 11 = $\overline{OE}$	L
Pin 1 and Pin 11 = Input	H

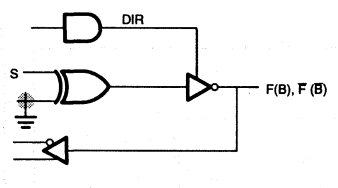
FUNCTION	CONTROL CELL CONFIGURATIONS			COMMENTS
	$AC1_1$	$AC2_N$	CONFIG. CELL	
Registered mode	Programmed	Programmed	Programmed	Dedicated clock from Pin 1. $\overline{OE}$ Control for all registerd OMCs from Pin 11 only.
Bidirectional I/O mode	Unprogrammed	Unprogrammed	Unprogrammed	Pins 1 and 11 are dedicated inputs. 3-State control from AND array only.
Fixed input mode	Unprogrammed	Programmed	Unprogrammed	Pins 1 and 11 are dedicated inputs.
Fixed output mode	Programmed	Unprogrammed	Unprogrammed	Pins 1 and 11 are dedicated inputs. The feedback path (via F_{MUX}) is disabled.

NOTE:
1. This is the virgin state as shipped from the factory.

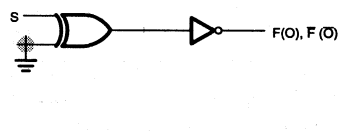
ARCHITECTURE CONTROL—AC1 and AC2



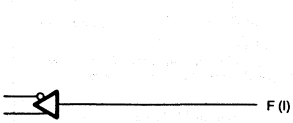
OMC CONFIGURATION	CODE
REGISTERED (D–TYPE)	D



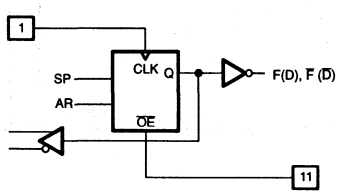
OMC CONFIGURATION	CODE
BIDIRECTIONAL I/O (COMBINATORIAL)	B



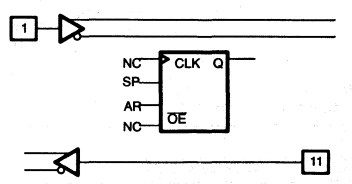
OMC CONFIGURATION	CODE
FIXED OUTPUT	O



OMC CONFIGURATION	CODE
FIXED INPUT	I



CONFIGURATION CELL	CODE
PIN 1 = CLK PIN 11 = $\overline{OE}$	L



CONFIGURATION CELL	CODE
PIN 1 = INPUT PIN 11 = INPUT	H^1

NOTES:
A factory shipped unprogrammed device is configured such that:
1. This configuration cannot be used if any OMCs are configured as registered (Code = D). The configuration cell will be automatically configured to ensure that the clock and output enable functions are enabled on Pins 1 and 11, respectively, if any one OMC is programmed as registered.
   * All AND gates are pulled to a logic "0" (Low).
   * Output polarity is inverting.
   * Pins 1 and 11 are configured as inputs 0 and 9. The clock and OE functions are disabled.
   * All Output Macro Cells (OMCs) are configured as bidirectional I/O, with the outputs disabled via the direction term.

ABSOLUTE MAXIMUM RATINGS[1]

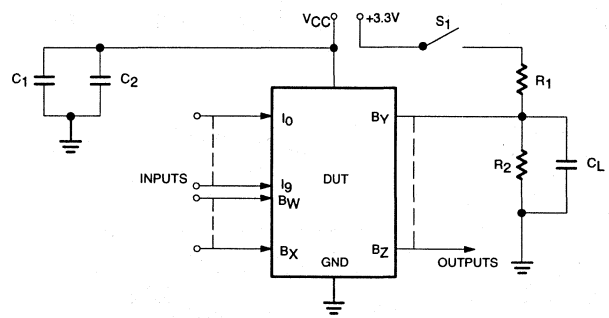
SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	–0.5 to +6	V_{DC}
V_{CC}	Operating supply voltage	2.7 to 3.6	V_{DC}
V_{IN}	Input voltage	–0.5 to V_{CC} +0.5	V_{DC}
V_{OUT}	Output voltage	–0.5 to V_{CC} +0.5	V_{DC}
$\Delta t/\Delta V$	Input/clock transition rise or fall[2]	200	ns/V maximum
I_{IN}	Input currents	–10 to +10	mA
I_{OUT}	Output currents	+24	mA
T_{amb}	Operating temperature range	–40 to +85 (Industrial) 0 to +75 (Commercial)	°C
T_{stg}	Storage temperature range	–65 to +150	°C

NOTES:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.
2. All digital circuits can oscillate or trigger prematurely when input rise and fall times are very long. When the input signal to a device is at or near the switching threshold, noise on the line will be amplified and can cause oscillation which, if the frequency is low enough, can cause subsequent stages to switch and give erroneous results. For this reason, external Schmitt-triggers are recommended if rise/fall times are likely to exceed 200ns at V_{CC} = 3.6V.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

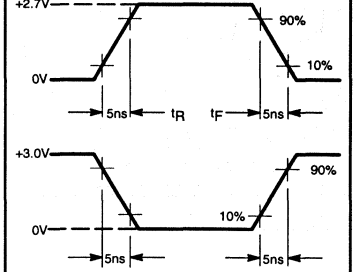
AC TEST CONDITIONS



NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

R1 = 200Ω R2 = 390Ω

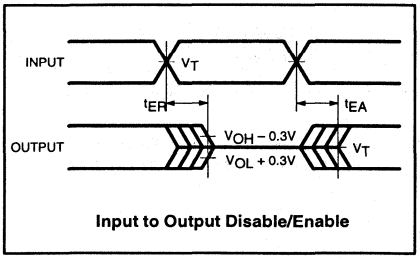
VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

SWITCHING WAVEFORM



Input to Output Disable/Enable

DC ELECTRICAL CHARACTERISTICS

2.7V ≤ V_{CC} ≤ 3.6 and 3.0V ≤ V_{CC} ≤ 3.6 ranges
Commercial = 0°C ≤ T_{amb} ≤ +75°C
Industrial = –40°C ≤ T_{amb} ≤ +85°C

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN	TYP[1]	MAX	
Input voltage						
V_{IL}	Low	V_{CC} = MIN	–0.3		0.8	V
V_{IH}	High	V_{CC} = MAX	2.0		V_{CC} + 0.3	V
Output voltage[2]						
V_{OL}	Low	V_{CC} = MIN, I_{OL} = 20µA V_{CC} = MIN, I_{OL} = 24mA			0.100 0.500	V V
V_{OH}	High	V_{CC} = 3.0, I_{OH} = –3.2mA V_{CC} = 3.0, I_{OH} = –20µA V_{CC} = 2.7, I_{OH} = –1.6µA	V_{CC} – 0.6 V_{CC} – 0.3 V_{CC} – 0.3			V V
Input current						
I_{IL}	Low[5]	V_{IN} = GND			–5	µA
I_{IH}	High	V_{IN} = V_{CC}			5	µA
Output current						
$I_{O(OFF)}$	Hi–Z state	V_{OUT} = V_{CC} V_{OUT} = GND			10 –10	µA µA
I_{OS}	Short-circuit[3]	V_{OUT} = GND			–130	mA
I_{CC}	V_{CC} supply current (Standby)	V_{CC} = MAX, V_{IN} = 0 or V_{CC}[6]		20	60	µA
I_{CC}/f	V_{CC} supply current (Active)[4]	V_{CC} = MAX			0.8	mA/MHz
Capacitance						
C_I	Input	V_{CC} = 5V V_{IN} = 2.0V		12		pF
C_B	I/O	V_B = 2.0V		15		pF

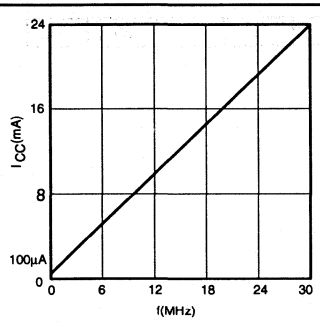


Figure 1. I_{CC} vs Frequency (Worst Case)

NOTES:
1. All typical values are at V_{CC} = 3.3V, T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Duration of short–circuit should not exceed one second. Test one at a time.
4. Measured with all outputs swtiching.
5. I_{IL} for Pin 1 (I_0/CLK) is ± 10µA with V_{IN} = 0.4V.
6. V_{IN} includes CLK and $\overline{OE}$ if applicable.

AC ELECTRICAL CHARACTERISTICS

3.0V ≤ V_{CC} ≤ 3.6V range; R_2 = 390Ω
Commercial = 0°C ≤ T_{amb} ≤ +75°C
Industrial = –40°C ≤ T_{amb} ≤ +85°C

SYMBOL	PARAMETER	FROM	TO	TEST CONDITION[1]	P3C18V8Z35 (Commercial)		P3C18V8ZI (Industrial)		UNIT
				C_L (pF)	MIN	MAX	MIN	MAX	
Pulse width									
t_{CKP}	Clock period (Minimum $t_{IS} + t_{CKO}$)	CLK +	CLK +	50	47		57		ns
t_{CKH}	Clock width High	CLK +	CLK –	50	20		25		ns
t_{CKL}	Clock width Low	CLK –	CLK +	50	20		25		ns
t_{ARW}	Async reset pulse width	I ±, F±	$\bar{I}$ ∓, $\bar{F}$ ∓		35		40		ns
Hold time									
t_{IH}	Input or feedback data hold time	CLK +	Input ±	50	0		0		ns
Setup time									
t_{IS}	Input or feedback data setup time	I ±, F±	CLK +	50	25		30		ns
Propagation delay									
t_{PD}	Delay from input to active output	I ±, F±	F±	50		35		40	ns
t_{CKO}	Clock High to output valid access Time	CLK +	F±	50		15		20	ns
t_{OE1}	Product term enable to outputs off	I ±, F±	F±	50		40		45	ns
t_{OD1}	Product term disable to outputs off	I ±, F±	F±	5		35		40	ns
t_{OD2}	Pin 11 output disable High to outputs off	OE –	F±	5		25		30	ns
t_{OE2}	Pin 11 output enable to active output	OE +	F±	50		30		35	ns
t_{ARD}	Async reset delay	I ±, F±	F +			35		40	ns
t_{ARR}	Async reset recovery time	I ±, F±	CLK +		25		30		ns
t_{SPR}	Sync preset recovery time	I ±, F±	CLK +		25		30		ns
t_{PPR}	Power-up reset	V_{CC} +	F +			35		40	ns
Frequency of operation									
f_{MAX}	Maximum frequency	1/($t_{IS} + t_{CKO}$)		50		25		20	MHz

NOTES:
1. Refer also to AC Test Conditions. (Test Load Circuit)

AC ELECTRICAL CHARACTERISTICS

$2.7V \leq V_{CC} \leq 3.6V$ range; $R_2 = 390\Omega$
Commercial = $0°C \leq T_{amb} \leq +75°C$
Industrial = $-40°C \leq T_{amb} \leq +85°C$

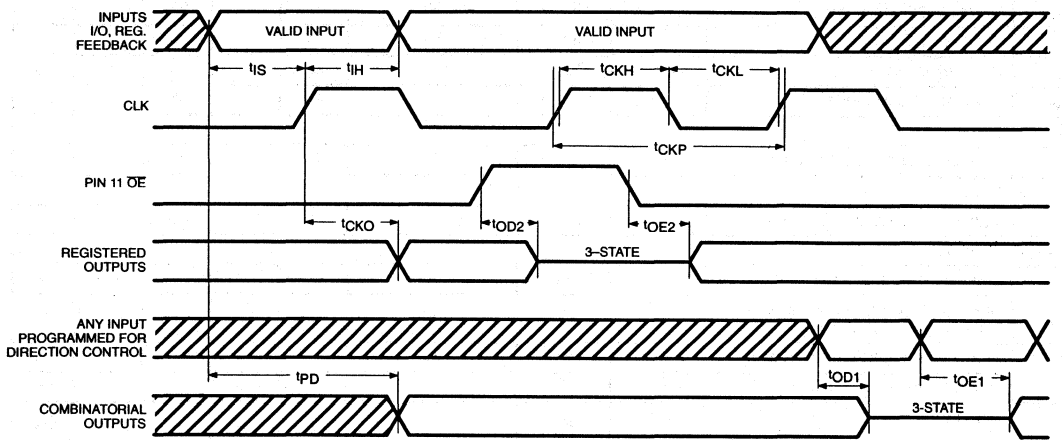
SYMBOL	PARAMETER	FROM	TO	TEST CONDITION[1] C_L (pF)	P3C18V8Z35 (Commercial) MIN	P3C18V8Z35 (Commercial) MAX	P3C18V8ZI (Industrial) MIN	P3C18V8ZI (Industrial) MAX	UNIT
Pulse width									
t_{CKP}	Clock period (Minimum $t_{IS} + t_{CKO}$)	CLK +	CLK +	50	57		57		ns
t_{CKH}	Clock width High	CLK +	CLK –	50	25		30		ns
t_{CKL}	Clock width Low	CLK –	CLK +	50	25		30		ns
t_{ARW}	Async reset pulse width	I ±, F±	I $\overline{+}$, F $\overline{+}$		40		45		ns
Hold time									
t_{IH}	Input or feedback data hold time	CLK +	Input ±	50	0		0		ns
Setup time									
t_{IS}	Input or feedback data setup time	I ±, F±	CLK +	50	30		35		ns
Propagation delay									
t_{PD}	Delay from input to active output	I ±, F±	F±	50		40		45	ns
t_{CKO}	Clock High to output valid access Time	CLK +	F±	50		17		22	ns
t_{OE1}	Product term enable to outputs off	I ±, F±	F±	50		45		50	ns
t_{OD1}	Product term disable to outputs off	I ±, F±	F±	5		40		45	ns
t_{OD2}	Pin 11 output disable High to outputs off	OE –	F±	5		30		35	ns
t_{OE2}	Pin 11 output enable to active output	OE +	F±	50		35		40	ns
t_{ARD}	Async reset delay	I ±, F±	F +			40		45	ns
t_{ARR}	Async reset recovery time	I ±, F±	CLK +		30		35		ns
t_{SPR}	Sync preset recovery time	I ±, F±	CLK +		30		35		ns
t_{PPR}	Power-up reset	V_{CC} +	F +			40		45	ns
Frequency of operation									
f_{MAX}	Maximum frequency	$1/(t_{IS} + t_{CKO})$		50		21		17	MHz

NOTES:
1. Refer also to AC Test Conditions. (Test Load Circuit)

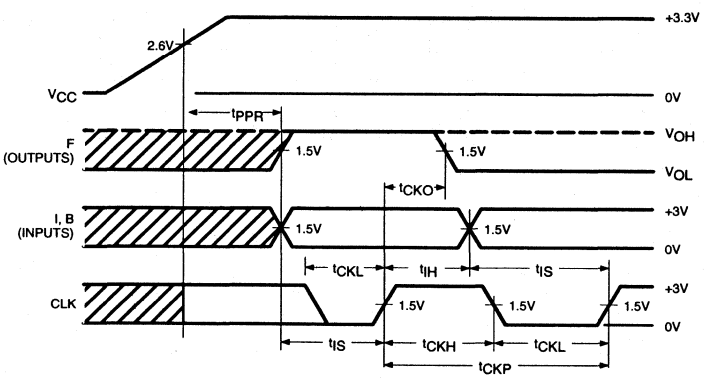
POWER-UP RESET

In order to facilitate state machine design and testing, a power-up reset function has been incorporated in the P3C18V8Z. All internal registers will reset to Active-Low (logical "0") after a specified period of time (t_{PPR}). Therefore, any OMC that has been configured as a registered output will always produce an Active-High on the associated output pin because of the inverted output buffer. The internal feedback (Q) of a registered OMC will also be set Low. The programmed polarity of OMC will not affect the Active-High output condition during a system power-up condition.

TIMING DIAGRAMS



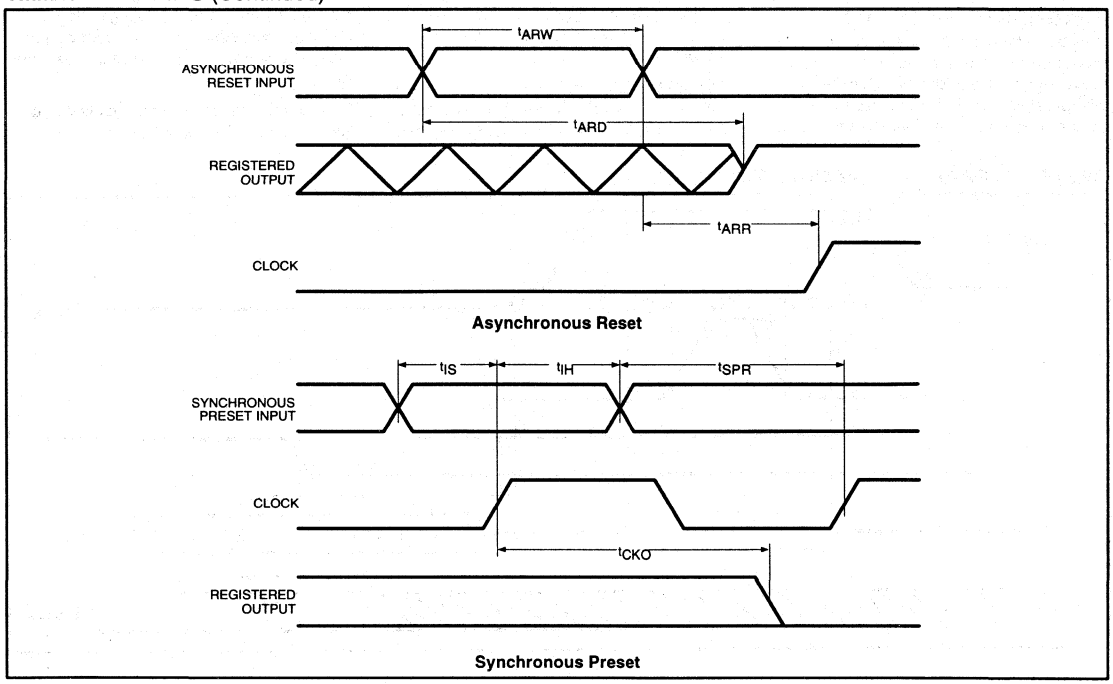
Switching Waveforms



NOTE:
Diagram presupposes that the outputs (F) are enabled. The reset occurs regardless of the output condition (enabled or disabled).

Power-Up Reset

TIMING DIAGRAMS (Continued)



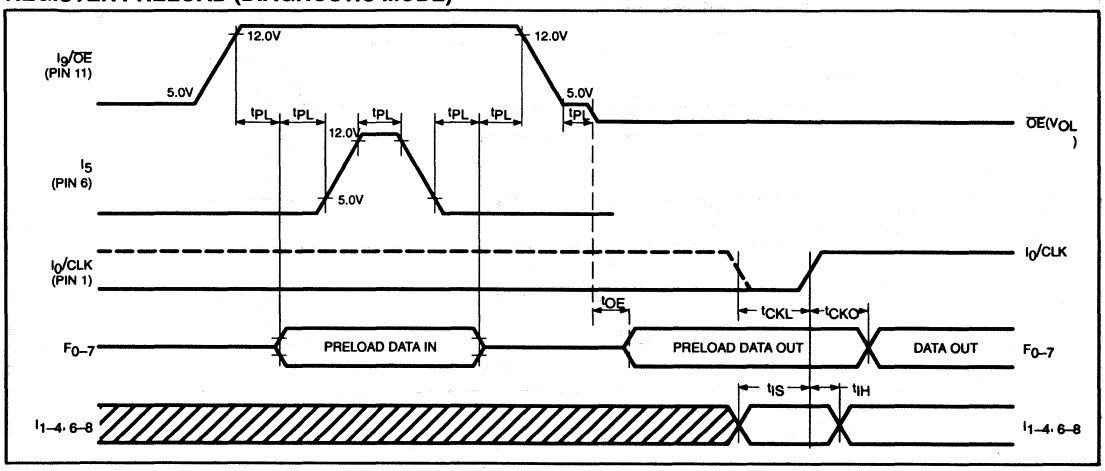
REGISTER PRELOAD FUNCTION (DIAGNOSTIC MODE ONLY)

In order to facilitate the testing of state machine/controller designs, a diagnostic mode register preload feature has been incorporated into the P3C18V8Z series device. This feature enables the user to load the registers with predetermined states while a super voltage is applied to Pins 11 and 6 ($I_9/\overline{OE}$ and I_5). (See diagram for timing and sequence.)

To read the data out, Pins 11 and 6 must be returned to normal TTL levels. The outputs, F_{0-7}, must be enabled in order to read data out. The Q outputs of the registers will reflect data in as input via F_{0-7} during preload. Subsequently, the register Q output via the feedback path will reflect the data in as input via F_{0-7}.

Refer to the voltage waveform for timing and voltage references. t_{PL} = 10µsec.

REGISTER PRELOAD (DIAGNOSTIC MODE)



LOGIC PROGRAMMING

The P3C18V8Z series is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Philips Semiconductors' SNAP design software package. ABEL™ and CUPL™ 90 design software packages also support the P3C18V8Z architecture.

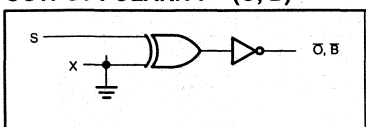
All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

P3C18V8Z logic designs can also be generated using the program table entry format, which is detailed on the following pages. This program table entry format is supported by SNAP only.

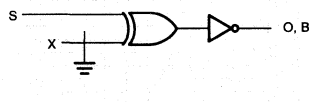
With Logic programming, the AND/OR/EX-OR gate input connections necessary to implement the desired logic function are coded directly from logic equations using the Program Table. Similarly, various OMC configurations are implemented by programming the Architecture Control bits AC1 and AC2. Note that the configuration cell is automatically programmed based on the OMC configuration.

In this table, the logic state of variables I, P and B associated with each Sum Term S is assigned a symbol which results in the proper fusing pattern of corresponding link pairs, defined as follows:

OUTPUT POLARITY – (O, B)

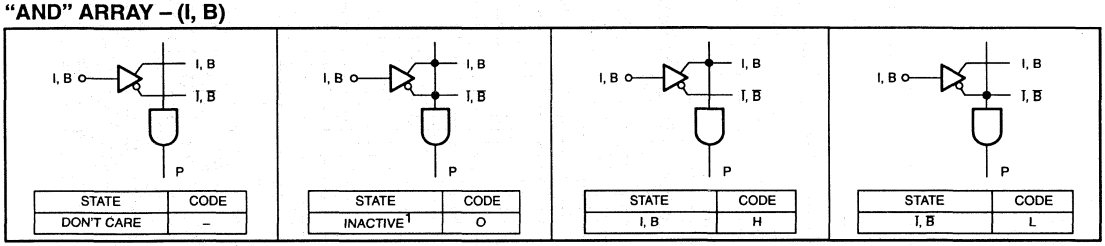


ACTIVE LEVEL	CODE
INVERTING[1]	L



ACTIVE LEVEL	CODE
NON-INVERTING	H

"AND" ARRAY – (I, B)



STATE	CODE
DON'T CARE	–

STATE	CODE
INACTIVE[1]	O

STATE	CODE
I, B	H

STATE	CODE
$\overline{I}$, $\overline{B}$	L

NOTE:
1. A factory shipped unprogrammed device is configured such that all cells are in a conductive state.

ERASURE CHARACTERISTICS (For Quartz Window Packages Only)

The erasure characteristics of the P3C18V8Z Series devices are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lighting could erase a typical P3C18V8Z in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the P3C18V8Z is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure for the P3C18V8Z is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15Wsec/cm^2. The erasure time with this dosage is approximately 30 to 35 minutes using an ultraviolet lamp with a 12,000µW/cm^2 power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a CMOS EPLD can be exposed to without damage is 7258Wsec/cm^2). Exposure of these CMOS EPLDs to high intensity UV light for longer periods may cause permanent damage.

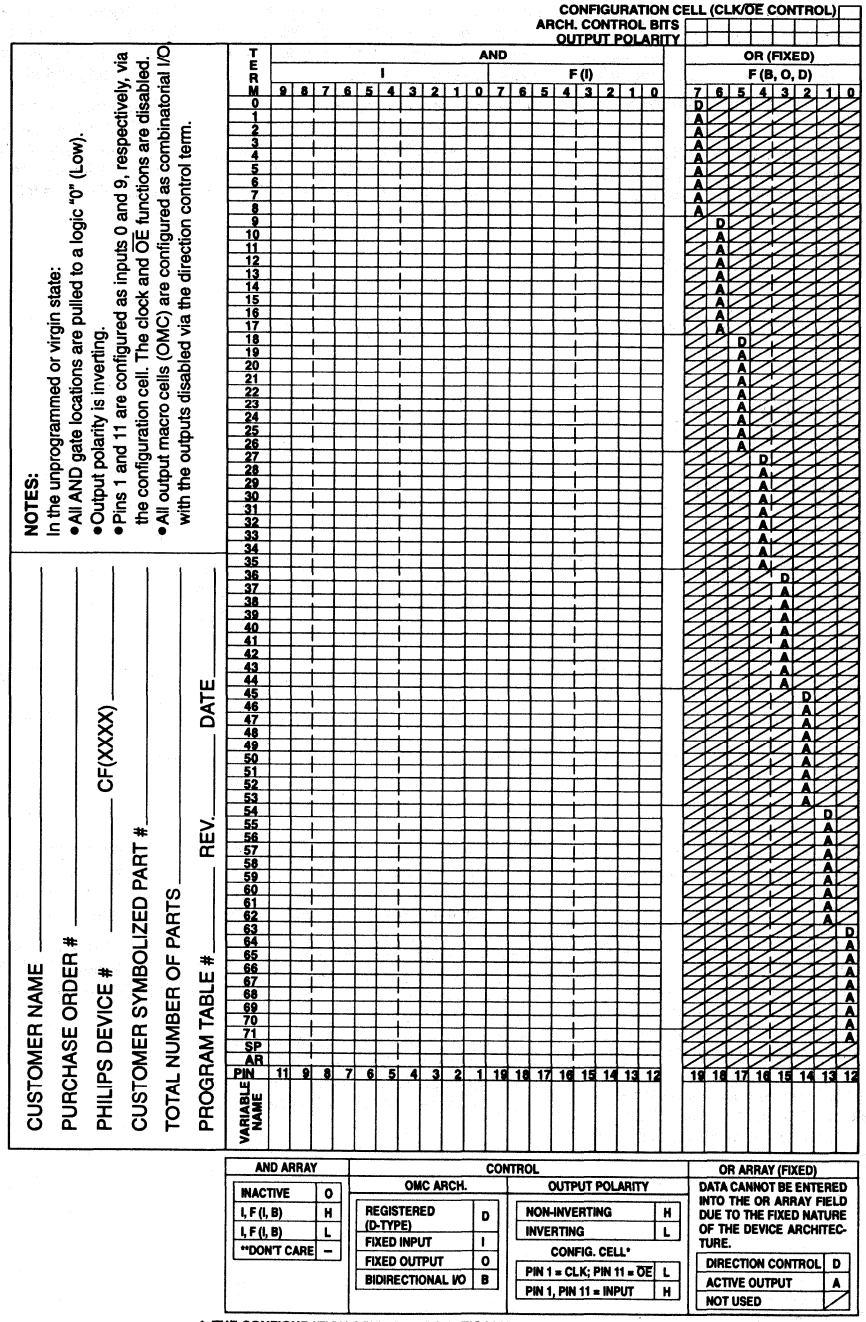
The maximum number of guaranteed erase/write cycles is 50. Data retention exceeds 20 years.

ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.

3 Volt zero standby power universal PAL devices

P3C18V8Z35/P3C18V8ZI

PROGRAM TABLE



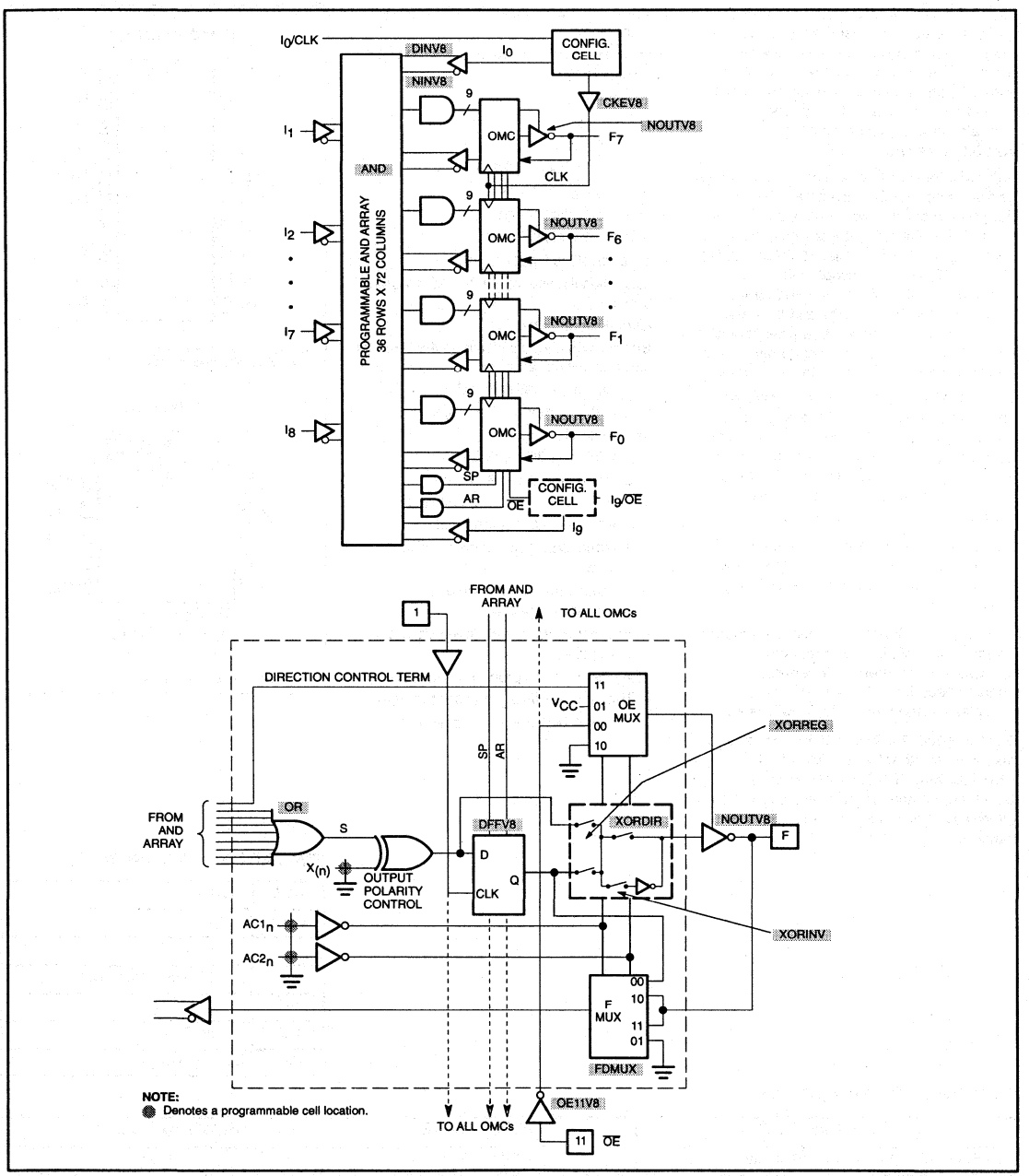
AND ARRAY	
INACTIVE	0
I, F (I, B)	H
I, F (I, B)	L
**DON'T CARE	–

CONTROL			
OMC ARCH.		OUTPUT POLARITY	
REGISTERED (D-TYPE)	D	NON-INVERTING	H
FIXED INPUT	I	INVERTING	L
FIXED OUTPUT	O	CONFIG. CELL*	
BIDIRECTIONAL I/O	B	PIN 1 = CLK; PIN 11 = OE	L
		PIN 1, PIN 11 = INPUT	H

OR ARRAY (FIXED)	
DATA CANNOT BE ENTERED INTO THE OR ARRAY FIELD DUE TO THE FIXED NATURE OF THE DEVICE ARCHITECTURE.	
DIRECTION CONTROL	D
ACTIVE OUTPUT	A
NOT USED	

* THE CONFIGURATION CELL IS AUTOMATICALLY PROGRAMMED BASED ON THE OMC ARCHITECTURE.
** FOR SP, AR: "–" IS NOT ALLOWED.

SNAP RESOURCE SUMMARY DESIGNATIONS



3 Volt BiCMOS Versatile GAL–type PLD — LVT16V8–7

DESCRIPTION

The LVT16V8–7 is a V–type GAL device designed to operate over the 3.0 to 3.6 volt range. This versatile device is fabricated using the BiCMOS process which produces superior performance, low noise and reduced ground bounce. The reduction from 5V to 3.3V also dramatically reduces power to less than 0.5 watts (worst case).

This industry standard device is ideal for high performance systems which have been designed to operate with 3.3V ± 0.3V power supplies, as well as systems which are operating with dual supplies (5.0V and 3.3V). The LVT16V8–7 can accept both 3.3 and 5.0V input levels without the need for level translators. Both the inputs and I/O have high state reverse current flow protection to insure that the outputs are not damaged if the 3V LVT16V8 is interfaced with 5V devices.

The LVT16V8–7 is designed with metastable hardened flip–flops so that the outputs can never display a metastable state due to set up or hold time violations. If set up or hold times are violated, the outputs will not glitch or display a metastable state (however propagation delays may extend).

Active bus-hold circuitry is provided to eliminate the need for external resistors to hold unused or floating inputs at valid logic levels.

The LVT16V8's flexible architecture supports a wide variety of high performance applications: counters, shift registers, address decoders, state machines, multiplexers and random logic collection.

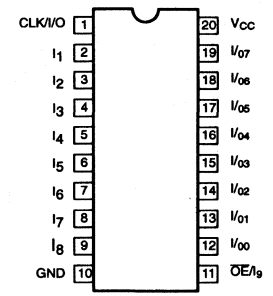
The LVT16V8–7 is identical, in function and fuse map, to other industry standard EEPROM and EPROM 16V8 devices. Development and programming support are offered by Philips and other third party vendors.

FEATURES

- Advanced low voltage BiCMOS process technology
- Ultra high performance over the 3.0 to 3.6 voltage range
  - 7.5ns T_{PD}
  - 5.0ns T_{IS}
  - 5.0ns T_{CKO}
  - 110 MH_Z F_{MAX} (internal feedback)
  - 143 MH_Z clock rate
- Low power dissipation
  - 300mW typical
- 5V compatible inputs and I/O
- Exceptional noise immunity and low ground bounce
- Live insertion/extraction
- Bus-hold data inputs eliminate the need for external pull up resistors.
- Wide package availability; DIP, PLCC, SOL
- Metastable hardened Flip-Flops
- Architectural Flexibility
  - Emulates all 20 pin PAL devices
  - Up to 16 inputs and 8 outputs
  - Independently programmable I/O macrocells (4 configurations)
  - Independently programmable output polarity
  - Product term output enable for combinatorial functions
  - Register Preload and Power Up reset of all registers
- Development and programming support
  - Third party software and programmers
  - Philips SNAP development software

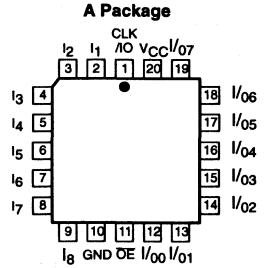
PIN CONFIGURATIONS

D and N Packages



N = Plastic DIP (300mil-wide)
D = Plastic SOL (300mil-wide)

A Package



A = Plastic Leaded Chip Carrier

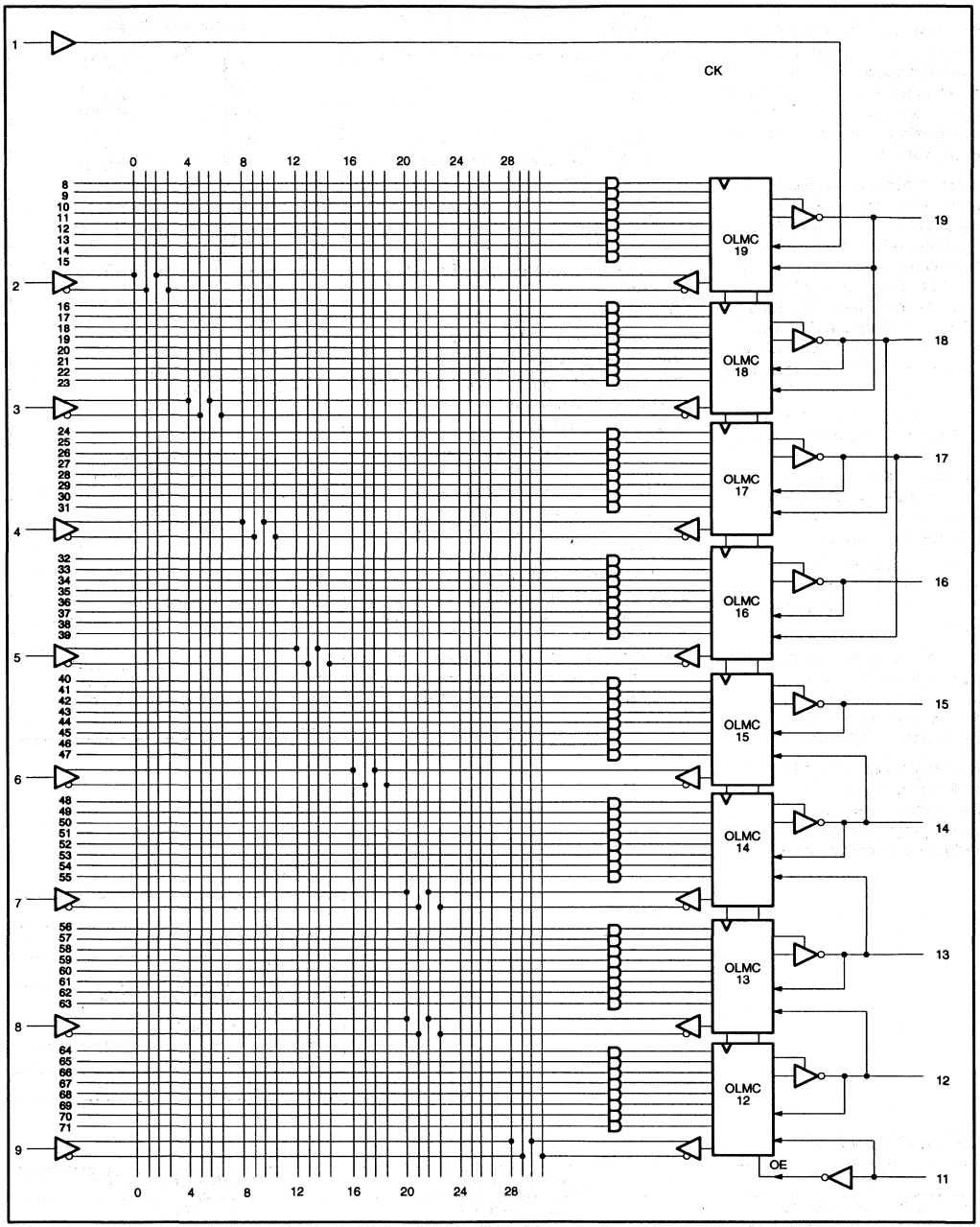
PIN TABLE DESCRIPTIONS

CLK	Clock
GND	Ground
I	Input
I/O	Input/Output Macro Cell
NC	No connect
$\overline{OE}$	Output Enable
V_{CC}	Supply Voltage

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	DRAWING NUMBER
20–Pin Plastic Dual In–Line Package	LVT16V8–7N	0408B
20–Pin Plastic Leaded Chip Carrier	LVT16V8–7A	0400E
20–Pin Plastic Small Outline Large Package	LVT16V8–7D	0172D

LOGIC DIAGRAM



3 Volt BiCMOS Versatile GAL–type PLD — LVT20V8–7

DESCRIPTION

The LVT20V8–7 is a V–type GAL device designed to operate over the 3.0 to 3.6 volt range. This versatile device is fabricated using the BiCMOS process which produces superior performance, low noise and reduced ground bounce. The reduction from 5V to 3.3V also dramatically reduces power to less than 0.5 watts (worst case).

This industry standard device is ideal for high performance systems which have been designed to operate with 3.3V ± 0.3V power supplies, as well as systems which are operating with dual supplies (5.0V and 3.3V). The LVT20V8–7 can accept both 3.3 and 5.0V input levels without the need for level translators. Both the inputs and I/O have high state reverse current flow protection to insure that the outputs are not damaged if the 3V LVT20V8 is interfaced with 5V devices.

The LVT20V8–7 is designed with metastable hardened flip–flops so the outputs can never display a metastable state due to set up or hold time violations. If set up or hold times are violated, the outputs will not glitch or display a metastable state (however propagation delays may extend).

Active bus-hold circuitry is provided to eliminate the need for external pull up resistors to hold unused or floating inputs at valid logic levels.

The LVT20V8's flexible architecture supports a wide variety of high performance applications: counters, shift registers, address decoders, state machines, multiplexers and random logic collection.

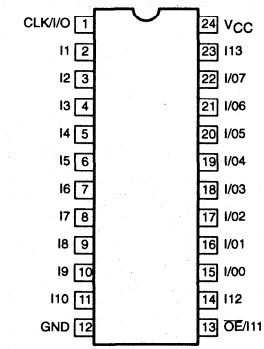
The LVT20V8–7 is identical, in function and fuse map, to other industry standard EEPROM and EPROM 20V8 devices. Development and programming support are offered by Philips and other third party vendors.

FEATURES

- Advanced low voltage BiCMOS process technology
- Ultra high performance over the 3.0 to 3.6 voltage range
  - 7.5ns T_{PD}
  - 5.0ns T_{IS}
  - 6.0ns T_{CKO}
  - 110MHz F_{MAX} (internal feedback)
  - 143MHz clock rate
- Low power dissipation
  - 300mW typical
- 5V compatible inputs and I/O
- Exceptional noise immunity and low ground bounce
- Live insertion/extraction
- Metastable hardened Flip–Flops
- Wide package availability; DIP, PLCC, SOL
- Bus-hold data inputs eliminate the need for external pull up resistors
- Architectural Flexibility
  - Emulates all 24 pin PAL devices
  - Up to 20 inputs and 8 outputs
  - Independently programmable I/O macrocells (4 configurations)
  - Independently programmable output polarity
  - Product term output enable for combinatorial functions
  - Register Preload and Power Up reset of all registers
- Development and programming support
  - Third party software and programmers
  - Philips SNAP development software

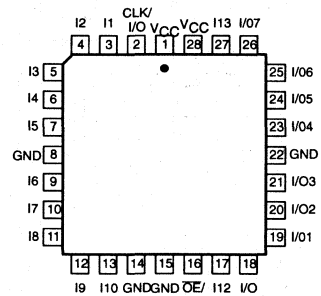
PIN CONFIGURATIONS

D and N Packages



N = Plastic DIP (300mil-wide)
D = Plastic SOL (300 mil–wide)

A Package



A = Plastic Leaded Chip Carrier

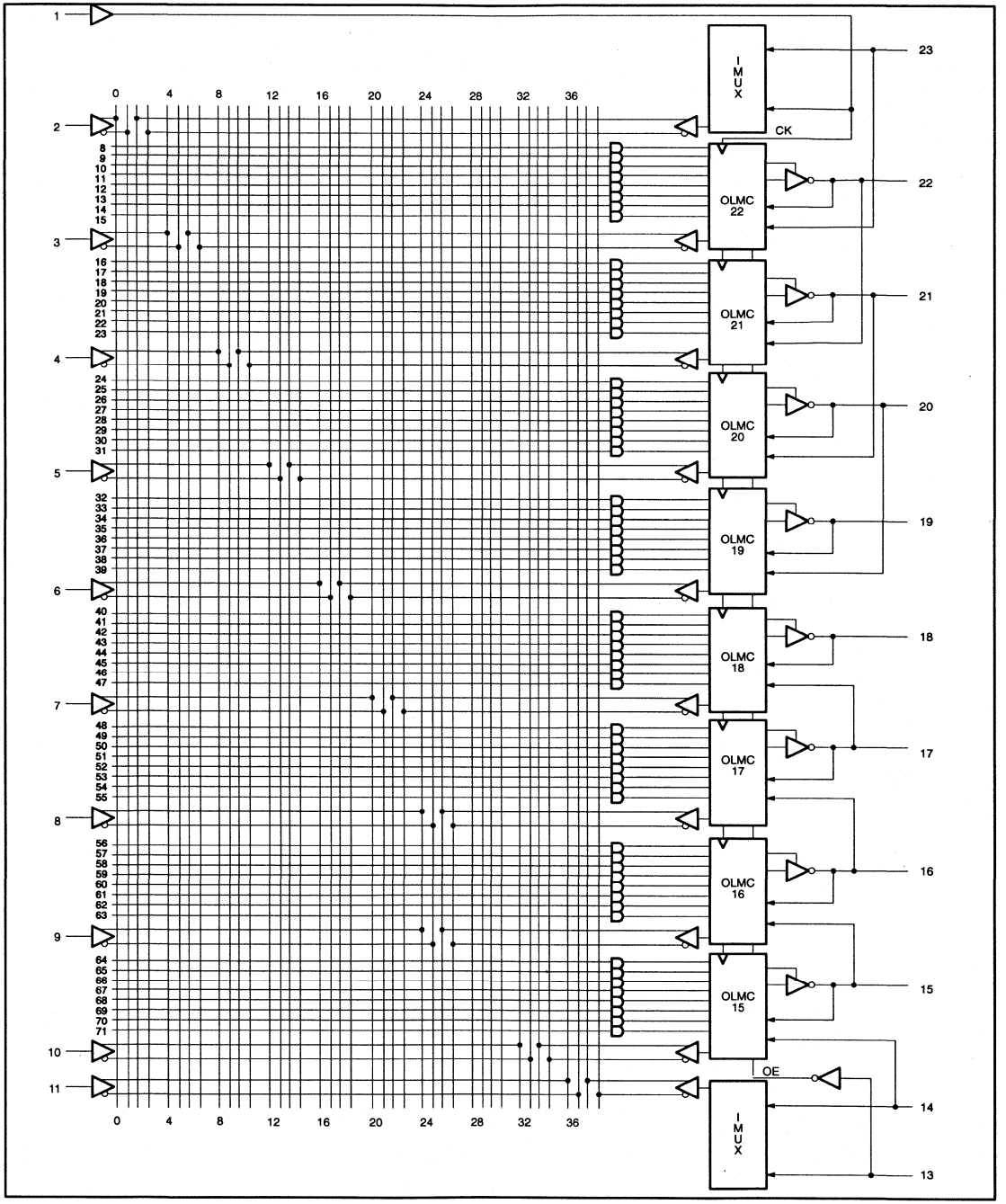
PIN TABLE DESCRIPTIONS

CLK	Clock
GND	Ground
I	Input
I/O	Input/Output Macro Cell
NC	No connect
$\overline{OE}$	Output Enable
V_{CC}	Supply Voltage

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	DRAWING NUMBER
24–Pin Plastic Dual In–Line Package	LVT20V8–7N	0410D
28–Pin Plastic Leaded Chip Carrier	LVT20V8–7A	0401F
24–Pin Plastic Small Outline Large Package	LVT20V8–7D	0173D

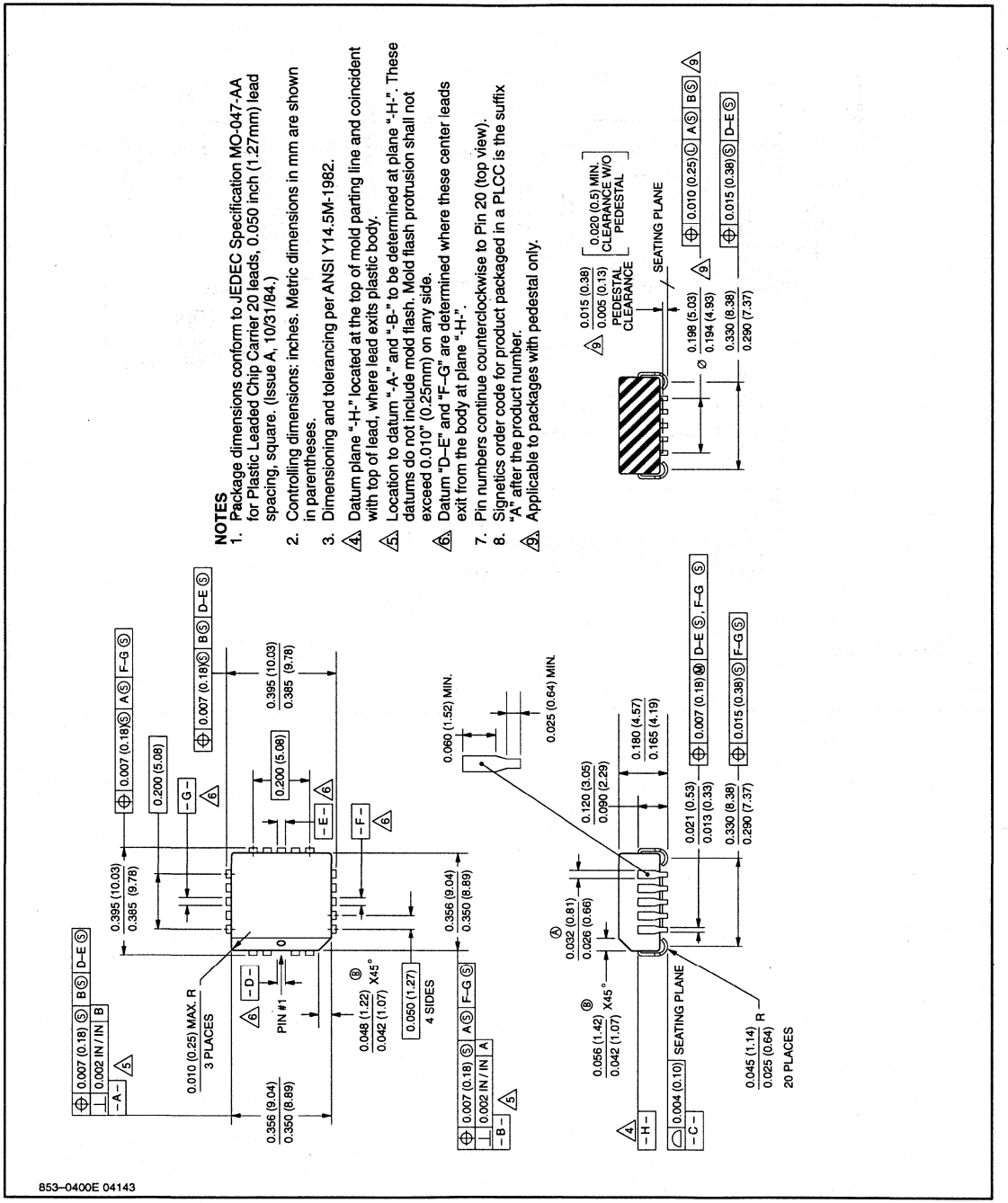
LOGIC DIAGRAM



PACKAGE INFORMATION

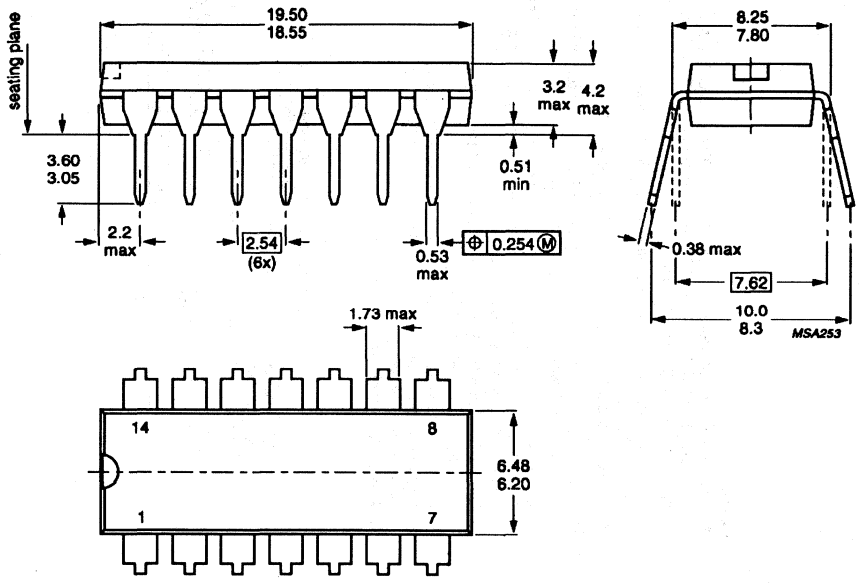
Package Outlines

0400E 20-PIN (350 mils wide) PLASTIC LEADED CHIP CARRIER (A) PACKAGE



Package Outlines

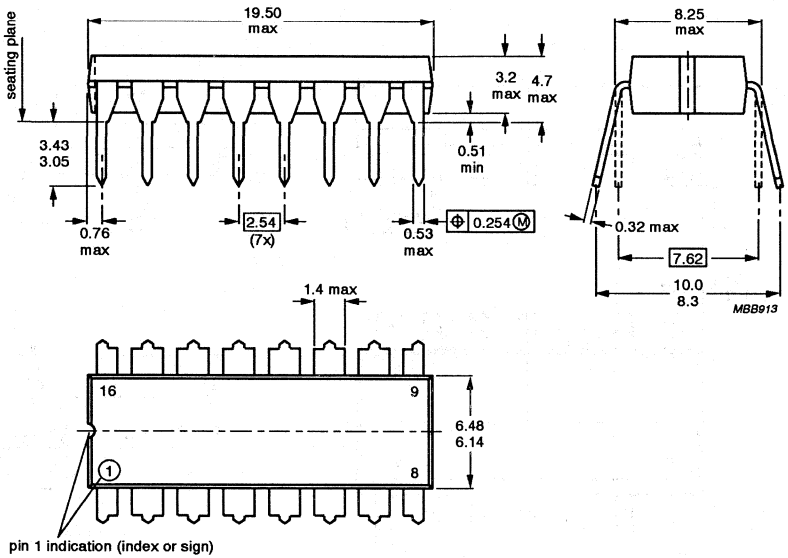
SOT27-1 PLASTIC DUAL IN-LINE PACKAGE; 14 LEADS (300 MIL).



Dimensions in mm.

Package Outlines

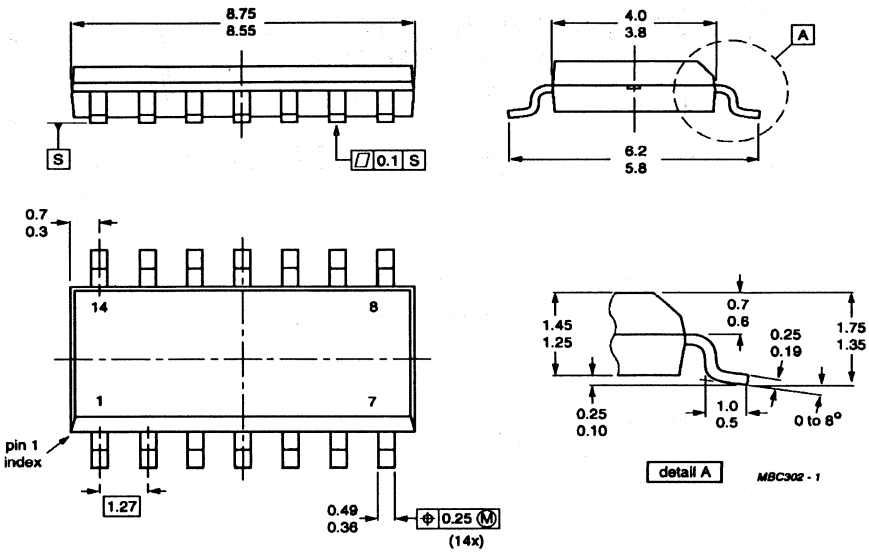
SOT38-3 PLASTIC DUAL IN-LINE PACKAGE; 16 LEADS (300 MIL)



Dimensions in mm.

Package Outlines

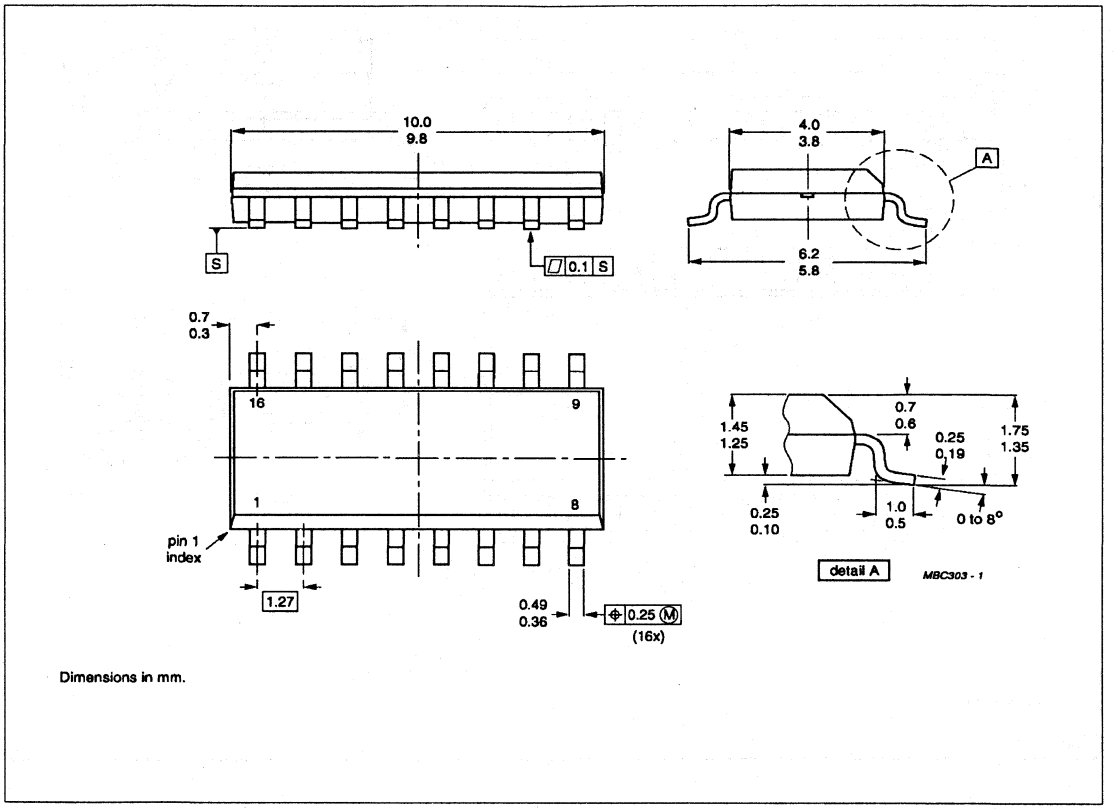
SOT108-1 PLASTIC SMALL OUTLINE PACKAGE; 14 LEADS; BODY WIDTH 3.9 MM.



Dimensions in mm.

Package Outlines

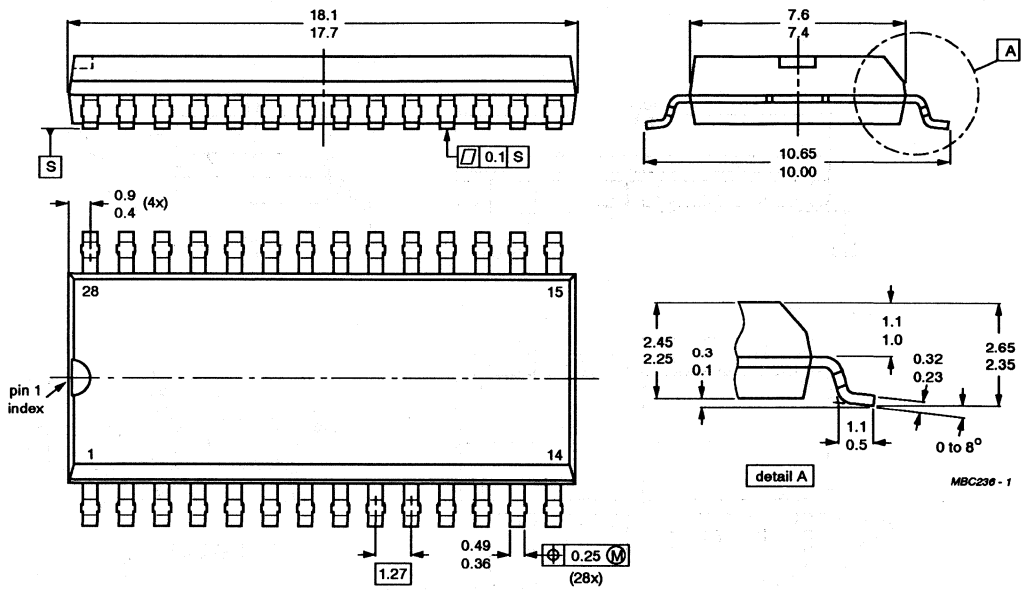
SOT109-1 **PLASTIC SMALL OUTLINE PACKAGE; 16 LEADS; BODY WIDTH 3.9 MM; LOW STAND-OFF HEIGHT**



Dimensions in mm.

Package Outlines

SOT136–1 PLASTIC SMALL OUTLINE PACKAGE; 28 LEADS; LARGE BODY

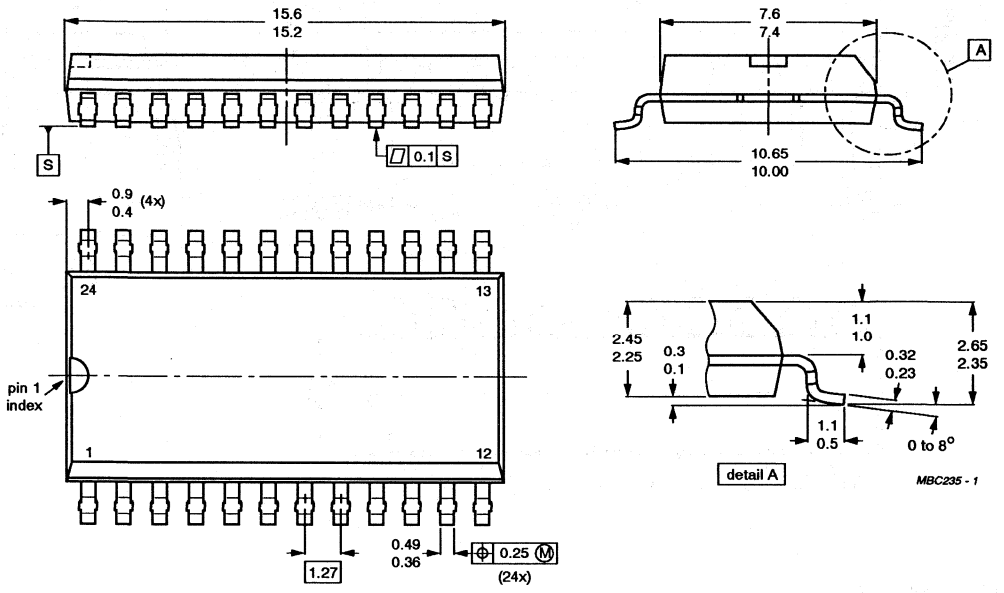


Dimensions in mm.

SOT136–1

Package Outlines

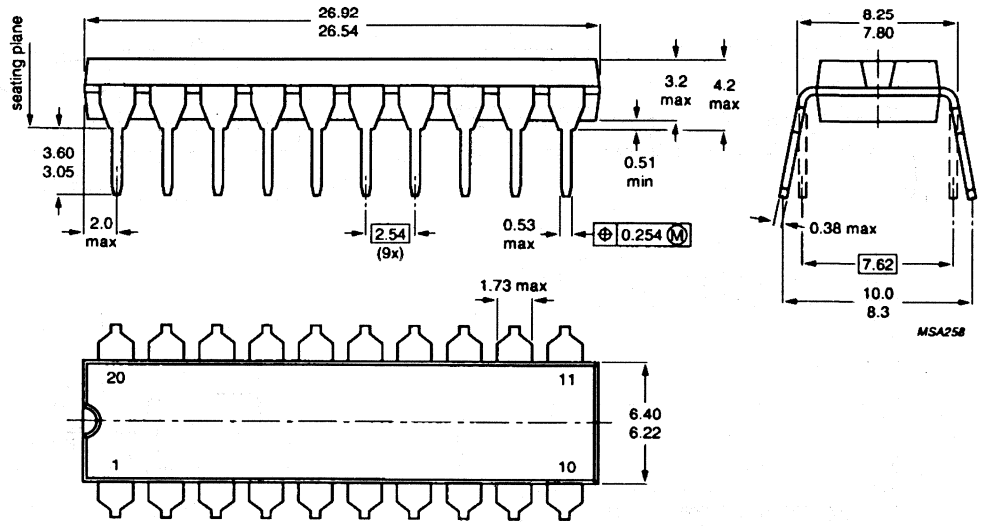
SOT137-1 PLASTIC SMALL OUTLINE PACKAGE; 24 LEADS; LARGE BODY



Dimensions in mm.

Package Outlines

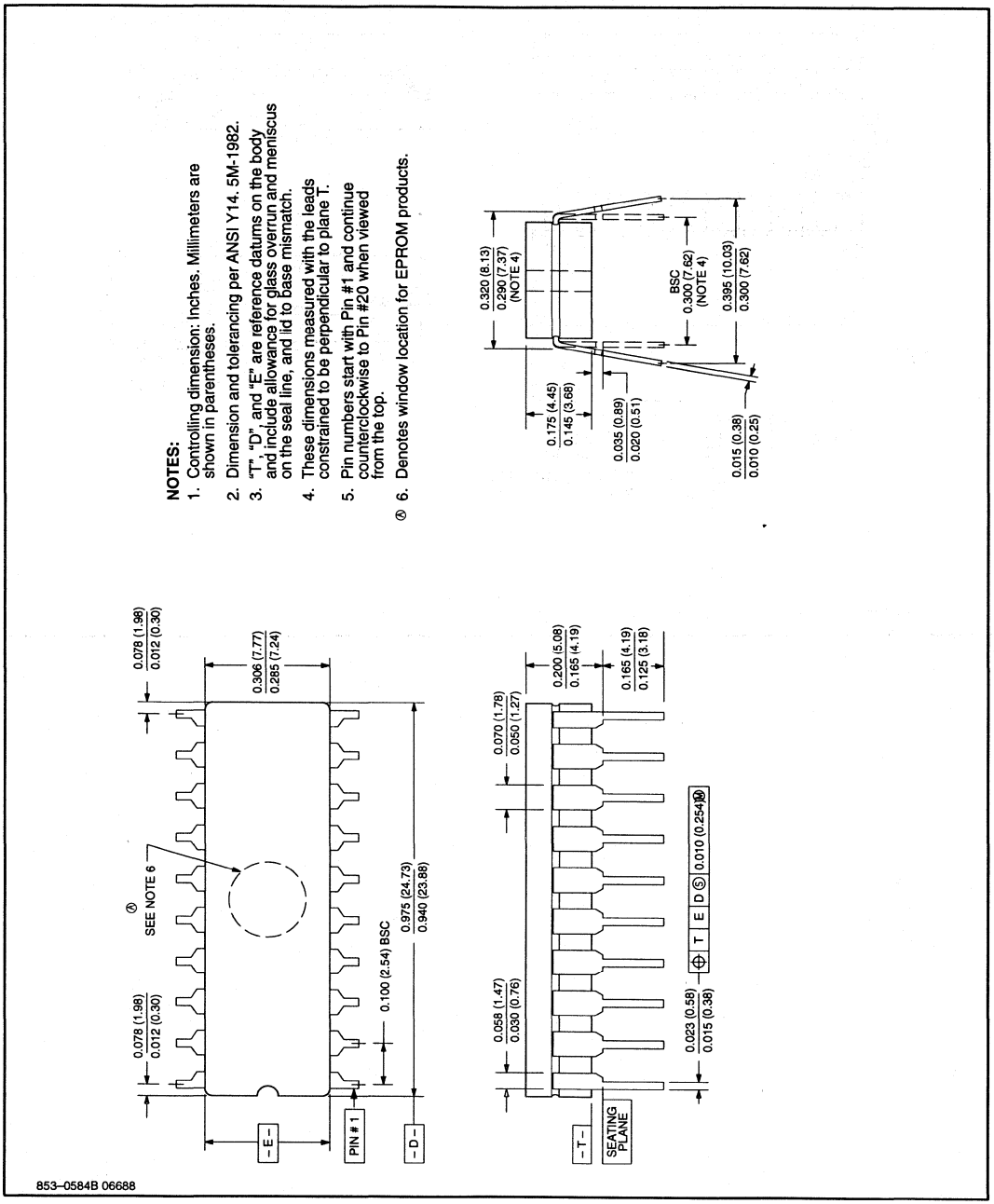
SOT146-1 PLASTIC DUAL IN-LINE PACKAGE; 20 LEADS (300 mil)



Dimensions in mm

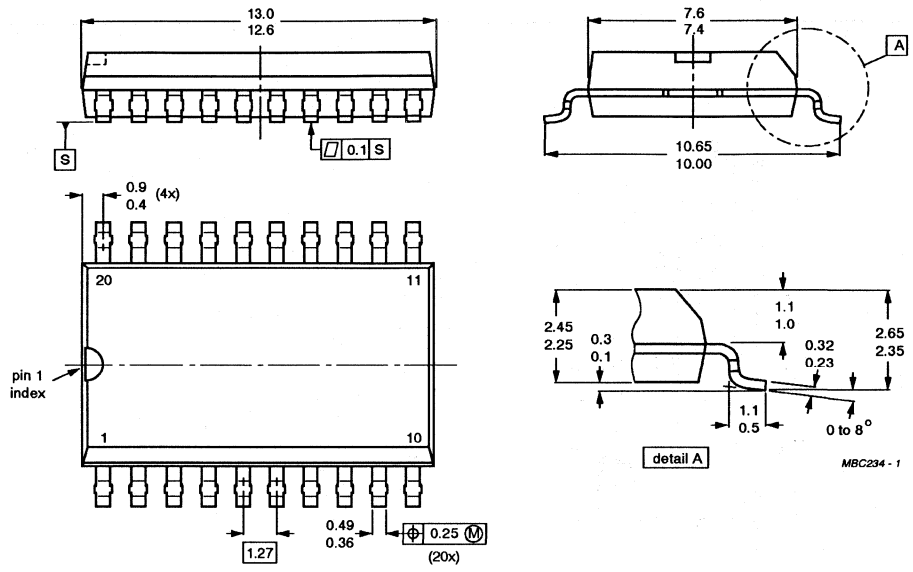
Package Outlines

SOT152/0584B 20-PIN (300 mils wide) CERAMIC DUAL IN-LINE (F) PACKAGE (WITH WINDOW (FA) PACKAGE)



Package Outlines

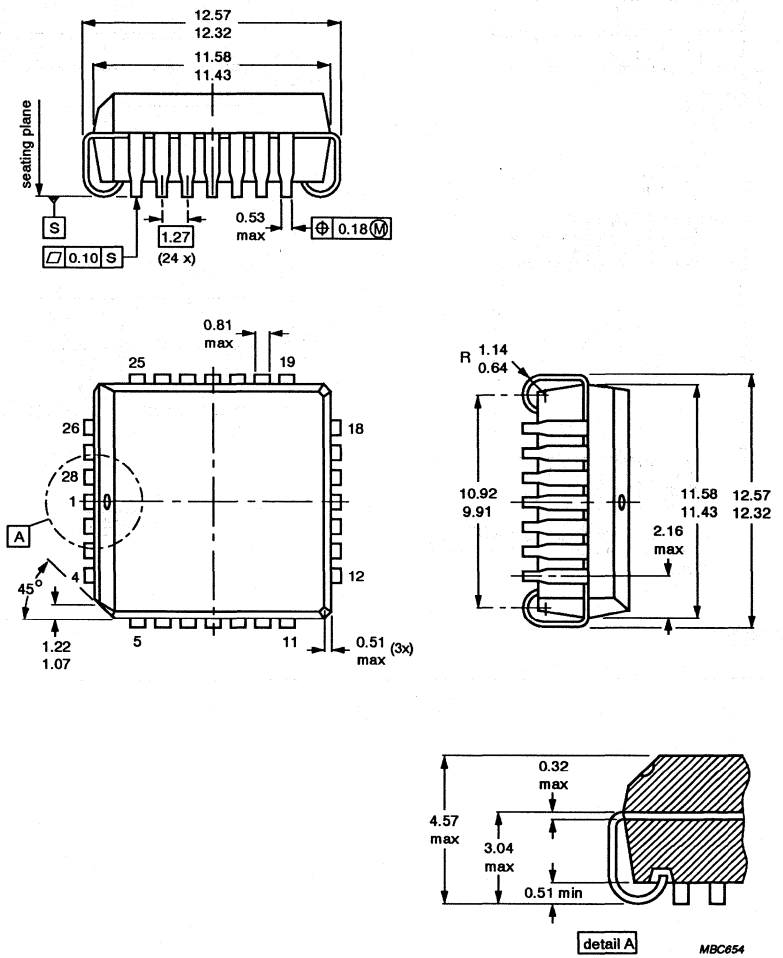
SOT163-1 PLASTIC SMALL OUTLINE PACKAGE; 20 LEADS; LARGE BODY (SO20L)



Dimensions in mm.

Package Outlines

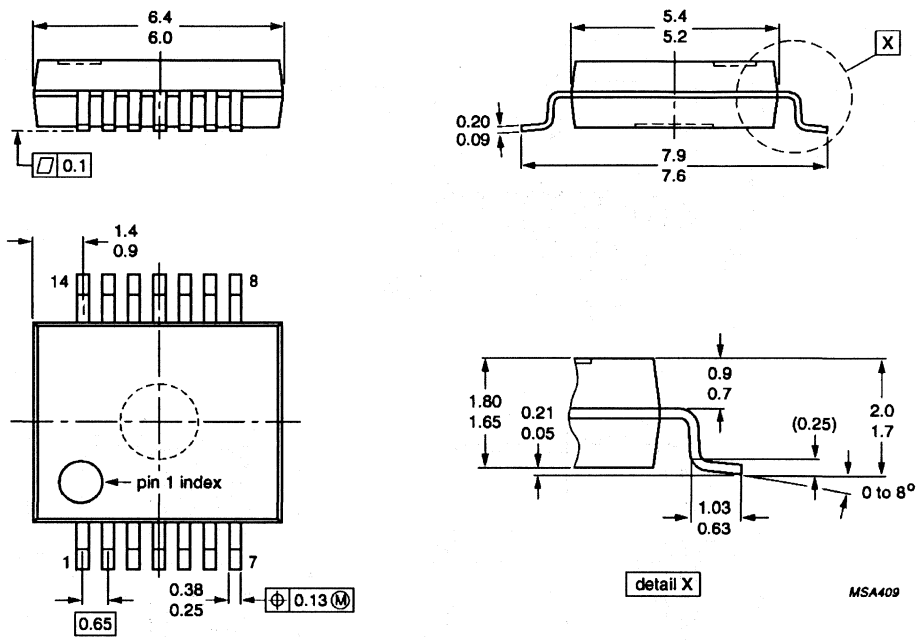
SOT261-2 PLASTIC LEADED CHIP CARRIER, 28 LEADS



Dimensions in mm.

Package Outlines

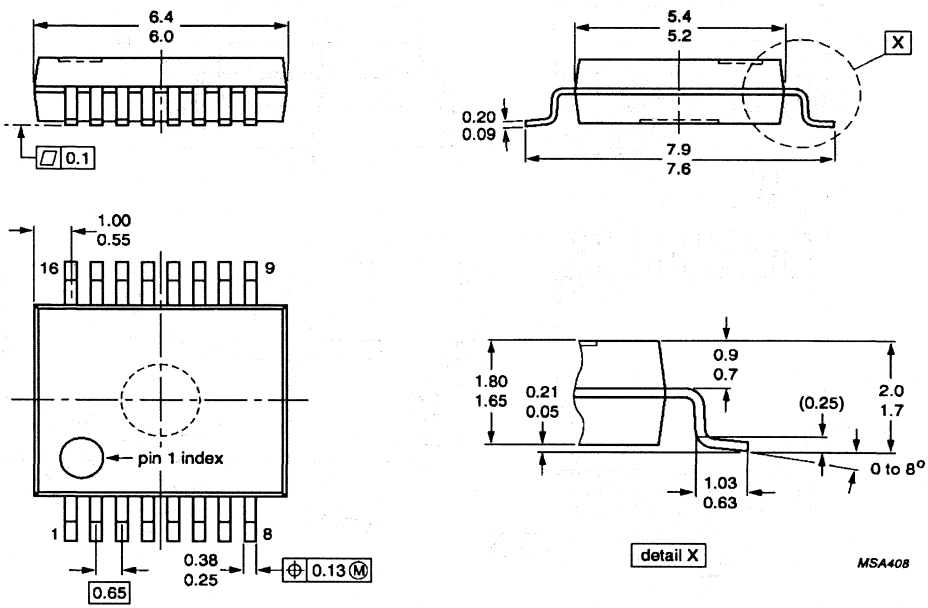
SOT337-1 PLASTIC SHRINK SMALL OUTLINE PACKAGE; 14 LEADS; BODY WIDTH 5.3 MM.



Dimensions in mm.

Package Outlines

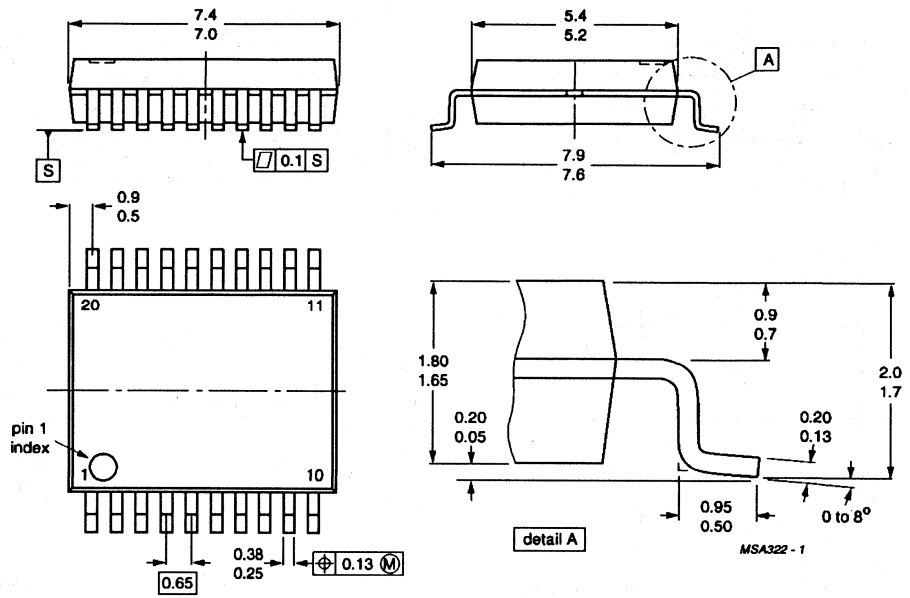
SOT338-1 PLASTIC SHRINK SMALL OUTLINE PACKAGE; 18 LEADS; BODY WIDTH 5.3 MM.



Dimensions in mm.

Package Outlines

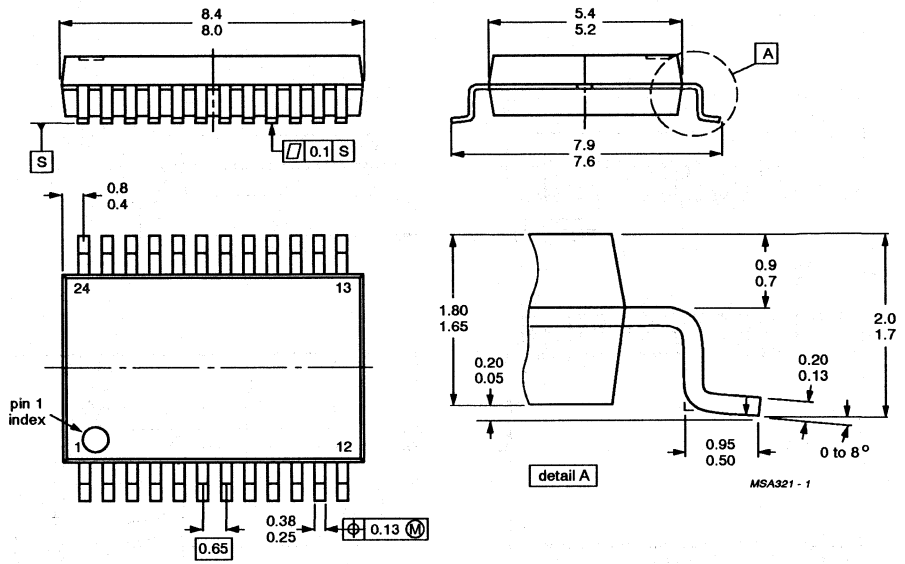
SOT339-1 PLASTIC SHRINK SMALL OUTLINE PACKAGE; 28 LEADS; BODY WIDTH 5.3 MM.



Dimensions in mm.

Package Outlines

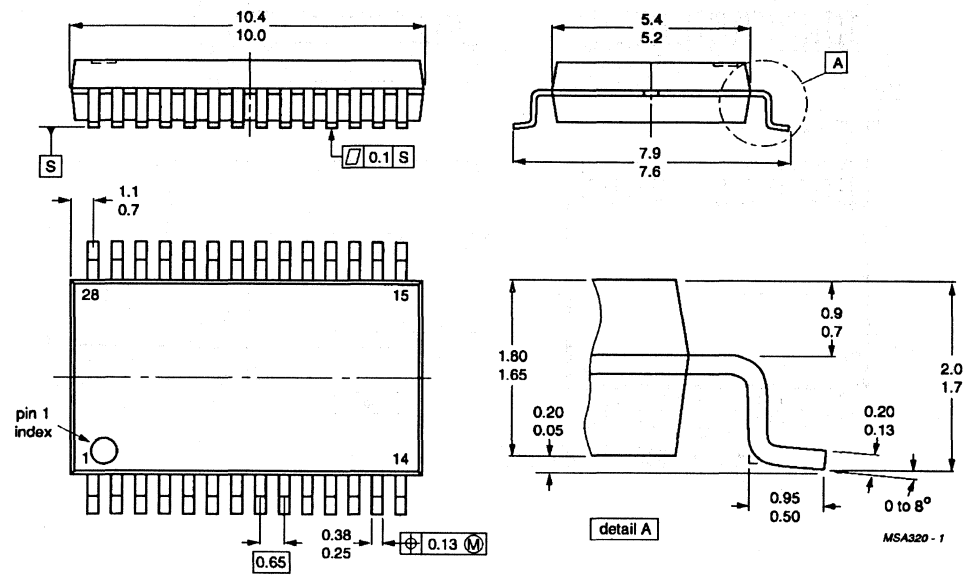
SOT340–1 PLASTIC SHRINK SMALL OUTLINE PACKAGE; 24 LEADS; MEDIUM BODY



Dimensions in mm.

Package Outlines

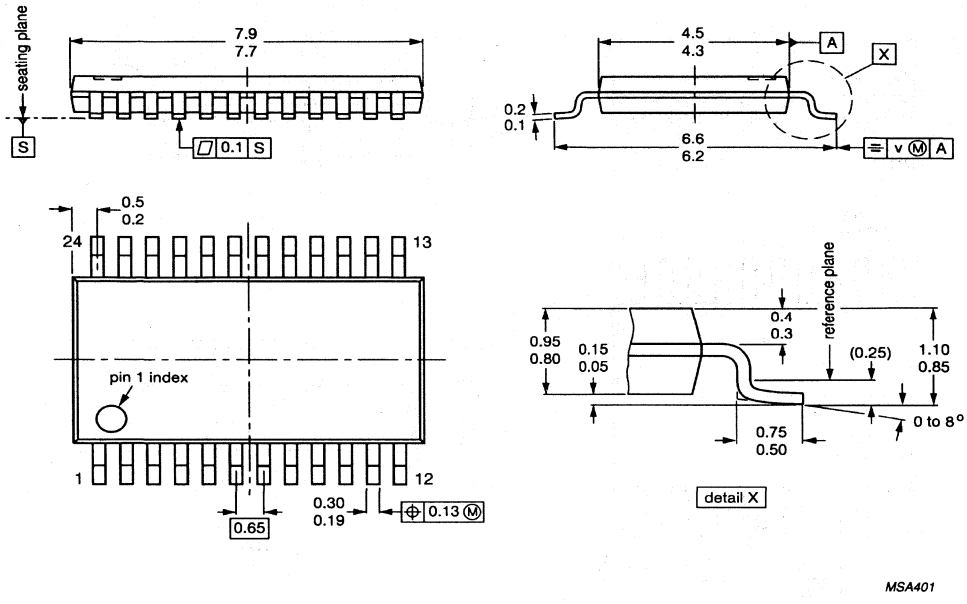
SOT341–1 PLASTIC SHRINK SMALL OUTLINE PACKAGE; 28 LEADS; BODY WIDTH 5.3 MM.



Dimensions in mm.

Package Outlines

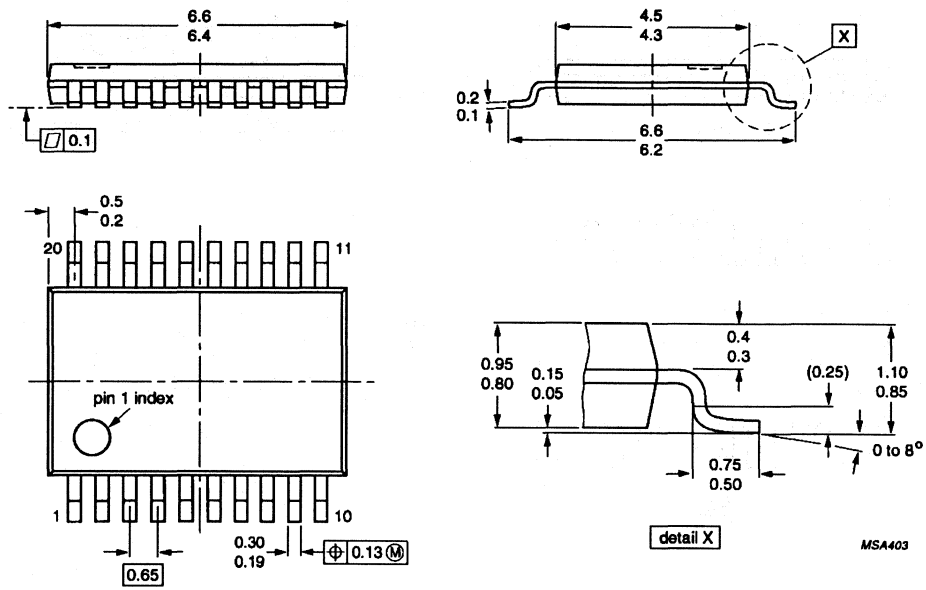
SOT355–1 PLASTIC SHRINK THIN SMALL OUTLINE PACKAGE; 24 LEADS; MEDIUM BODY



Dimensions in mm.

Package Outlines

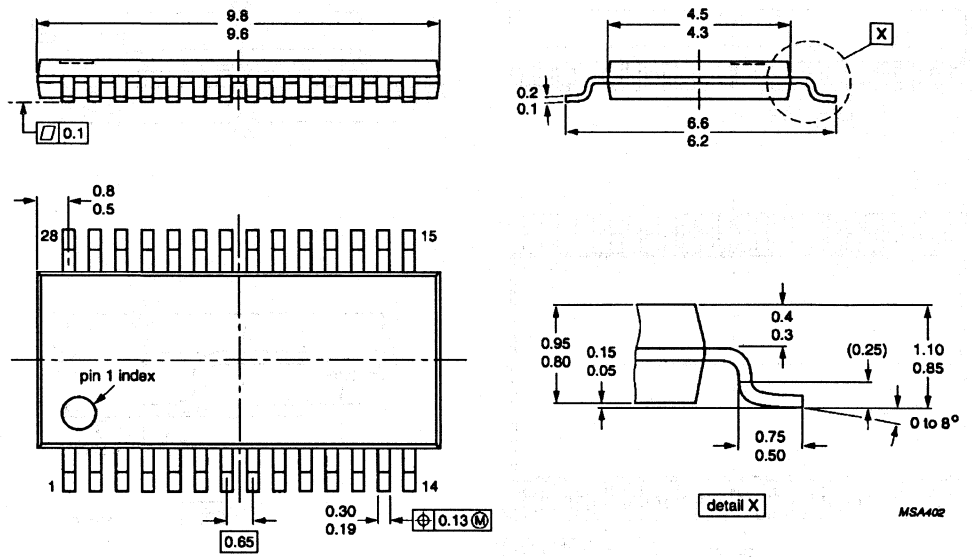
SOT360-1 PLASTIC THIN SHRINK SMALL OUTLINE PACKAGE; 20 LEADS; BODY WIDTH 4.4 MM.



Dimensions in mm.

Package Outlines

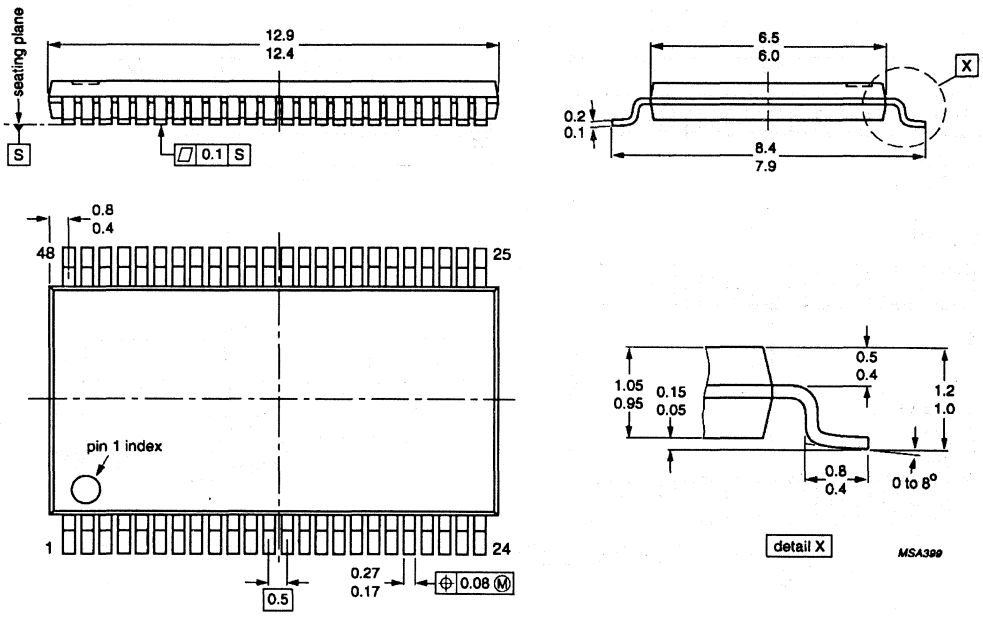
SOT361-1 PLASTIC THIN SHRINK SMALL OUTLINE PACKAGE; 28 LEADS; BODY WIDTH 4.4 MM.



Dimensions in mm.

Package Outlines

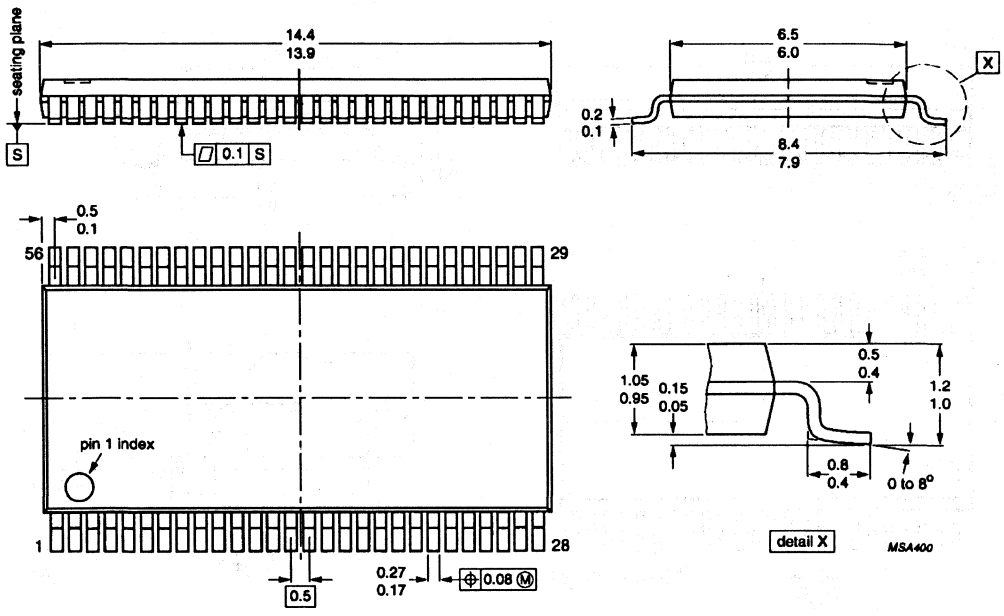
SOT362-1 PLASTIC THIN SHRINK SMALL OUTLINE PACKAGE; 48 LEADS; BODY WIDTH 6.1 MM.



Dimensions in mm.

Package Outlines

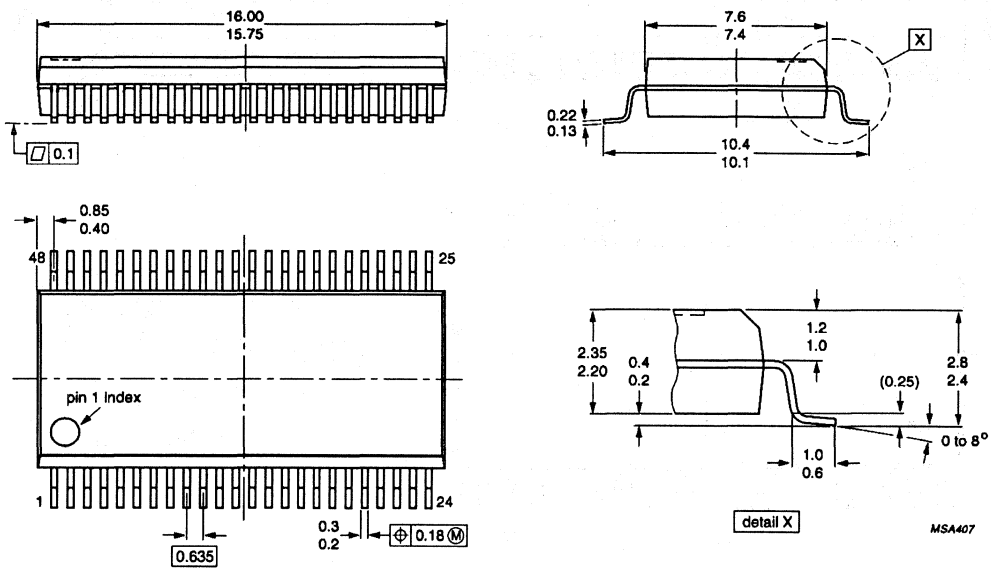
SOT364-1 PLASTIC THIN SHRINK SMALL OUTLINE PACKAGE; 56 LEADS; BODY WIDTH 5.1 MM.



Dimensions in mm.

Package Outlines

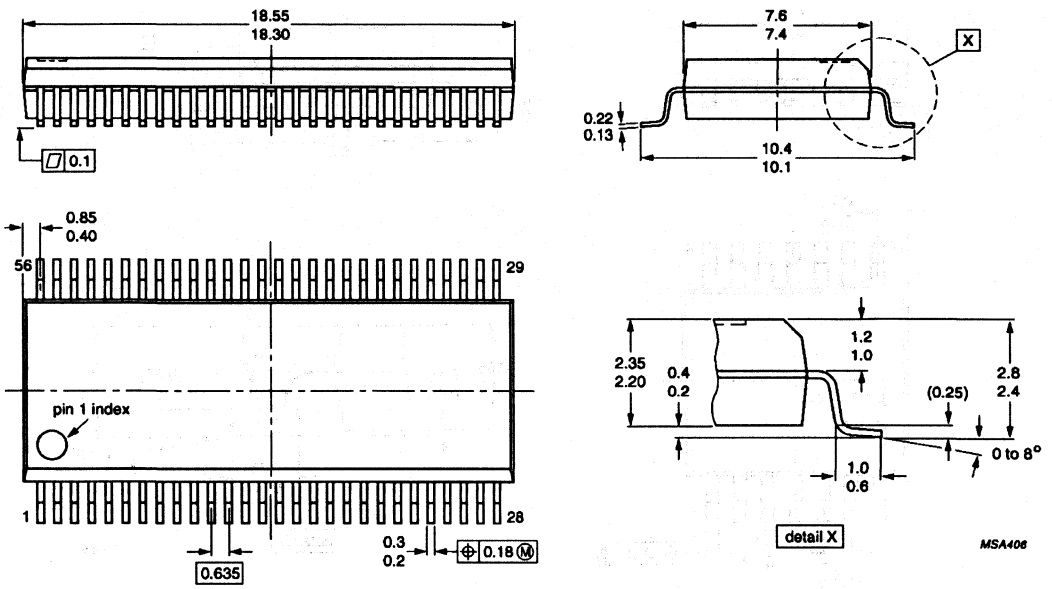
SOT370-1 PLASTIC SHRINK SMALL OUTLINE PACKAGE; 48 LEADS; BODY WIDTH 7.5 MM.



Dimensions in mm.

Package Outlines

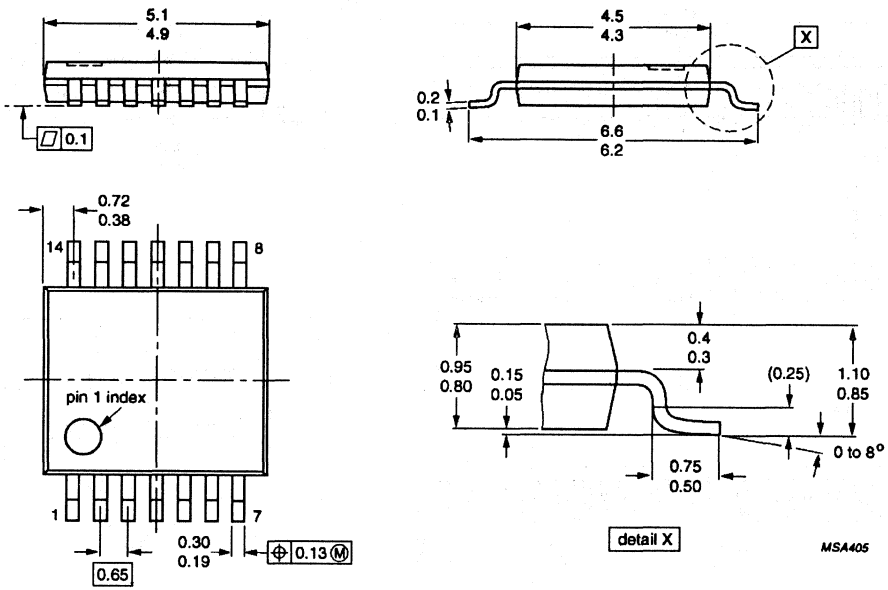
SOT371-1 PLASTIC SHRINK SMALL OUTLINE PACKAGE; 56 LEADS; BODY WIDTH 7.5 MM.



Dimensions in mm.

Package Outlines

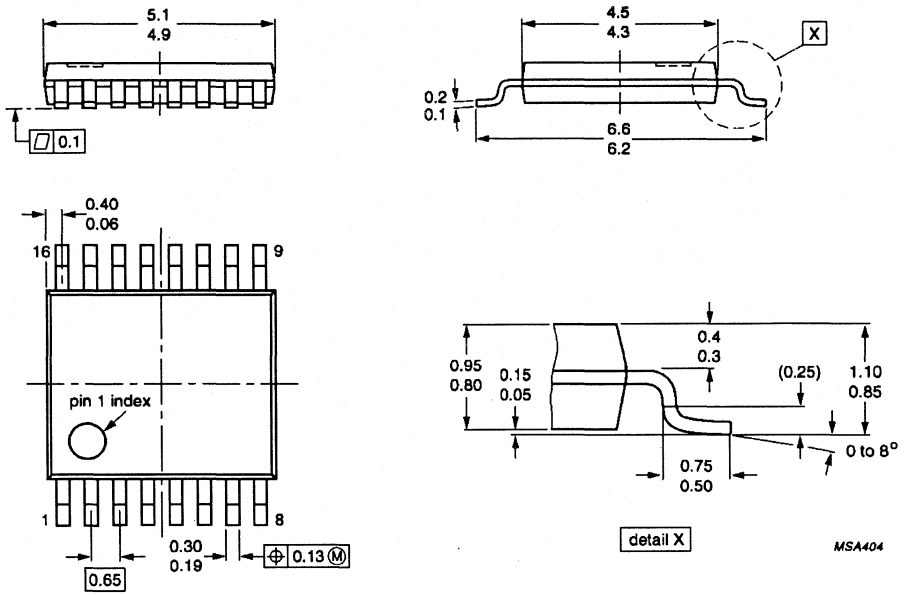
SOT402-1 PLASTIC THIN SHRINK SMALL OUTLINE PACKAGE; 14 LEADS; BODY WIDTH 4.4 MM.



Dimensions in mm.

Package Outlines

SOT403-1 PLASTIC THIN SHRINK SMALL OUTLINE PACKAGE; 16 LEADS; BODY WIDTH 4.4 MM.



Dimensions in mm.

NORTH AMERICAN SALES OFFICES, REPRESENTATIVES AND DISTRIBUTORS

North American Sales Offices, Representatives and Distributors

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07/20/94

DATA HANDBOOK SYSTEM

Data handbook system

Appendix A

DATA HANDBOOK SYSTEM

Philips Semiconductors data handbooks contain all pertinent data available at the time of publication and each is revised and reissued regularly.

Loose data sheets are sent to subscribers to keep them up-to-date on additions or alterations made during the lifetime of a data handbook.

Catalogs are available for selected product ranges (some catalogs are also on floppy discs).

Our data handbook titles are listed here.

Integrated Circuits

Book	*Title*
IC01	Semiconductors for Radio and Audio Systems
IC02	Semiconductors for Television and Video Systems
IC03	Semiconductors for Telecom Systems
IC04	CMOS HE4000B Logic Family
IC05	Advanced Low-power Schottky (ALS) Logic Series
IC06	High-speed CMOS Logic Family
IC08	100K ECL Logic Families
IC10	Memories
IC11	General-purpose/Linear ICs
IC12	Display Drivers and Microcontroller Peripherals (planned)
IC13	Programmable Logic Devices (PLD)
IC14	8048-based 8-bit Microcontrollers
IC15	FAST TTL Logic Series
IC16	ICs for Clocks and Watches
IC18	Semiconductors for In-car Electronics and General Industrial Applications (planned)
IC17	RF/Wireless Communications
IC19	Semiconductors for Datacom: LANs, UARTs, Multi-protocol Controllers and Fibre Optics
IC20	80C51-based 8-bit Microcontrollers
IC21	68000-based 16-bit Microcontrollers (planned)
IC22	ICs for Multi-media Systems (planned)
IC23	QUBiC Advanced BiCMOS Bus Interface Logic ABT, MULTIBYTE™
IC24	Low Voltage CMOS & BiCMOS Logic

Discrete Semiconductors

Book	*Title*
SC01	Diodes
SC02	Power Diodes
SC03	Thyristors and Triacs
SC04	Small-signal Transistors
SC05	Low-frequency Power Transistors and Hybrid IC Power Modules
SC06	High-voltage and Switching NPN Power Transistors
SC07	Small-signal Field-effect Transistors
SC08a	RF Power Bipolar Transistors
SC08b	RF Power MOS Transistors
SC09	RF Power Modules
SC10	Surface Mounted Semiconductors
SC13	Power MOS Transistors including TOPFETs and IGBTs
SC14	RF Wideband Transistors, Video Transistors and Modules
SC15	Microwave Transistors
SC16	Wideband Hybrid IC Modules
SC17	Semiconductor Sensors

Professional Components

PC01	High-power Klystrons and Accessories
PC06	Circulators and Isolators

MORE INFORMATION FROM PHILIPS SEMICONDUCTORS?

For more information about Philips Semiconductors data handbooks, catalogs and subscriptions contact your nearest Philips Semiconductors national organization, select from the **address list on the back cover of this handbook**. Product specialists are at your service and inquiries are answered promptly.

Data handbook system — Appendix A

OVERVIEW OF PHILIPS COMPONENTS DATA HANDBOOKS

Our sister product division, Philips Components, also has a comprehensive data handbook system to support their products. Their data handbook titles are listed here.

Display Components

Book	*Title*
DC01	Colour Display Components Colour TV Picture Tubes and Assemblies Colour Monitor Tube Assemblies
DC02	Monochrome Monitor Tubes and Deflection Units
DC03	Television Tuners, Coaxial Aerial Input Assemblies
DC05	Flyback Transformers, Mains Transformers and General-purpose FXC Assemblies

Magnetic Products

MA01	Soft Ferrites
MA03	Piezoelectric Ceramics Specialty Ferrites
MA04	Dry-reed Switches

Passive Components

PA01	Electrolytic Capacitors
PA02	Varistors, Thermistors and Sensors
PA03	Potentiometers and Switches
PA04	Variable Capacitors
PA05	Film Capacitors
PA06	Ceramic Capacitors
PA07	Quartz Crystals for Special and Industrial Applications
PA08	Fixed Resistors
PA10	Quartz Crystals for Automotive and Standard Applications
PA11	Quartz Oscillators

Professional Components

PC04	Photo Multipliers
PC05	Plumbicon Camera Tubes and Accessories
PC07	Vidicon and Newvicon Camera Tubes and Deflection Units
PC08	Image Intensifiers
PC12	Electron Multipliers

MORE INFORMATION FROM PHILIPS COMPONENTS?

For more information contact your nearest Philips Components national organizaiton shown in the following list.

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